

7 Pin SIL 4 Tap TTL Compatible Active Delay Lines

TAP DELAYS ±5% or ±2 nS †	TOTAL DELAYS ±5% or ±2 nS†	Part Number	TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	Part Number
1.0 ± 0.5	*3 ± 0.5	EPA1190-4	15	60	EPA1190-60
2.0 ± 1	*8 ± 1.0	EPA1190-6	20	80	EPA1190-80
3.0 ± 1	*9	EPA1190-9	25	100	EPA1190-100
4.0 ± 1.5	*12	EPA1190-12	30	120	EPA1190-120
5.0	*15	EPA1190-15	35	140	EPA1190-140
6.0	*18	EPA1190-18	40	160	EPA1190-160
7.0	28	EPA1190-28	50	200	EPA1190-200
8.0	32	EPA1190-32	60	240	EPA1190-240
9.0	36	EPA1190-36	70	280	EPA1190-280
10.0	40	EPA1190-40	80	320	EPA1190-320
12.0	48	EPA1190-48	90	360	EPA1190-360
			100	400	EPA1190-400

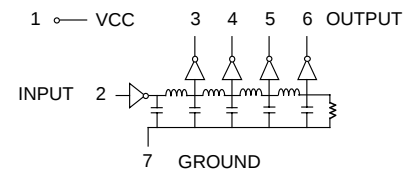
†Whichever is greater. Delay times referenced from input to leading edges at 25°C, 5.0V, with no load.

*Delay times referenced from 1st tap

1st tap is the inherent delay: approx. 7 nS

DC Electrical Characteristics					
Parameter	Test Conditions	Min	Max	Unit	
V _{OH}	High-Level Output Voltage	V _{CC} = min. V _{IL} = max. I _{OH} = max	2.7		V
V _{OL}	Low-Level Output Voltage	V _{CC} = min. V _{IH} = min. I _{OL} = max	0.5		V
V _{IK}	Input Clamp Voltage	V _{CC} = min. I _I = I _{IK}	-1.2V		V
I _{IH}	High-Level Input Current	V _{CC} = max. V _{IN} = 2.7V	50		µA
		V _{CC} = max. V _{IN} = 5.25V	1.0		mA
I _{IL}	Low-Level Input Current	V _{CC} = max. V _{IN} = 0.5V	-2		mA
I _{OS}	Short Circuit Output Current	V _{CC} = max. V _{OUT} = 0.	-40		mA
	(One output at a time)				
I _{CCH}	High-Level Supply Current	V _{CC} = max. V _{IN} = OPEN	115		mA
I _{CCL}	Low-Level Supply Current	V _{CC} = max. V _{IN} = 0	115		mA
T _{RO}	Output Rise Time	T _d ≤ 500 nS (0.75 to 2.4 Volts)	4		nS
N _H	Fanout High-Level Output	V _{CC} = max. V _{OH} = 2.7V	20		TTL LOAD
N _L	Fanout Low-Level Output	V _{CC} = max. V _{OL} = 0.5V	10		TTL LOAD

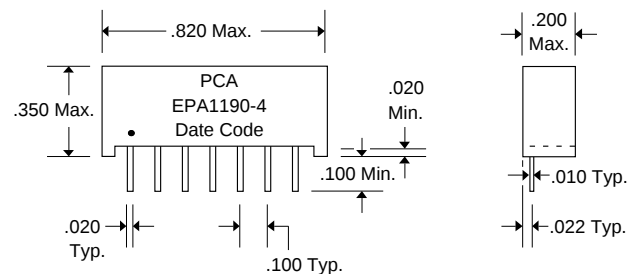
Schematic



Recommended Operating Conditions		Min	Max	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High-Level Input Voltage	2.0		V
V _{IL}	Low-Level Input Voltage		0.8	V
I _{IK}	Input Clamp Current		-18	mA
I _{OH}	High-Level Output Current		-1.0	mA
I _{OL}	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle	40		%
T _A	Operating Free-Air Temperature	0	+70	°C

*These two values are inter-dependent.

Package Dimensions



Input Pulse Test Conditions @ 25° C			Unit
E _{IN}	Pulse Input Voltage	3.2	Volts
P _W	Pulse Width % of Total Delay	110	%
T _{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
P _{RR}	Pulse Repetition Rate @ T _d ≤ 200 nS	1.0	MHz
	Pulse Repetition Rate @ T _d > 200 nS	100	KHz
V _{CC}	Supply Voltage	5.0	Volts