Description

The Edge6420 is a monolithic device which has 64 integrated DACs that are designed specifically for all per channel wide-voltage and current levels needed for pin electronics inside automatic test equipment. The chip can also be used for other applications requiring multiple integrated voltage or current DAC outputs.

Voltage DACs

- Wide voltage (17V range)
- Adjustable full scale range
- Adjustable minimum output
- 13 bits resolution

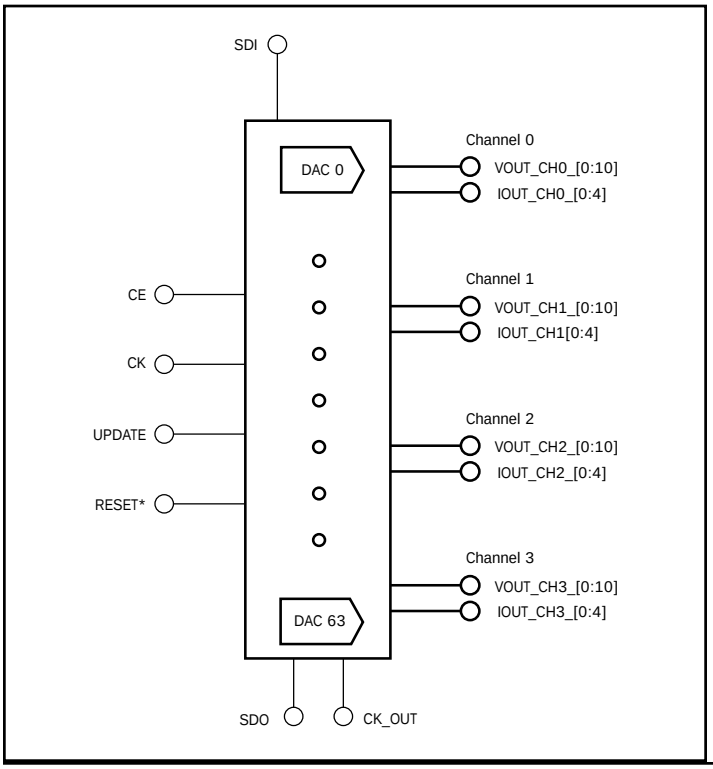
Current DACs

- ~3.6 mA full scale range
- Adjustable full scale range
- 6/13 bits resolution

The DACs are programmed using a 1 bit serial interface.

The inclusion of 64 total DACs into 1 package offers an extremely high density, flexible solution normally implemented using multiple components.

Functional Block Diagram



Features

64 Total DACs/Package Including:

- Wide Voltage Output Range (17V Range); Useful for Supervoltage
- 44 Voltage DACs / Package
- 20 Current DACs / Package
- Adjustable Full Scale Range
- Adjustable Output Voltage Offset
- Small 13x13mm BGA Package
- All DACs are Guaranteed Monotonic

Applications

- Test Equipment
- Applications requiring multiple programmable voltage and currents

PIN Description

Ball Name	Ball Location	Description
VOUT_CH[0:3]_[0:4]	G13, G15, F14, F13, F15, G3, F1, F2, F3, E1, J3, J1, K2, K3, K1, J13, K15, K14, K13, L15	Group A DAC output volages for channels 0 to 3.
VOUT_CH[0:3]_[5:6]	E14, E15, E2, E3, L2, L1, L14, L13	Group B DAC output voltages for channels 0 to 3.
VOUT_CH[0:3]_[7:8]	E13, D14, D1, D2, L3, M2, M15, M14	Group C DAC output voltaqges for channels 0 to 3.
VOUT_CH[0:3]_[9:10]	D15, D13, D3, C1, M1, M3, M13, N15	Group D DAC output voltages for channels 0 to 3.
IOUT_CH[0:3]_[0:1]	C15, C14, B1, C2, N1, N2, P15, N14	Group E DAC output voltages for channels 0 to 3.
IOUT_CH[0:3]_[2:4]	H14, H15, G14, H3, G1, G2, H2, H1, J2, H13, J15, J14	Group F DAC output voltages for channels 0 to 3.
R_MASTER	P5	Master external resistor used to define the reference current for the gain and offset setting block for voltage DACs.
R_GAIN_(A,B,C,D,E,F)	P11, R10, N10, P10, R9, N9	Pins for external resistor to set current gain for both voltage and current output DACs.
R_OFFSET_(A,B,C,D)	R6, P6, N6, R5	Pins for external resistor to set the offset voltage for Group A, B, C, and D voltage output DAC's.
SDI	B10	Serial data input.
CK	A11	Clock for the input data shift register.
UPDATE	C6	Strobe to transfer the shift register data to the DACs.
CE	A10	Chip enable.
RESET*	C5	Active low chip reset. Sets the DACs to a known default state.
SDO	B5	Serial Data Out.
CK_OUT	A6	Regenerated clock output for daisy chain purposes.
SCAN_OUT	B11	Analog output test pin.
TEST_MODE	B6	Test mode pin for internal scan.
VREF	C9	Reference input (for a 2.5V band gap).
AVCC	C3, C12, N4, R12	Positive analog voltage supply.
AVDD	C7, N7	Analog 5V supply.
VEE	A9, R8, B9, P9	Negative analog voltage supply.
AGND	B8, N8	Analog ground (minimize noise).
SGND	A8, R7	Supply ground.
DVDD	B7, P7	Digital voltage supply.
DGND	C8, P8	Digital supply ground.

PIN Description *(continued)*

13mm x 13mm CSPBGA Package

A1 Ball Pad Indicator

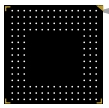
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	A1 1	A2 144	A3 142	A4 139	A5 136	A6 134 CK_OUT	A7 131	A8 128 SGND	A9 125 VEE	A10 122 CE	A11 119 CK	A12 116	A13 113	A14 111	A15 109
B	B1 3 IOUT_CH1_0	B2 2	B3 141	B4 138	B5 135 SDO	B6 132 TEST_MODE	B7 129 DVDD	B8 127 AGND	B9 124 VEE	B10 121 SDI	B11 118 SCAN_OUT	B12 115	B13 112	B14 110	B15 108
C	C1 5 VOUT_CH1_10	C2 4 IOUT_CH1_1	C3 143 AVCC	C4 140	C5 137 RESET*	C6 133 UPDATE	C7 130 AVDD	C8 126 DGND	C9 123 VREF	C10 120	C11 117	C12 114 AVCC	C13 107	C14 105 IOUT_CH0_1	C15 106 IOUT_CH0_0
D	D1 8 VOUT_CH1_7	D2 7 VOUT_CH1_8	D3 6 VOUT_CH1_9	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13 104 VOUT_CH0_10	D14 102 VOUT_CH0_8	D15 103 VOUT_CH0_9
E	E1 11 VOUT_CH1_4	E2 10 VOUT_CH1_5	E3 9 VOUT_CH1_6	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13 101 VOUT_CH0_7	E14 99 VOUT_CH0_5	E15 100 VOUT_CH0_6
F	F1 14 VOUT_CH1_1	F2 13 VOUT_CH1_2	F3 12 VOUT_CH1_3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13 97 VOUT_CH0_3	F14 96 VOUT_CH0_2	F15 98 VOUT_CH0_4
G	G1 17 IOUT_CH1_3	G2 16 IOUT_CH1_4	G3 15 VOUT_CH1_0	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13 94 VOUT_CH0_0	G14 93 IOUT_CH0_4	G15 95 VOUT_CH0_1
H	H1 20 IOUT_CH2_3	H2 19 IOUT_CH2_2	H3 18 IOUT_CH1_2	H4	H5						H11	H12	H13 90 IOUT_CH3_2	H14 91 IOUT_CH0_2	H15 92 IOUT_CH0_3
J	J1 23 VOUT_CH2_1	J2 21 IOUT_CH2_4	J3 22 VOUT_CH2_0	J4	J5						J11	J12	J13 87 VOUT_CH3_0	J14 88 IOUT_CH3_4	J15 89 IOUT_CH3_3
K	K1 26 VOUT_CH2_4	K2 24 VOUT_CH2_2	K3 25 VOUT_CH2_3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13 84 VOUT_CH3_3	K14 85 VOUT_CH3_2	K15 86 VOUT_CH3_1
L	L1 28 VOUT_CH2_6	L2 27 VOUT_CH2_5	L3 29 VOUT_CH2_7	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13 81 VOUT_CH3_6	L14 82 VOUT_CH3_5	L15 83 VOUT_CH3_4
M	M1 31 VOUT_CH2_9	M2 30 VOUT_CH2_8	M3 32 VOUT_CH2_10	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13 78 VOUT_CH3_9	M14 79 VOUT_CH3_8	M15 80 VOUT_CH3_7
N	N1 34 IOUT_CH2_0	N2 33 IOUT_CH2_1	N3 35	N4 42 AVCC	N5 45	N6 48 R_OFFSET_C	N7 51 AVDD	N8 54 AGND	N9 58 R_GAIN_F	N10 61 R_GAIN_C	N11 65	N12 68	N13 71	N14 76 IOUT_CH3_1	N15 77 VOUT_CH3_10
P	P1 36	P2 38	P3 40	P4 43	P5 46 R_MASTER	P6 49 R_OFFSET_B	P7 52 DVDD	P8 55 DGND	P9 57 VEE	P10 60 R_GAIN_D	P11 63 R_GAIN_A	P12 66	P13 69	P14 74	P15 75 IOUT_CH3_0
R	R1 37	R2 39	R3 41	R4 44	R5 47 R_OFFSET_D	R6 50 R_OFFSET_A	R7 53 SGND	R8 56 VEE	R9 59 R_GAIN_E	R10 62 R_GAIN_B	R11 64	R12 67 AVCC	R13 70	R14 72	R15 73

NOTE: Balls populating the inner 9x9 grid are for improved thermal dissipation. This middle grid of balls should be connected to the VEE plane or left floating. Order E6420BBG if populated middle is desired.

PIN Description *(continued)*

13mm x 13mm CSPBGA Package



A1 Ball Pad Indicator

Actual Size

Bottom View

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	A15 109	A14 111	A13 113	A12 116	A11 119 CK	A10 122 CE	A9 125 VEE	A8 128 SGND	A7 131	A6 134 CK_OUT	A5 136	A4 139	A3 142	A2 144	A1 1	A
B	B15 108	B14 110	B13 112	B12 115	B11 118 SCAN_OUT	B10 121 SDI	B9 124 VEE	B8 127 AGND	B7 129 DVDD	B6 132 TEST_MODE	B5 135 SDO	B4 138	B3 141	B2 2	B1 3 IOUT_CH1_0	B
C	C15 106 IOUT_CH0_0	C14 105 IOUT_CH0_1	C13 107	C12 114 AVCC	C11 117	C10 120	C9 123 VREF	C8 126 DGND	C7 130 AVDD	C6 133 UPDATE	C5 137 RESET*	C4 140	C3 143 AVCC	C2 4 IOUT_CH1_1	C1 5 VOUT_CH1_10	C
D	D15 103 VOUT_CH0_9	D14 102 VOUT_CH0_8	D13 104 VOUT_CH0_10	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3 6 VOUT_CH1_9	D2 7 VOUT_CH1_8	D1 8 VOUT_CH1_7	D
E	E15 100 VOUT_CH0_6	E14 99 VOUT_CH0_5	E13 101 VOUT_CH0_7	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3 9 VOUT_CH1_6	E2 10 VOUT_CH1_5	E1 11 VOUT_CH1_4	E
F	F15 98 VOUT_CH0_4	F14 96 VOUT_CH0_2	F13 97 VOUT_CH0_3	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3 12 VOUT_CH1_3	F2 13 VOUT_CH1_2	F1 14 VOUT_CH1_1	F
G	G15 95 VOUT_CH0_1	G14 93 IOUT_CH0_4	G13 94 VOUT_CH0_0	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3 15 VOUT_CH1_0	G2 16 IOUT_CH1_4	G1 17 IOUT_CH1_3	G
H	H15 92 IOUT_CH0_3	H14 91 IOUT_CH0_2	H13 90 IOUT_CH3_2	H12	H11	H10						H4	H3 18 IOUT_CH1_2	H2 19 IOUT_CH2_2	H1 20 IOUT_CH2_3	H
J	J15 89 IOUT_CH3_3	J14 88 IOUT_CH3_4	J13 87 VOUT_CH3_0	J12	J11	J10						J4	J3 22 VOUT_CH2_0	J2 21 IOUT_CH2_4	J1 23 VOUT_CH2_1	J
K	K15 86 VOUT_CH3_1	K14 85 VOUT_CH3_2	K13 84 VOUT_CH3_3	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3 25 VOUT_CH2_3	K2 24 VOUT_CH2_2	K1 26 VOUT_CH2_4	K
L	L15 83 VOUT_CH3_4	L14 82 VOUT_CH3_5	L13 81 VOUT_CH3_6	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3 29 VOUT_CH2_7	L2 27 VOUT_CH2_5	L1 28 VOUT_CH2_6	L
M	M15 80 VOUT_CH3_7	M14 79 VOUT_CH3_8	M13 78 VOUT_CH3_9	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3 32 VOUT_CH2_10	M2 30 VOUT_CH2_8	M1 31 VOUT_CH2_9	M
N	N15 77 VOUT_CH3_10	N14 76 IOUT_CH3_1	N13 71	N12 68	N11 65	N10 61 R_GAIN_C	N9 58 R_GAIN_F	N8 54 AGND	N7 51 AVDD	N6 48 R_OFFSET_C	N5 45	N4 42 AVCC	N3 35	N2 33 IOUT_CH2_1	N1 34 IOUT_CH2_0	N
P	P15 75 IOUT_CH3_0	P14 74	P13 69	P12 66	P11 63 R_GAIN_A	P10 60 R_GAIN_D	P9 57 VEE	P8 55 DGND	P7 52 DVDD	P6 49 R_OFFSET_B	P5 46 R_MASTER	P4 43	P3 40	P2 38	P1 36	P
R	R15 73	R14 72	R13 70	R12 67 AVCC	R11 64	R10 62 R_GAIN_B	R9 59 R_GAIN_E	R8 56 VEE	R7 53 SGND	R6 50 R_OFFSET_A	R5 47 R_OFFSET_D	R4 44	R3 41	R2 39	R1 37	R

NOTE: Balls populating the inner 9x9 grid are for improved thermal dissipation. This middle grid of balls should be connected to the VEE plane or left floating. Order E6420BBG if populated middle is desired.

Circuit Description

Chip Overview

The Edge6420 provides 64 output levels (44 voltage and 20 current). These outputs can easily be configured to generate the specific analog voltage and current requirements for 4 channels of ATE pin electronics including:

- 3 level driver
- Window comparator
- Active load
- Per pin PMU

without requiring any scaling or shifting via external components.

The Edge6420 has the flexibility to be used in other configurations for other applications.

Programming of the chip is done using a 4 bit digital interface comprised of:

- Serial Data In
- Clock
- Update
- Chip Enable.

Grouping of DACs

DACs are separated into 4 channels of 6 distinct functional groups. Groups are defined by:

- Type (voltage or current output)
- Resolution (# of bits)
- Output range
- Output compliance.

Table 1 defines the DACs on a per channel basis:

Attribute	Group A	Group B	Group C	Group D	Group E	Group F
Total # of DACs in Group	5 per channel	2 per channel	2 per channel	2 per channel	2 per channel	3 per channel
Type	V	V	V	V	I	I
Resolution (# of bits)	13	13	13	13	13	6
Output Range: Max DAC Range (Note 1) Offset Range	11.5V -3.5V to 2.5V	11.5V -3.5V to 2.5V	17V -3.5V to 2.5V	11.5V -3.5V to 2.5V	3.6 mA –128 LSB (Note 2)	3.6 mA 0
Adjustable Output Offset	yes	yes	yes	yes	no	no
Compliance	±100 µA	±100 µA	±100 µA	±100 µA	–0.2 to AVDD – 2.2V (Note 3)	–0.2 to AVDD – 2.2V (Note 3)

Note 1: The max DAC range is achieved through specific AVCC, AVEE, and Gain resistor settings. See the equations in the "DAC Voltage Output Overview", "DAC Current Output Overview", and specifications for details.

Note 2: –128 LSB is equivalent to –128 * LSB, where LSB = Range / 2^{13}. For max range case of 3.6 mA, this offset would thus be: –56.26 µA of offset current at Code 0.

Note 3: Compliance specified in the table is at IOUT = 1.3mA. Maximum compliance is lower at higher currents. Please refer to specifications for compliance at other output currents.

Table 1. DAC Grouping

Circuit Description *(continued)*

DAC Voltage Output Overview

The output voltage of Group A, B, C, and D DACs is governed by the following equation:

$$V_{OUT\_[A:D]} = \left(K_{G[A:D]} * V_{REF} * \frac{R\_GAIN\_[A:D]}{R\_MASTER} * \frac{DATA}{8192}\right) + V_{OFFSET\_[A:D]}$$

Equation 1.

where:
DATA corresponds to the base-10 value of the binary data loaded into the shift register shown in Figure 2.

$K_{G[A:D]}$ is a multiplying factor that is fixed, as follows:

$K_{GA} = 4$ $K_{GB} = 4$
$K_{GC} = 8$ $K_{GD} = 4$

$V_{REF} = 2.5V$

Offset

The offset for each of the voltage DACs is governed by the following equation:

$$V_{OFFSET\_[A:D]} = K_{OFFSET} * V_{REF} * \left(0.5 - \left(\frac{R\_OFFSET\_[A:D]}{R\_MASTER}\right)\right)$$

Equation 2.

where:

$K_{OFFSET} = 2$

$V_{REF} = 2.5V$

External Resistors

The recommended resistor values for the above equations are as follows:

R_MASTER = 100KΩ (0.1% precision)

R_GAIN_[A:D] = (0.4 to 1.15) * R_MASTER

R_OFFSET_[A:D] = (0.0 to 1.2) * R_MASTER

Minimum / Maximum Output Voltages

See Table 2 for the minimum and maximum possible voltages of a voltage output.

DAC Setting MSB ... LSB	$V_{OUT\_[A:D]}$ (V)
0000H	$V_{OFFSET\_[A:D]}$
1FFFH	$V_{MAX\_[A:D]}$

Table 2. Minimum/Maximum Output Voltages

where:

$V_{OFFSET[A:D]}$ is defined in equation 2

and

$$V_{MAX\_[A:D]} = \left(K_{G[A:D]} * V_{REF} * \frac{R\_GAIN\_[A:D]}{R\_MASTER} * \frac{8191}{8192}\right) + V_{OFFSET\_[A:D]}$$

Equation 3.

The most negative voltage possible for the Edge6420 is –3.5V when VEE = –4.5V.

Resolution

The resolution of the DACs in Groups A, B, C, and D is:

$$V_{RANGE\_[A:D]} / 2^{13}$$

where $V_{RANGE\_[A:D]}$ is defined in Equation 4.

Range

The range of the DACs in Groups A, B, C and D is:

$$V_{RANGE\_[A:D]} = K_{G[A:D]} * V_{REF} * \frac{R\_GAIN\_[A:D]}{R\_MASTER} * \frac{8191}{8192}$$

Equation 4.

Circuit Description *(continued)*

Group A DACs

There are five Group A DACs/channel. Group A DACs have a centralized offset, gain and range that is independent of any other group.

Group A DACs are characterized by 13 bit resolution and their typical outputs are governed by the following equation:

$$V_{OUT\_A} = \left(10 * \frac{R\_GAIN\_A}{R\_MASTER} * \frac{DATA}{8192}\right) + V_{OFFSET\_A}$$

where:

$$V_{OFFSET\_A} = \left(5 * \left(.5 - \frac{R\_OFFSET\_A}{R\_MASTER}\right)\right)$$

Note: V_{REF} = 2.5V

Group B DACs

There are two Group B DACs/channel. Group B DACs have a centralized offset, gain and range that is independent of any other group.

Group B DACs are characterized by 13 bit resolution and their typical outputs are governed by the following equation:.

$$V_{OUT\_B} = \left(10 * \frac{R\_GAIN\_B}{R\_MASTER} * \frac{DATA}{8192}\right) + V_{OFFSET\_B}$$

where:

$$V_{OFFSET\_B} = \left(5 * \left(.5 - \frac{R\_OFFSET\_B}{R\_MASTER}\right)\right)$$

Note: V_{REF} = 2.5V

Group C DACs

There are two Group C DACs/channel. Group C DACs have a centralized offset, gain and range that is independent of any other group'.

Group C DACs are characterized by 13 bit resolution and their typical outputs are governed by the following equation:

$$V_{OUT\_C} = \left(20 * \frac{R\_GAIN\_C}{R\_MASTER} * \frac{DATA}{8192}\right) + V_{OFFSET\_C}$$

where:

$$V_{OFFSET\_C} = \left(5 * \left(.5 - \frac{R\_OFFSET\_C}{R\_MASTER}\right)\right)$$

Note: V_{REF} = 2.5V

Group D DACs

There are two Group D DACs/channel. Group D DACs have a centralized offset, gain and range that is independent of any other group.

Group D DACs are characterized by 13 bit resolution and their typical outputs are governed by the following equation:

$$V_{OUT\_D} = \left(10 * \frac{R\_GAIN\_D}{R\_MASTER} * \frac{DATA}{8192}\right) + V_{OFFSET\_D}$$

where:

$$V_{OFFSET\_D} = \left(5 * \left(.5 - \frac{R\_OFFSET\_D}{R\_MASTER}\right)\right)$$

Note: V_{REF} = 2.5V

DAC Current Output Overview

The output current of Group E and F DACs is governed by the following equation:

$$I_{OUT\_[E:F]} = \left(K_{G[E:F]} * I_{REF\_[E:F]} * \frac{DATA}{MAX\_COUNT\_[E:F]}\right) + I_{OFFSET\_[E:F]}$$

Equation 5.

where:

DATA corresponds to the base-10 value of the binary data loaded into the shift resister in Figure 2.

$$I_{REF\_[E:F]} = \frac{V_{REF}}{R\_GAIN\_[E:F]}$$

$K_{G[E:F]}$ is a multiplying factor that is fixed, as follows:

K_{GE} = 80 K_{GF} = 80

V_{REF} = 2.5V

MAX_COUNT_E = 8192
MAX_COUNT_F = 64

Circuit Description *(continued)*

Offset

The typical offset for each current DAC is governed by the following equations:

$$I_{OFFSET\_E} = -\frac{K_{GE} * V_{REF}}{R\_GAIN\_E} * \frac{128}{MAX\_COUNT\_E}$$

Equation 6.

$$I_{OFFSET\_F} = 0$$

Group E DACs

There are 2 Group E DACs/channel. Group E DACs are characterized by:

- Current outputs (current flows out of the chip)
- 13 bit resolution
- Fixed offset (–128 * LSB typical)
- Adjustable full scale range (but < 3.6 mA).

The output current equation for Group E DACs is:

$$I_{OUT\_E} = \left(\frac{DATA}{8192} * \frac{200}{R\_GAIN\_E}\right) - \frac{3.125}{R\_GAIN\_E}$$

where:

$$55\ k\Omega \leq R\_GAIN\_E \leq 156\ k\Omega$$

Note: $V_{REF} = 2.5V$

Group F DACs

There are 3 Group F DACs/channel. Group F DACs are characterized by:

- Current outputs (current flows out of the chip)
- 6 bit resolution
- Fixed offset (0 typical)
- Adjustable full scale range (but < 3.6 mA).

The output current equation for Group F DACs is:

$$I_{OUT\_F} = \frac{DATA}{64} * \frac{200}{R\_GAIN\_F}$$

where:

$$55\ k\Omega \leq R\_GAIN\_F \leq 156\ k\Omega$$

Note: $V_{REF} = 2.5V$

Circuit Description *(continued)*

Address Map

Address	Channel	Group	Type	Typical Uses
0 1 2 3 4	0 0 0 0 0	A A A A A	V V V V V	Driver & Comparator Levels
5 6	0 0	B B	V V	PPMU Comparator Thresholds
7 8	0 0	C C	V V	PPMU Force Voltage, Flash Programming Supervoltage
9 10	0 0	D D	V V	TBD TBD
11 12	0 0	E E	I I	Load Source and Sink Programming currents
13 14 15	0 0 0	F F F	I I I	Chip Bias, Rising/Falling Slew Rate Adjust
16-31	1	Same format as above for Channel 1.		
32-47	2	Same format as above for Channel 2.		
48-63	3	Same format as above for Channel 3.		
64	N/A	All	V/I	Parallel Load for all DACs
65-255	Not used (reserved for future upgradability).			

Circuit Description *(continued)*

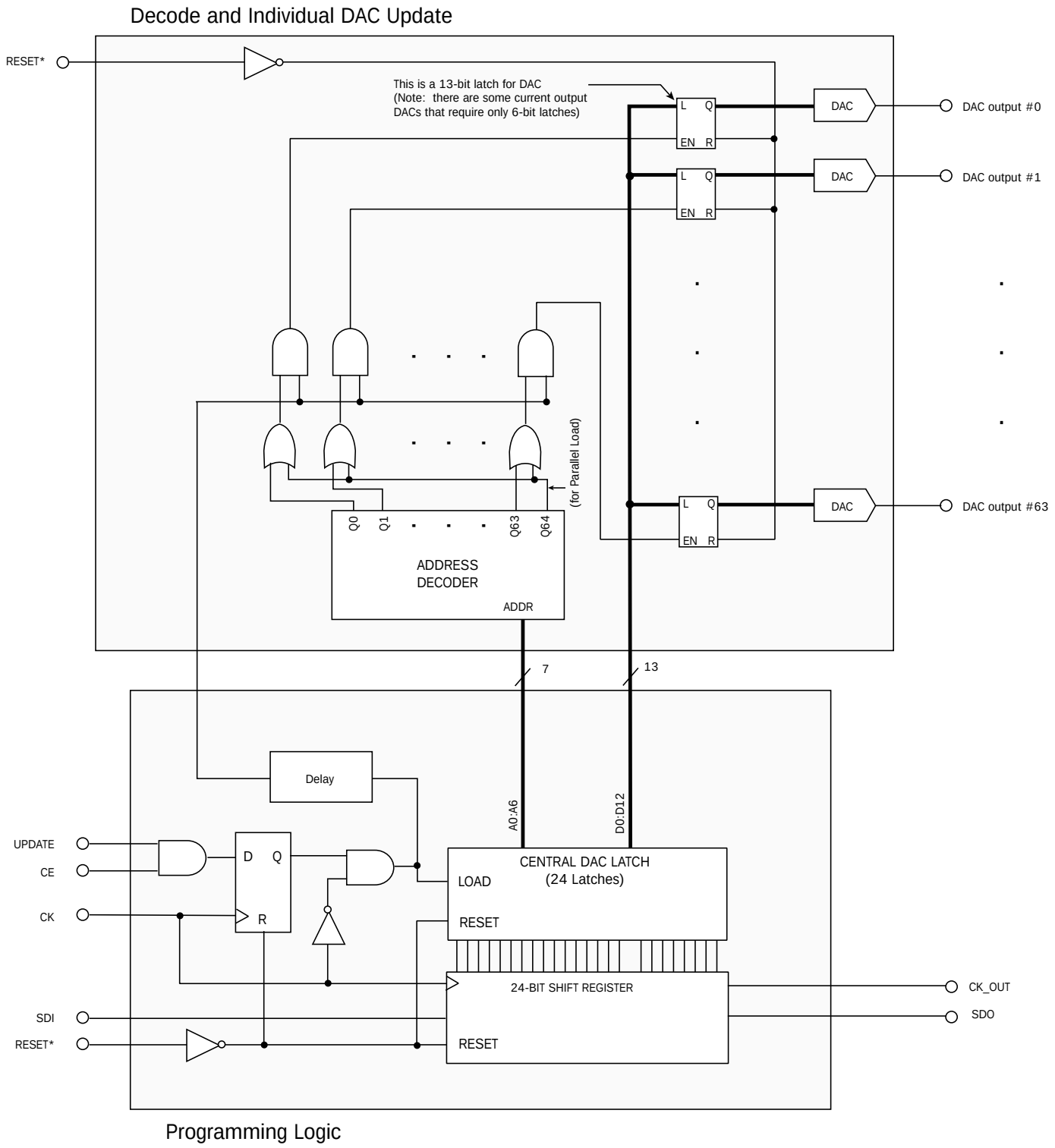


Figure 1. DAC Functionality Block Diagram

Circuit Description *(continued)*

Programming Sequence

The DACs are programmed serially (see Figures 1, 2a, 2b, and 3). On each rising edge of CK, SDI is loaded into a shift register. It requires 24 Clocks to fully load the shift register (8 address bits + 16 data bits).

For Groups A, B, C, D, and E DACs:

Address and data are loaded LSB first, MSB last. In a 24 clock sequence, A0, as shown in Figure 2a, is loaded into the shift register on the first CK rising edge, and D15 is loaded last on the 24th rising CK edge. Note that a 24th falling CK edge is required to transfer the data from the Central DAC Latch to the selected DAC latch (See Figure 1). See detailed Timing Diagrams in the "AC Characteristics" specifications section.

For Group F DACs:

The loading sequence is the same as Groups A-E, but Group F uses only 6 bits, and these bits must be programmed as shown in Figure 2b. 24 clock cycles are required for programming, with A0 loaded on the first rising CK edge, and D8 (as shown in Figure 2b) loaded on the 24th rising CK edge.

As is the case with other groups, a 24th falling edge of CK24 is required for proper programming of Group F DACs.

Chip Enable

CE is a synchronous input which determines whether the Central DAC latch shown in Figure 1 is loaded with data from the shift register. CE is also necessary to update a DAC. If CE is high, rising edges of CK load data from the shift register to an internal latch. If CE is low, central DAC latch updating is disabled.

CE	Central and Individual DAC Latch "Load" Status
low	Central and individual DAC latch loading is disabled
high	Central and individual DAC latches are loaded

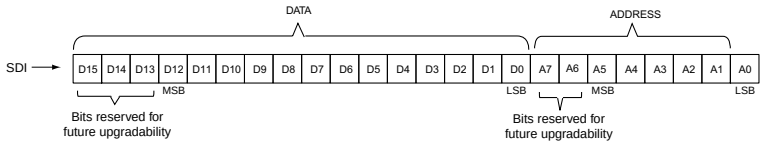


Figure 2a. Format of Address and Data in Shift Register for Group A, B, C, D, and E DACs (13-bits)

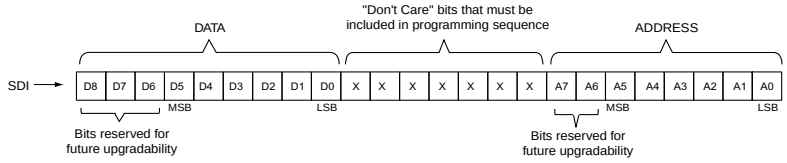


Figure 2b. Format of Address and Data in Shift Register for Group F DACs (6-bits)

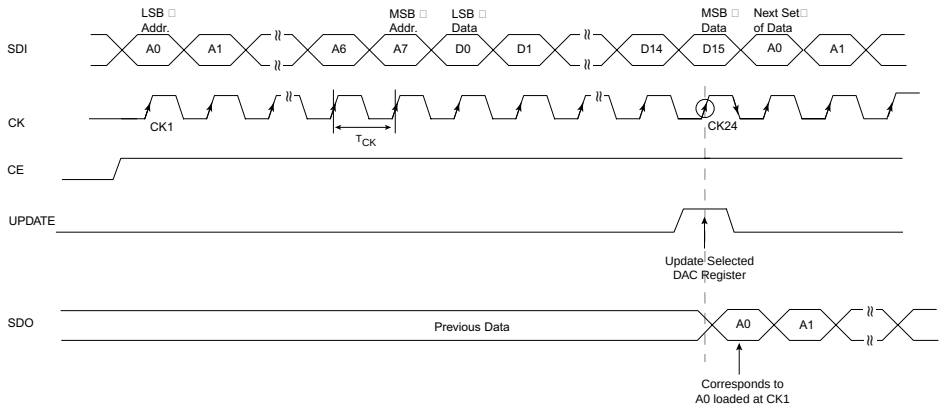


Figure 3. Serial Data Programming Sequence

Circuit Description *(continued)*

Digital Outputs

SDO is a CMOS output, swinging rail to rail between DVDD and DGND.

Chip Reset and Power Up

RESET* for the Edge6420 is active low.

When the Edge6420 first powers up, the latches will turn on to the same state as though RESET* had been asserted.

When RESET* is brought low, the latches, and therefore the DAC levels, will go to a known state that corresponds to a specific DATA code. See the "Application Information" section for an example of how this functionality works. The known states are:

GROUP	RESET* State (Code)
A	1000H
B	1000H
C	1000H
D	1000H
E	0000H
F	1000H

Care should be taken to ensure RESET* is invoked properly. It is critical to ensure that if a RESET* is asserted after UPDATE has transitioned from a high to low state, that RESET* stay low, at least 2 µs. To understand this precaution, notice in Figure 1 that UPDATE is delayed in order to enable individual DAC latches. If RESET* is not brought low for sufficient time, an individual DAC update will occur.

By simply forcing the RESET* pulse low for a minimum of 2 µs, when a CK frequency of 50 MHz or less is used, the 6420 will clear properly to the known states shown above.

Power Supply Sequence

Power supplies should be asserted in the following order:

1. VEE
2. AVDD
3. DVDD
4. AVCC

To avoid latchup and ensure a predictable power up, the above sequence should be followed.

Analog Scan Test Feature

Voltage Outputs

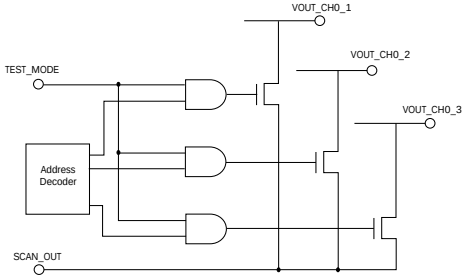
Each voltage output of the Edge6420 has high impedance FET(s) connected from the outputs to a common analog scan line.

The feature utilizes the normal address decoding, as shown on page 8, as well as a "high" level on the TEST_MODE pin (see truth table below).

TEST_MODE	SCAN STATE
0	Scan Off
1	Scan On

To test an output, a DAC should be loaded as shown by timing in Figure 3. The clock should be stopped after the falling edge of CK24 after UPDATE is unasserted. At this point, the SCAN_OUT pin, which is an analog output, will reflect the voltage at the addressed DAC's output pin.

Note that the scan output is switched off when the parallel load is selected (address 64). This prevents a parallel connection of all the DAC outputs when the scan feature is used.



NOTE: When address 64 is invoked (parallel load), scan is disabled.

Figure 5. Voltage Output Scan

Circuit Description *(continued)*

Current Outputs

The TEST_MODE and SCAN_OUT pins on the Edge6420 are used in the same way as for voltage outputs. The scan circuits for current outputs are shown in Figure 6.

The voltage measured at the SCAN_OUT pin, using the configuration in Figure 6, for Group E and F current outputs are as follows:

$$V_{SCAN\_OUT\_E} = (R_{SENSE\_E} + R_{PAD}) * I_{OUT\_E}$$

where:

$R_{SENSE\_E} = 400\Omega \pm 30\%$
$R_{PAD} = 30\Omega \pm 30\%$

and

$$V_{SCAN\_OUT\_F} = (R_{SENSE\_F} + R_{PAD}) * I_{OUT\_F}$$

where:

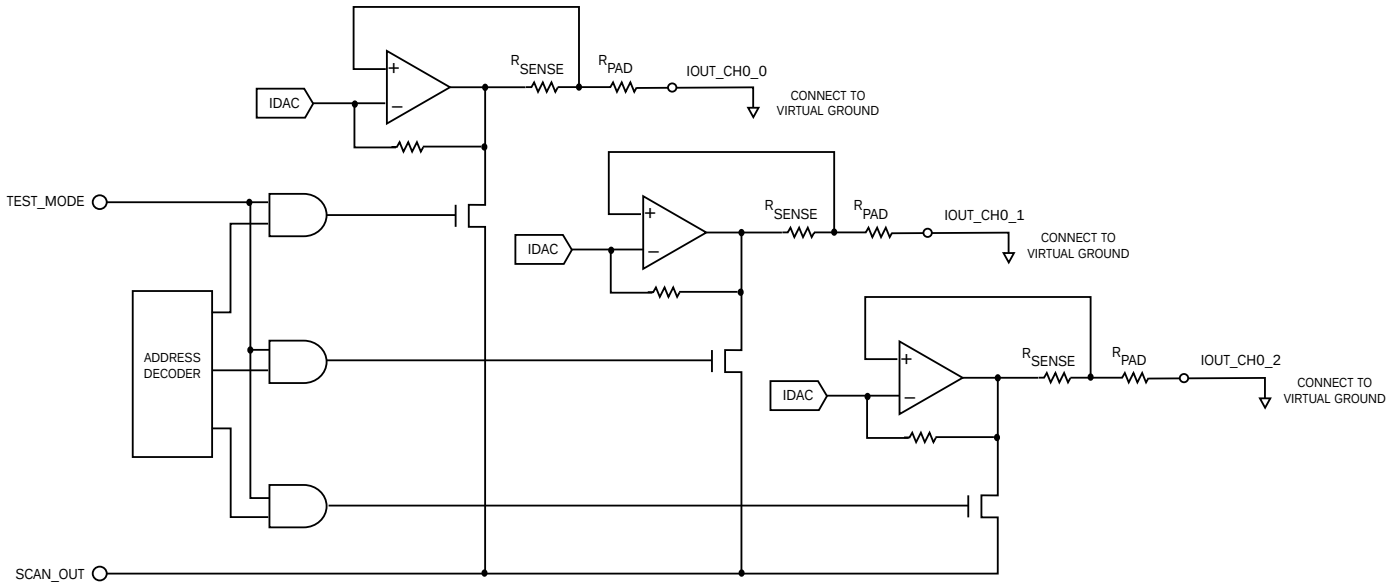
$R_{SENSE\_F} = 400\Omega \pm 30\%$
$R_{PAD} = 30\Omega \pm 30\%$

The typical "ON" resistance of the FET switch is 100 kΩ, but can varry from 60 kΩ to 180 kΩ as a function of process and output voltage.

Notes when Using SCAN Feature with Multiple Chips

When multiple 6420s are used on a board, and it is desired to gang the SCAN_OUT pins of these 6420s, or gang the TEST_MODE inputs to one point, it is required for proper functioning that the following rules be followed:

1) If TEST_MODE inputs are ganged together, SCAN_OUT cannot be ganged, or invalid results will be observed at the SCAN_OUT pin. Hence, each SCAN_OUT pin on a 6420 will have to be measured separately.
2) If SCAN_OUT is ganged, TEST_MODE pins cannot be ganged together.



NOTE: WHEN ADDRESS 64 IS INVOKED (PARALLEL LOAD), SCAN IS DISABLED.

Figure 6. Current Output Scan Circuits

Application Information

One application for the Edge6420 is to provide necessary DC voltages and currents for 4 channels of pin electronics (driver, receiver, load) and per pin measurement units.

For example, using the:

- Edge720 Load / Driver / Comparator
- Edge4707 PPMU

with the following specifications:

Edge720

- –1.5 < driver output high < +7.5V
- –1.5 < driver output low < +7.5V
- –1.5 < comparator threshold high < +7.5V
- –1.5 < comparator threshold low < +7.5V
- –1.5 < commutating voltage < 7.5V
- 0 < load source current < 24 mA
- 0 < load sink current < 24 mA

Edge 4707 PPMU

- –2.8 < PPMU (MI) compare high voltage < +2.8V
- –2.8 < PPMU (MI) compare low voltage < +2.8V
- –3.0 < PPMU (FV) < +14.0V

Other

- 0 < flash programming voltage (VHH) < +14V

Table 8 demonstrates Edge6420 settings that can be used to fulfill the above requirements.

Power Supplies (for this application):

15.25 ≤ AVCC ≤ 15.75V
–4.75V ≤ VEE ≤ –4.25V
4.6V ≤ AVDD ≤ 5.25V
4.85 ≤ DVDD ≤ 5.15V
AGND = 0, SGND = 0

Channel 0 Address	Group	Type	# Bits	Resolution	Offset	Resulting Range	Output Compliance	Power on Reset (DAC Code)	Suggested Application
0 1 2 3 4	A	V	13	1.10 mV	–1.5V	–1.5 / +7.5V	±100 µA	1000H (3V)	VIH VIL VOH VOL VCOM1
5 6	B	V	13	0.684 mV	–2.8V	–2.8 / 2.8V	±100 µA	1000H (0V)	PPMU CH PPMU CL
7 8	C	V	13	2.07 mV	–3.0V	–3.0 / +14.0V	±100 µA	1000H (6V)	PPMU FV VHH
9 10	D	V	13	1.10 mV	–1.5V	–1.5 / +7.5V	±100 µA	1000H (3V)	VCOM2 TBD
11 12	E	I	13	159 nA	N/A	0 to 1.3 mA	–.2 / 2.4V (Note 1)	0000H (0 mA)	ISC_IN ISK_IN
13 14 15	F	I	6	39 µA	N/A	0 to 2.5 mA	–.2 / 2.1V (Note 1)	1000H (1.0 mA)	RADJ FADJ IBIAS
16 – 31	Same as above for Channel 1.								
32 – 47	Same as above for Channel 2.								
48 – 63	Same as above for Channel 3.								

Note 1: Max compliance depends on maximum current required. See specifications for limits.

Table 8. Application Chart – Possible Chip Specification

Application Information *(continued)*

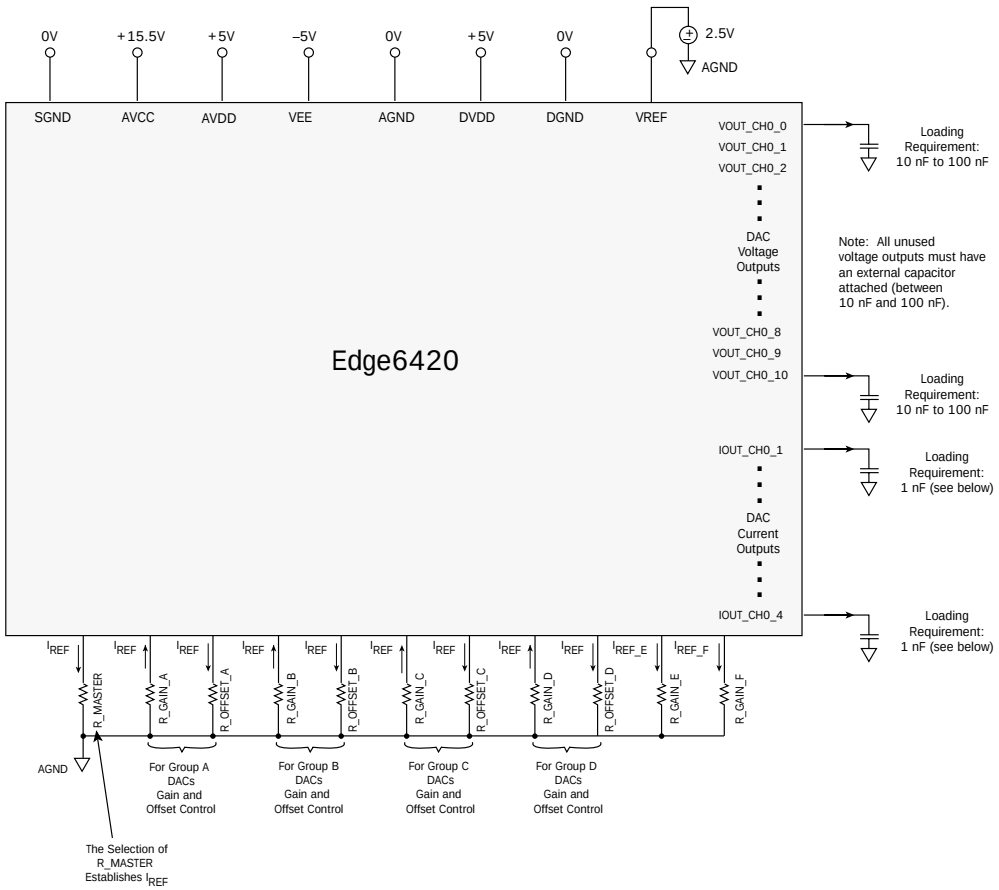


Figure 7. Required External Resistors and Components

Loading Requirements

Voltage Outputs

All voltage outputs (denoted VOUT_CH[0:3]_[0:10]) require a load capacitance between 10 nF and 100 nF for stability.

Current Outputs

All current outputs require capacitive loading; the amount of loading needed to ensure stability is dependent on the impedance that the current outputs of the 6420 drive. For impedances of 1.3 KΩ to 1.6 KΩ, such as what is seen at the E720 current inputs (ISK, ISRC, IBIAS, RADJ, and FADJ), it is recommended that 1 nF be used.

Caution on Exceeding Compliance Limits on Current Output DACs

Current output DACs (i.e., Group E and F DACs) can exhibit a “lock-up” condition in situations when the actual voltage seen at the outputs of these DACs exceeds the compliance limits in the specification. Care should be taken in the design of circuits being driven by Group E and F outputs to ensure compliance limits stated in the specifications are not exceeded.

Application Information *(continued)*

Temperature Coefficient Effect on DACs

There is a gain and offset temperature coefficient that should be taken into account in the system design that will affect calibration and performance.

The equation for voltage drift on output DACs is as follows:

$$\Delta V_{OUT\_A,B,C,D} = \Delta T * \left[TC_{OFFSET\_A,B,C,D} \left(\frac{\mu V}{^\circ C} \right) + CODE * LSB * TC_{GAIN\_A,B,C,D} (\%/^\circ C) \right]$$

Current outputs drift follow the following equation:

$$\Delta I_{OUT\_E,F} = \Delta T * \left[TC_{OFFSET\_E,F} \left(\frac{\mu A}{^\circ C} \right) + CODE * LSB * TC_{GAIN\_E,F} (\%/^\circ C) \right]$$

Average values for TC_{OFFSET} and TC_{GAIN} can be found in the specifications.

Compliance of Current Output DACs (Groups E, F)

The compliance of the current output DACs (Groups E and F) is governed by the following two equations:

$I_{OUT} < 2.5$ mA:

$$V_{COMPLIANCE} = (-250\ \Omega * I_{OUT}) + AVDD - 1.875V$$

$I_{OUT} \geq 2.5$ mA:

$$V_{COMPLIANCE} = (-600\ \Omega * I_{OUT}) + AVDD - 1V$$

See Figure 8 for a graphical depiction.

Note: I_{OUT} is current sourced from output of DAC.

Care should be taken to ensure that devices being driven by Group E and F DACs are designed to be within the compliance specification.

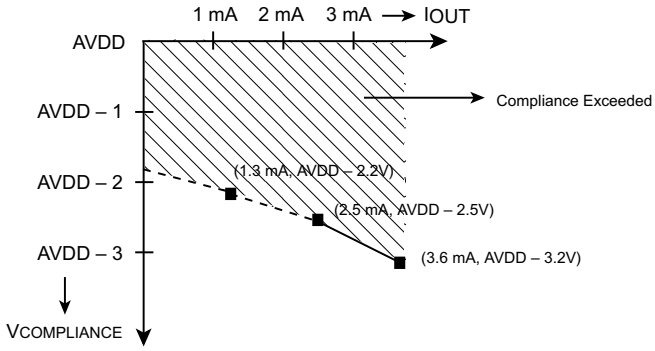


Figure 8. Compliance of Current Output DACs (Groups E and F)

Caution Regarding Power Dissipation of the 6420 During Parallel Load:

The Voltage DAC output amplifiers, for a FAST process, can:

- Source up to 10 mA (8 mA @ TJ = 100˚C)
- Sink up to 4.5 mA (3.5 mA @ TJ = 100˚C)

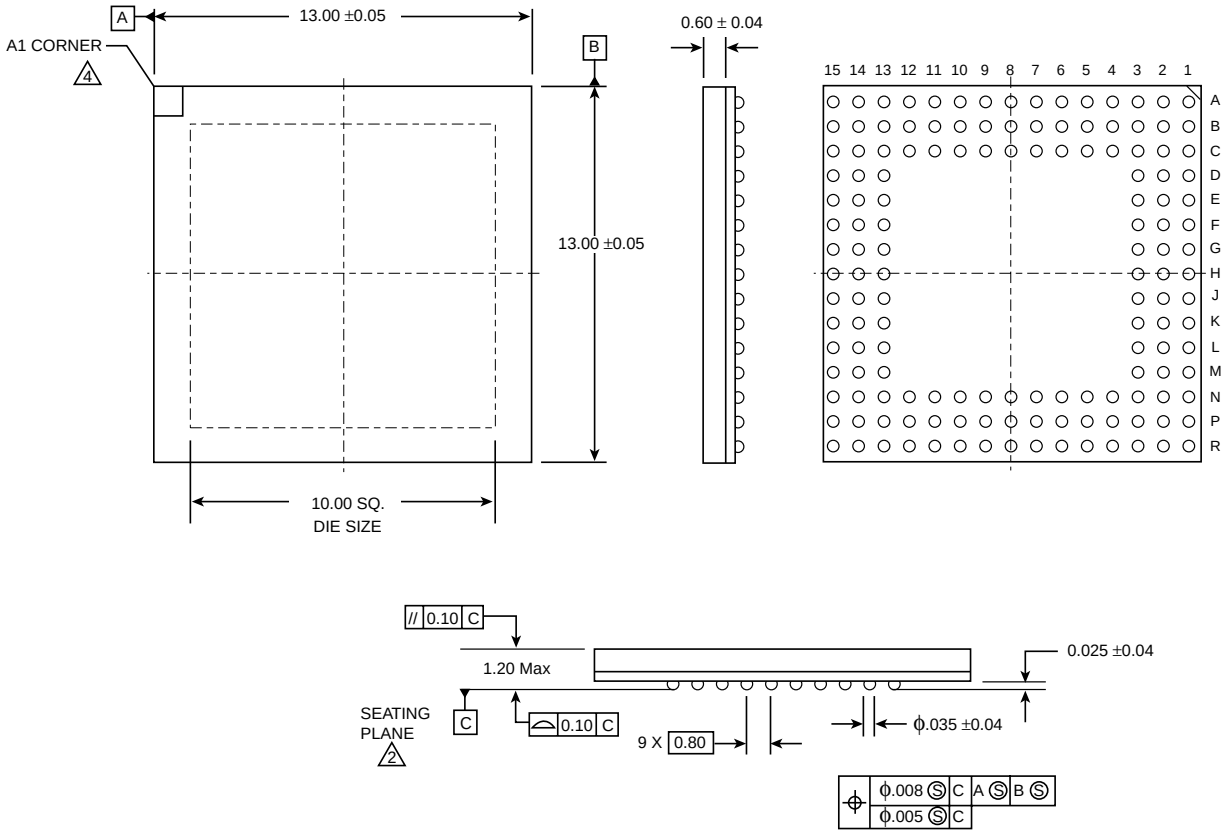
Caution must be taken during a parallel load, particularly when the voltage DACs are loaded with a large filtering capacitor (10 to 100 nF). In this scenario, a large voltage change can induce a large current peak. For example, the currents calculated below can be induced in the VCC/VEE supplies:

- Source case:
  44 DACs * 10 mA / DAC + 40 mA = 480 mA
  (or 400 mA @ TJ = 100˚C) in the VCC supply
- Sink case:
  44 DACs * 4.5 mA / DAC + 120 mA = 320 mA
  (or 280 mA @ TJ = 100˚C) in the VEE supply

Therefore, the user must take care of extra power dissipation due to these currents peaks, and should avoid large voltage changes during a parallel load.

Package Information

Edge6420ABG Package

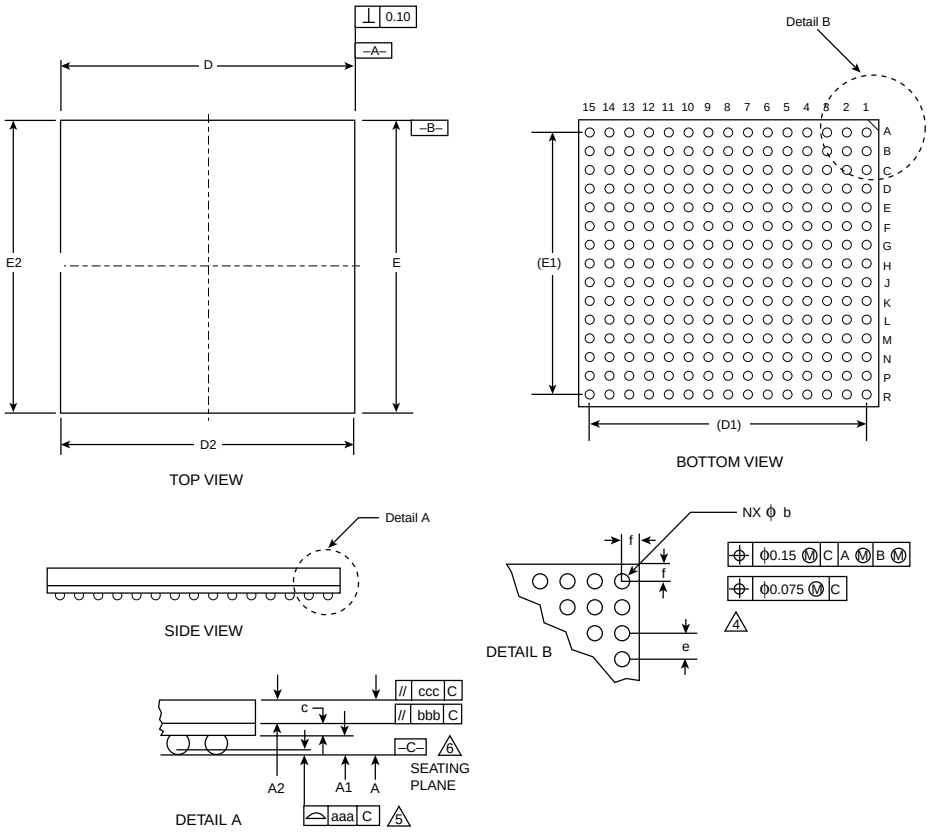


NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5K-1982.
2. Primary datum –C– and seating plane are defined by the high points of the solder balls.
3. f0.30 mm.
4. A1 corner defined by marking on the top package.

Package Information *(continued)*

Edge6420BBG Package



NOTE: The inner 9x9 balls are for improved thermal dissipation. They will be at the VEE potential, so board layout should ensure that these inner balls are connected to the VEE plane.

DIMENSIONAL REFERENCES			
REF	**MIN**	**NOM**	**MAX**
A	0.96	1.06	1.16
A1	0.21	0.26	0.31
A2	0.50	0.55	0.60
D1		11.20 BSC	
D2	12.90	13.00	13.10
E	12.90	13.00	13.10
E1		11.20 BSC	
E2	12.90	13.00	13.10
b	0.40	0.45	0.55
c		0.25	
aaa			0.12
bbb			0.20
ccc			0.20
e		0.8	
f	0.80	0.90	1.00
M		15	
N		225	

NOTES:
1. All dimensions are in millimeters.
2. ‘e’ represents the basic solder ball grid pitch.
3. “M” represents the basic solder ball matrix size, and symbol “N” is the number of balls after depopulating.
4. ‘b’ is measurable at the maximum solder ball dimaeter after reflow parallel to primary datum –C–.
5. Dimension ‘aaa’ is measured parallel to primary datum –C–.
6. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be matte finish charmilles 24 to 27.
8. Package centering to substrate shall be 0.0780 mm maximum for both X and Y directions respectively.
9. Package warp shall be 0.050 mm maximum.
10. Substrate material base is BT resin.
11. The overall package thickness “A” already considers collapse balls.
12. Dimensioning and tolerancing per ASME Y14.5M 1994.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply	AVCC	+15.25	+15.5	+15.75	V
Positive Analog Power Supply 2	AVDD	+4.6	+5	+5.25	V
Negative Power Supply	VEE	–5.25	–5	–4.3	V
Reference Voltage (Note 2)	VREF		2.500		V
Supply Ground (Note 1)	SGND	–.25	0	+.25	V
Total Analog Supply 1	AVCC – VEE		20.5	+23	V
Digital Power Supply	DVDD – DGND	3.00	5.0	5.50	V
Digital Ground (Note 1)	DGND	–.25	0	+.25	V
Thermal Resistance of Package (6420BBG) (measured at top-center of package)	θjc		3		°C/W
Case Temperature (at top of package)	T_{CASE}	40		80	°C

All Power Supply voltages are referred to AGND, the reference signal ground, unless othewise specified.

Note 1: Not production tested.
Note 2: User should use a precision supply for VREF setting because the offset and gain of all DACs will change proportionately to a deviation from VREF = 2.500V. See Equations 1 and 5 to determine the extent of offset and gain change to deviations in VREF.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Positive Analog Supply	AVCC	–.35	+20	V
Positive Analog Supply 2	AVDD	–.35	+5.5	V
Negative Analog Supply	VEE	–5.5	+.35	V
Digital Power Supply	DVDD – DGND	–.35	+5.5	V
Total Power Supply	AVCC – VEE	–.35	+25	V
	AVCC – AVDD	–5.5	+20	V
	DGND	–.35	+.35	V
	SGND	–.35	+.35	V
Digital Input Voltages	CE, CK, UPDATE, RESET*, SDI, TEST_MODE	DGND – .35	DVDD + .35	V
Analog Input Voltages	V_{REF}, V_{MASTER}, $V_{OFFSET\_[A:D]}$, $V_{GAIN\_[E:F]}$	AGND – .35	AVDD + .35	V
	$V_{GAIN\_[A:D]}$	AVEE – .35	AGND + .35	V
Analog Input Currents	$I_{GAIN\_[E:F]}$	–1	+1	mA
	I_{MASTER}	–1	+1	mA
Analog Output Voltages				
Groups A, B, C, D	VOUT_[A:D]	AVEE – .35	AVCC + .35	V
Groups E, F	VOUT_[E:F]	AGND – .35	AVDD + .35	V
Analog Output Currents				
Groups A, B, C, D Continuous DC Current	IOUT_[A:D]	–300	+300	µA
Output Voltage Compliance (Groups E, F) (Note 1)			3.3	V
Minimum Time Required Between Successive Parallel Loads of all 64 DACs @ C_{LOAD} = 100 nF, Full Scale Steps (Note 2)	Tmin	2		ms
Storage Temperature	TS	–65	+150	˚C
Junction Temperature	TJ		+125	˚C
Soldering Temperature (5 seconds, .25" from the pin)	TSOL		+260	˚C

All Power Supply voltages are referred to AGND, the reference signal ground, unless othewise specified.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Note 1: Exceeding this limit may result in a monostable output state at maximum current.
Note 2: Full scale step definition: 11.5V step for Group A, B, D DACs, 20V step for Group C, 3.6 mA steps for Groups E and F.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs (SDI, CE, CK, UPDATE, RESET*, TEST_MODE)					
Input Low Voltage	VIL			.8	V
Input High Voltage	VIH	2.4			V
Input Current	IIL, IIH	–1		1	µA
Digital Outputs (SD0, CK_OUT)					
Output Low Voltage @ I_{OL} = 1.6 mA	VOL			.4	V
Output High Voltage @ I_{OH} = –0.4 mA	VOH	2.4		DVDD	V
DAC Outputs					
Groups A, B, D (Voltage Outputs) Resolution			13		Bits
Max Output Voltage Range	VOUT_RANGE				
@ R_GAIN / R_MASTER = .4			4		V
@ R_GAIN / R_MASTER = 1		9.8	10	10.2	V
@ R_GAIN / R_MASTER = 1.15			11.5		V
Output Offset Range (DATA = 0000H)	V_{OFFSET}				
@ R_OFFSET / R_MASTER = 0.0			2.5		V
@ R_OFFSET / R_MASTER = 0.5			0		V
@ R_OFFSET / R_MASTER = 1.0		–2.60	–2.5	–2.35	V
@ R_OFFSET / R_MASTER = 1.2			–3.5		V
Output Current Compliance		–100		+100	µA
Headroom of Voltage Outputs (while maintaining current compliance limit) (Note 1)					
VOUT(max) to VCC	AVCC – VOUT(max)	1.25			V
VOUT(min) to VEE	VOUT(min) – VEE	1.00			V
Integral Linearity Error with 9 Point Calibration (Note 2)				±2	LSB
Integral Linearity Error with 2 Point Calibration (Note 4)				±15	LSB
Differential Linearity Error				< ±1	LSB
Gain TempCo (Notes 3, 6)	$TC_{GAIN\_A,B,D}$		–.00285		%/°C
Offset TempCo (Notes 3, 6)	$TC_{OFFSET\_A,B,D}$				
@ R_OFFSET / R_MASTER = 0.0			–288		µV/°C
@ R_OFFSET / R_MASTER = 0.5			–110		µV/°C
@ R_OFFSET / R_MASTER = 1.0			+145		µV/°C
@ R_OFFSET / R_MASTER = 1.2			+231		µV/°C

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Group C (Voltage Outputs)					
Resolution			13		Bits
Max Output Voltage Range (DATA = IFFFH)	VOUT_RANGE				
@ R_GAIN / R_MASTER = .4			8		V
@ R_GAIN / R_MASTER = .6			12		V
@ R_GAIN / R_MASTER = .85		16.75	17	17.22	V
Output Offset Range (DATA = 0000H)	V_{OFFSET}				
@ R_OFFSET / R_MASTER = 0.0			2.5		V
@ R_OFFSET / R_MASTER = 0.5			0		V
@ R_OFFSET / R_MASTER = 1.1		–3.10	–3.0	–2.9	V
@ R_OFFSET / R_MASTER = 1.2			–3.5		V
Output Current Compliance		–100		+100	µA
Headroom of Voltage Outputs – Group C (while maintaining current compliance limit) (Note 1)					
VOUT(max) to VCC	AVCC – VOUT(max)	1.25			V
VOUT(min) to VEE	VOUT(min) – VEE	1.00			V
Integral Linearity Error with 9 Point Calibration (Note 2)				±3	LSB
Integral Linearity Error with 2 Point Calibration (Note 4)				±20	LSB
Differential Linearity Error				< ±1	LSB
Gain TempCo (Notes 3, 6)	TC_{GAIN_C}		–.0012		%/°C
Offset TempCo (Notes 3, 6)	TC_{OFFSET_C}				
@ R_OFFSET / R_MASTER = 0.0			–250		µV/°C
@ R_OFFSET / R_MASTER = 0.5			–77		µV/°C
@ R_OFFSET / R_MASTER = 1.1			+240		µV/°C
@ R_OFFSET / R_MASTER = 1.2			+166		µV/°C

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Group E (Current Outputs) Resolution			13		Bits
Max Output Current Range	IOUT				
@ R_GAIN_E = 55 kΩ			3.6		mA
@ R_GAIN_E = 62.5 kΩ		3.09	3.2	3.35	mA
@ R_GAIN_E = 156 kΩ			1.28		mA
Output Voltage Compliance (Notes 1, 6)					
@ 1.3 mA		–0.20		AVDD – 2.20	V
@ 2.5 mA		–0.20		AVDD – 2.50	V
@ 3.2 mA		–0.20		AVDD – 2.92	V
@ 3.6 mA		–0.20		AVDD – 3.20	V
Integral Linearity Error with 9 point Calibration (Note 2)				±2	LSB
Integral Linearity Error with 2 point Calibration (Note 4)				±15	LSB
Differential Linearity Error				< ±1	LSB
Current Offset		(–128 * LSB) – 20	–128 * LSB	(–128 * LSB) + 20	µA
Gain TempCo (Notes 3, 6)	TC_{GAIN_E}		–.0021		%/˚C
Offset TempCo (Notes 3, 6)	TC_{OFFSET_E}		±100		nA/˚C
Group F (Current Outputs) Resolution			6		Bits
Max Output Current Range	IOUT				
@ R_GAIN_F = 55 KΩ			3.54		mA
@ R_GAIN_F = 62.5 KΩ		3.09	3.15	3.35	mA
@ R_GAIN_F = 156 KΩ			1.26		mA
Output Voltage Compliance (Notes 1, 6)					
@ 1.3 mA		– 0.20		AVDD – 2.20	V
@ 2.5 mA		– 0.20		AVDD – 2.50	V
@ 3.15 mA		– 0.20		AVDD – 2.89	V
@ 3.6 mA		–0.20		AVDD – 3.20	V
Integral Linearity Error with 2 Point Calibration (Note 5)				±0.25	LSB
Differential Linearity Error				< ±1	LSB
Current Offset		–20	0	20	µA
Gain TempCo (Notes 3, 6)	TC_{GAIN_F}		–.0057		%/˚C
Offset TempCo (Notes 3, 6)	TC_{OFFSET_F}		±23		nA/˚C

DC Characteristics *(continued)*

Power Supplies

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Consumption					
Positive Analog Supply 1 (Note 6)	ICC		20.5	41.5	mA
Positive Analog Supply 2 (Note 6)	IADD		60	132	mA
Digital Supply (Note 6)	IDDD		2	10	mA
Negative Power Supply 1 (Note 6)	IEE		–73	–118	mA
Reference Supply	IREF		0.2	1.4	mA
Power Supply Rejection Ratio (Note 1)	PSRR				
5 MHz			65		dB
1 MHz			45		dB
100 KHz			50		dB
Power Supply – DC Sensitivity (Note 1)	ΔVOUT/ ΔAVDD		40		dB

All specifications are guaranteed over Recommended Operating Conditions unless otherwise noted.
DC Test Conditions (unless otherwise specified): VREF = 2.50V.

Note 1: Not production tested. Guaranteed by bench characterization.
Note 2: The 9 calibration points recommended are:
DATA values of 0000H, 03FFH, 07FFH, 0BFFH, OFFFH, 13FFH, 17FFH, 1BFFH, 1FFFH.
Note 3: Assuming R_MASTER = 100 KΩ, stable VREF, nominal external resistor values, and stable supply voltage values.
Note 4: Calibration points are: Data values of 0000H and 1FFFH.
Note 5: Calibration points are: Data values of OOOOH and OO3FH.
Note 6: See “Applications Information” for further information.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Set Up Times (Note 1)					
SDI to Rising CK	T_{SU_SDI}	10			ns
CE (rising edge) to Rising CK24	T_{SU_CE}	10			ns
UPDATE (rising edge) to Rising CK24 (Notes 2, 3)	T_{SU_UPDT}	5		70% of T_{CK}	ns
Hold Times (Note 1)					
SDI to Rising CK	T_{HLD_SDI}	10			ns
CE (falling edge) to Rising CK24	T_{HLD_CE}	10			ns
UPDATE (falling edge) to Rising CK24 (Notes 2, 3)	T_{HLD_UPDT}	5		70% of T_{CK}	ns
CK					
Fmax at DVDD = 3.3V ± .30V (Notes 1,5)	F_{max}				
30 to 50% Duty Cycle (Note 5)		33			MHz
70% Duty Cycle		20			MHz
Fmax at DVDD = 5.0V ± .50 (Notes 4,5)	F_{max}				
30 to 50% Duty Cycle		55			MHz
70% Duty Cycle		35			MHz
Duty Cycle (Note 1)	PW_{CK}	30	50	70	%
RESET Pulse Width	PW_{RESET}	2			µs
Output Voltage Settling Time (Note 1) (from CK Ø corresponding to UPDATE)					
Full Scale Step, 10V (to 0.025% FSR)					
for Groups A, B, D	Ts				
Load: 10 nF			30	70	µs
Load: 100 nF			250	700	µs
Full Scale Step, 17V (to 0.025% FSR)					
for Group C					
Load: 10 nF			50	150	µs
Load: 100 nF			410	1	ms
Output Current Settling Time					
Group E (to .025%)					
Load: 1 nF			53	100	µs
Load: 10 nF			230	500	µs
Group F (to .8%)					
Load: 1 nF			4.4	10	µs
Load: 10 nF			29	50	µs

Test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: Not production tested. Guaranteed by design and characterization.

Note 2: The max spec of 70% of T_{CK} is not production tested.

Note 3: CK24 refers to 24th rising clock edge, which corresponds to a full shift register. Note that a falling CK24 edge is also required for proper operation of circuit.

Note 4: The 6420 is production tested at 55 MHz only, with 50% duty cycle.

Note 5: Duty cycle % shown refers to "high" duration of clock in a period.

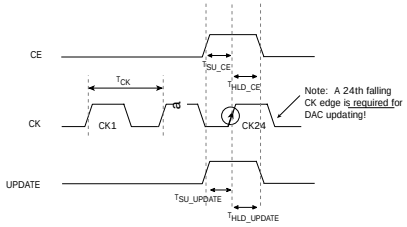


Figure 9. Central and Individual DAC Updating

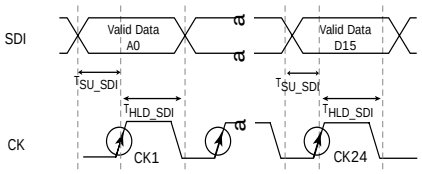


Figure 8. Shift Register Loading Timing Diagram

Ordering Information

Model Number	Package
E6420ABG	144 Ball, 13 mm x 13 mm BGA
E6420BBG	225 Ball, 13 mm x 13 mm BGA
6420EVM	Edge6420 Evaluation Board

Contact Information

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Revision History

Current Revision: September 25, 2001
Previous Revision: August 3, 2001

Page #	Section Name	Previous Revision	Current Revision
16	Application Information	Caution Regarding Power Dissipation of the 6420 During Parallel Load	Reword entire section
19	Recommended Operating Conditions	Negative Power Supply1 Analog Ground 2 (Notes 1, 3)	*Delete:* (referred to AGND) from all specs Negative Power Supply Supply Ground (Note 1) *Delete:* Analog Ground Notes: Delete Note 2, 3, Note 4 becomes new Note 2 *Add:* "All Power Supply voltages ..." at beginning of notes
20	Ab Max Ratings	Positive Analog Supply 2 Digital Power Supply, Sym: DVDD Total Power Supply DGND – AGNE, SGND – AGND	Min: –.35 Digital Power Supply, Sym: DVDD – DGND Total Power Supply DGND, SGND *Delete:* AVDD – AGND and VEE – AGND specs *Add:* "All Power Supply voltages ..." at beginning of notes
21	DC Characteristics	Max Output Voltage Range @ R_GAIN/R_MASTER = 1, Min: 9.86, Max: 10.14 Output Offset Range @ R_OFFSET/R_MASTER = 1.0, Min: –2.6, Max: –2.4 Gain TempCo, Typ: –.000285 Offset TempCo @ VOFFSET = 2.5V @ VOFFSET = 0, Typ: –72 @ VOFFSET = –2.5V @ VOFFSET = –3.5V	Max Output Voltage Range @ R_GAIN/R_MASTER = 1, Min: 9.8, Max: 10.2 Output Offset Range @ R_OFFSET/R_MASTER = 1.0, Min: –2.60, Max: –2.35 Gain TempCo, Typ: –.00285 Offset TempCo @ R_OFFSET / R_MASTER = 0.0 R_OFFSET / R_MASTER = 0.5, Typ: –110 @ R_OFFSET / R_MASTER = 1.0 @ R_OFFSET / R_MASTER = 1.2
22	DC Characteristics	Output Offset Range @ R_OFFSET/R_MASTER = 1.1, Min: –3.05, Max: –2.95 Gain TempCo, Typ: –.000447 Offset TempCo @ VOFFSET = 2.5V @ VOFFSET = 0 @ VOFFSET = –3.0V, Typ: +132 @ VOFFSET = –3.5V	Output Offset Range @ R_OFFSET/R_MASTER = 1.1, Min: –3.10, Max: –2.9 Gain TempCo, Typ: –.0012 Offset TempCo @ R_OFFSET / R_MASTER = 0.0 @ R_OFFSET / R_MASTER = 0.5 @ R_OFFSET / R_MATER = 1.1, Typ: +240 @ R_OFFSET / R_MASTER = 1.2
23	DC Characteristics	Group E Max Output Current Range @ R_GAIN_# = 62.5, Min: 3.14, Max: 3.32 Output Voltage Compliance 3.6 mA, Min: –0.29 Gain TempCo, Typ: –.00129 Group F Output Voltage Compliance Integral Linearity Error, Max: ±2 Gain TempCo, Typ: –.00129 Offset TempCo, Typ: +23	Max Output Current Range @ R_GAIN_# = 62.5, Min: 3.09 Max: 3.35 Output Voltage Compliance: Add: @ 3.2 mA 3.6 mA, Min: –0.20 Gain TempCo, Typ: –.0021 Group F Output Voltage Compliance: *Add:* 3.15 mA Integral Linearity Error, Max: ±0.25 Gain TempCo, Typ: –.0057 Offset TempCo, Typ: ±23
24	DC Characteristics	Positive Analog Supply2, Digital Supply Negative Power Supply, Min: 73, Max: 118 Note 4: ... and IFFFH	Add Note 6 Negative Power Supply, Min: –73, Max: –118 Note 4: ... and 1FFFH
25	AC Characteristics	Fmax at DVDD	Add Note 5

Revision History

Current Revision: August 3, 2001
Previous Revision: June 28, 2001

Page #	Section Name	Previous Revision	Current Revision
	All	Target	Preliminary
7	DAC Current Output Overview & Offset		*Add:* Equation numbers
8	Offset	The offset for each current ...	The typical offset for each current ...
14	Table 8	Channels 11, 12 Resolution: 0.159 nA	Channels 11, 12 Resolution: 159 nA *Delete:* Note 2
15	Application Information	 Current Outputs, last sentence: ... it is recommended that 100 pF be used.	change 100 pF to 1 nF ... it is recommended that 1 nF be used.
16	Temperature Coefficient Effect on DACs		Add: Last paragraph, "Contact Semtech for a summary of equations to derive TC_{OFFSET} and TC_{GAIN}.
17	6420ABG Package	Note 3	*Delete:* all but "f0.30 mm"
19	Recommended Operating Conditions	 Reference Voltage, Min: 2.475, Typ: 2.50000, Max: 2.525 Digital Power Supply, Min: 4.85, Max: 5.15 Thermal Resistance of Package, Typ: TBD, Units: ˚C	*Delete:* Notes 1 & 2 *Add:* New Notes 1 and 4, renumber remaining notes Reference Voltage, Typ: 2.500, delete Min & Max values Digital Power Supply, Min: 3.00, Max: 5.50 Thermal Resistance of Package (measured at top-center of package), Typ: 3, Units: ˚C/W
20	Ab Max Ratings	Digital Input Voltages	*Add:* "SDI, TEST_MODE" to Symbols
21	DC Characteristics	Gain TempCo, Typ: –.0012 Offset Tempco, Typ: –200, 0, +236, +324	Gain TempCo (Notes 3, 6), Typ: –.000285 Offset Tempco, Typ: –288, –72, +145, +231
22	DC Characteristics	Integral Linearity Error with 2 Point Calibration, Max: ±2 Gain TempCo, Typ: –.0015 Offset TempCo, Typ: –200, 0, TBD, +325	Integral Linearity Error with 2 Point Calibration, Max: ±3 Gain TempCo (Notes 3, 6), Typ: –.000447 Offset TempCo, Typ: –250, –77, +132, +166
23	DC Characteristics	Group E Gain TempCo, Typ: –.0018 Offset TempCo, Typ: TBD, Group F Gain Tempco Offset TempCo, Typ: TBD	Groups E Gain TempCo (Notes 3, 6), Typ: –.00129 Offset TempCo, Typ: ±100 Group F Gain Tempco (Notes 3, 6) Offset TempCo, Typ: ±23
24	DC Charcteristics	Digital Supply, Typ: TBD, Max: TBD Power Supply Rejection Ratio 1 MHz, Typ: TBD 500 kHz, Typ: TBD 100 kHz, Typ: TBD	Digital Supply, Typ: 2, Max: 10 Power Supply Rejection Ratio 5 MHz, Typ: –65 1 MHz, Typ: –45 100 kHz, Typ: –50 *Add:* Power Supply – DC Sensitivity
24	DC Charcteristics (Notes)	VREF = 2.50000V	VREF = 2.50V
25	AC Characteristics	Fmax at DVDD = 3.3V (Note 4) Fmax at DVDD = 5.0V (Note 1) Full Scale Step, 0 to 10V Load: 10 nF, Max: TBD, Load: 100 nF, Max: TBD, Units: ms Full Scale Step, 0 to 17V, Load: 100 nF, Units: µS	Fmax at DVDD = 3.3V ± .30V (Note 1) Fmax at DVDD = 5.0V ± .50V (Note 4) Full Scale Step, 10V Load: 10 nF, Max: 70, Load: 100 nF, Max: 700, Units: µs Full Scale Step, 17V, Load: 100 nF, Units: ms *Delete: Power Supply Sensitivity*
		Note 4: tested at 33 MHz only ...	Note 4: tested at 55 MHz only; delete last sentence