

10/100 Interface Module with Enhanced Common Mode Attenuation

EPF8017GH



- Optimized for DP83840A/DP83223 Chip Set •
- Recommended for use with ICS 1890 Series and SSI78Q2120 when connected per appropriate schematic
- Guaranteed to operate with 8mA DC bias at 70°C •
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

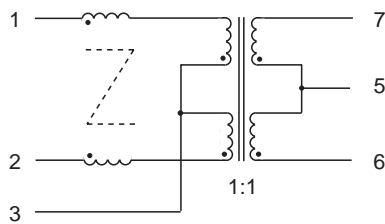
Electrical Parameters @ 25°C

OCL @ 70°C	Insertion Loss (dB Max.)						Return Loss (dB Min.)						Common Mode Rejection (dB Min.)						Crosstalk (dB Min.) [Between Channels]	
100KHz, 0.1Vrms 8mA DC Bias	1-80 MHz		80-100 MHz		100-150 MHz		1-30 MHz		30-60 MHz		60-100 MHz		1-30 MHz		30-100 MHz		100-500 MHz		5-10 MHz	10-100 MHz
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv		
350μH	-1	-1	-2	-2	-3.5	-3	-18	-18	-12	-12	-10	-10	-40	-40	-35	-30	-10	-10	-35	-35

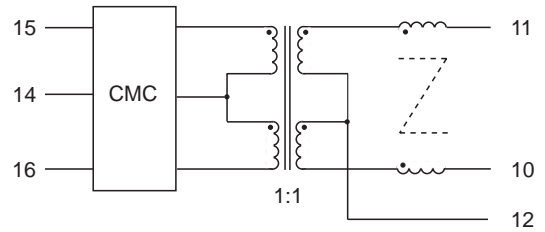
• Isolation : 1500Vrms • Rise Time : 3.0nS Max. • Impedance : 100Ω •

Schematic

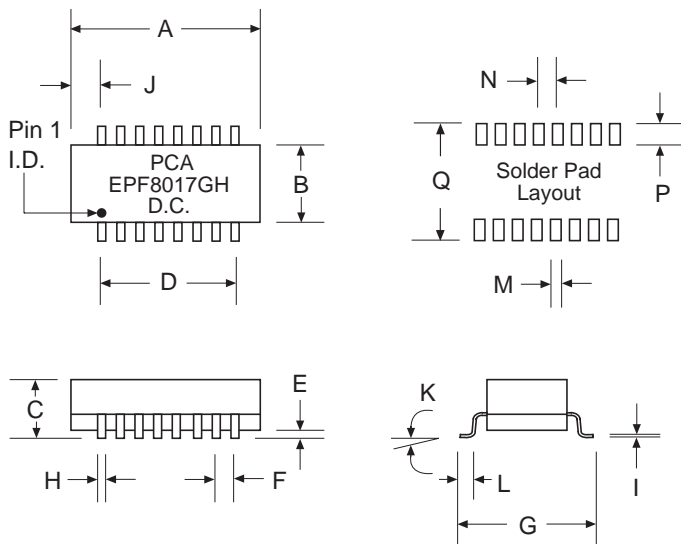
Receive Channel



Transmit Channel



Package



Dimensions

Dim.	(Inches)			(Millimeters)		
	Min.	Max.	Nom.	Min.	Max.	Nom.
A	.970	.990	.980	24.64	25.15	24.89
B	.380	.400	.390	9.65	10.16	9.91
C	.234	.252	.247	5.94	6.40	6.30
D	---	---	.700	---	---	17.78
E	.010	.015	.013	.254	.381	.330
F	---	---	.100	---	---	2.54
G	.490	.510	.500	12.45	12.95	12.70
H	.017	.022	.020	.432	.559	.508
I	.008	.013	.011	.203	.330	.279
J	---	---	.140	---	---	3.56
K	0°	8°	4°	0°	8°	4°
L	.025	.045	.035	.635	1.14	.889
M	---	---	.030	---	---	.762
N	---	---	.100	---	---	2.54
P	---	---	.092	---	---	2.34
Q	---	---	.560	---	---	14.22

The circuit below is a guideline for interconnecting PCA's EPF8017GH with National DP83840A and DP83223 twister chip set for 10/100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes. Please consult PCA for applications help regarding the SSI78Q2120 or ICS1890 series parts or consult with the respective application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the TXREF resistor of the twister chip to get at least 2.12V pk-pk across pins 16-15.

Note that significant low frequency response improvement can be obtained in the system (improving equalization effects) if the DC blocking capacitors were not used; this can only be done by choosing a different pinout for the 10 Base-T receiver side. This is accomplished without impacting any other behavior. If any user has a need to improve this feature, please consult with the PCA Technical support group. This solution is similar to approaches used in EPF8013GM, EPF8022G and EPF8038S (a repeater interface module).

It is recommended that system designers do not use the receiver side center tap to ground, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8017GH. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω , balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP (Excerpts from NSC DP83840A application notes)

