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Photon Vision Systems

High Performance Linear CMOS Image Sensors
ELIS CMOS IMAGER

The Photon Vision Systems ELIS is a family of high performance linear image sensor designed for a wide variety of applications as a superior CCD replacement, including:

Edge Detection
Contact Imaging
Bar Code Reading
Finger Printing
Encoding and Positioning
Text Recognition

Description

The ELIS Linear Image Sensor consists of an array of high performance low dark current photo-diode pixels. The device features nearly the same performance characteristics of our LIS series of linear imagers, but also adds sample and hold capability and the ability to bin pixels together. This in effect allows the user to select the devices resolution. The device can operate at voltages as low as 2.8 VDC. A key feature over traditional CCD technology, is that the device can be read and reread Non-Destructively, allowing the user to maximize signal to noise and dynamic range.

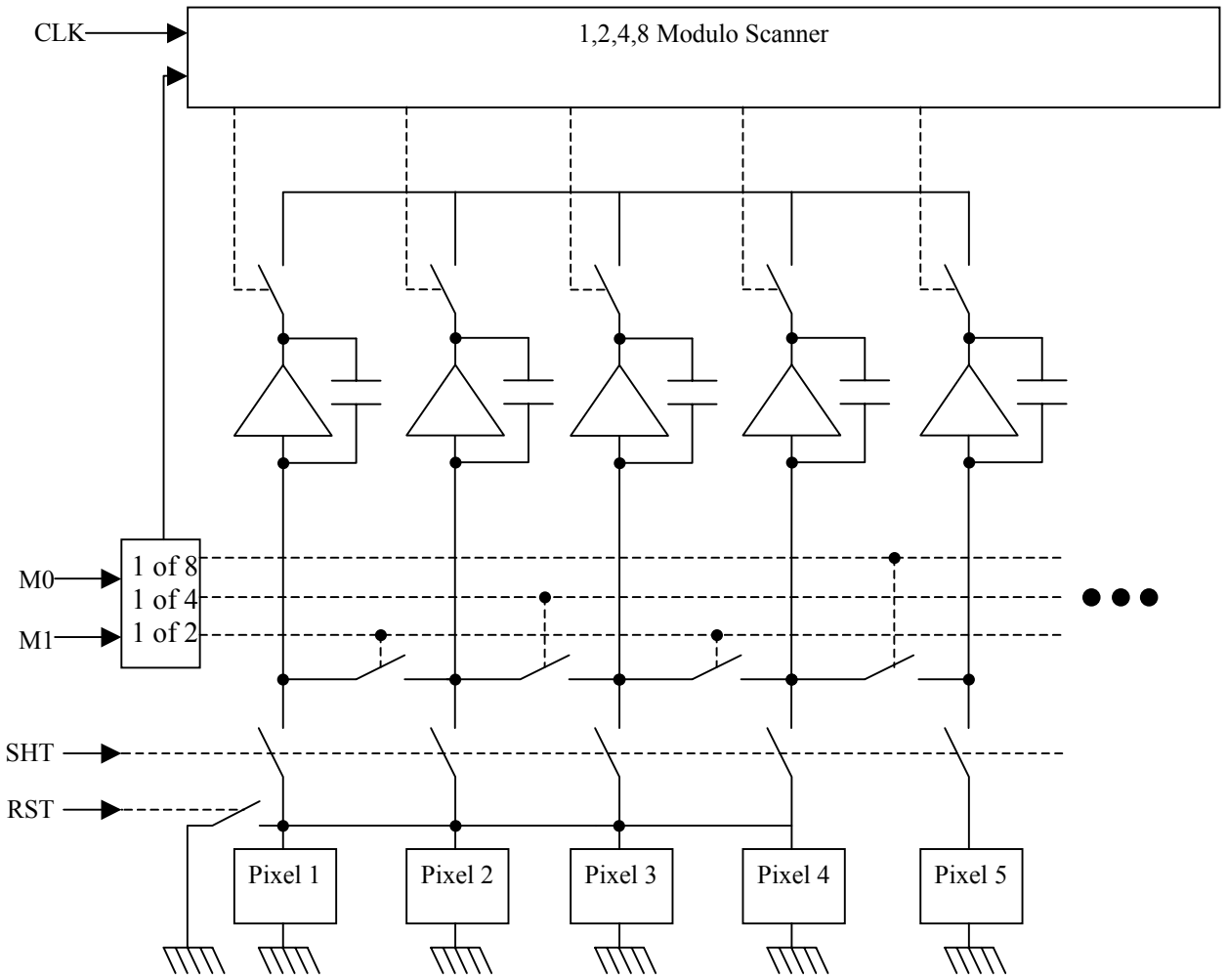
Operation is simplified by on chip logic which requires only the user to select the bin resolution, input a clock equal to the desired pixel read rate, selecting the reset mode, and external reset to initiate read-out when running asynchronously.

The ELIS imager is supplied in our exclusive PHOTO-SURF™ package. The package utilizes an optically clear window, virtually eliminating distortion over that caused by traditional 'clear' plastic packages.

Key Features

- Low Cost
- Single Supply Operation
- Sample and Hold
- High Sensitivity
- High Signal to Noise
- Non-Destructive read capable
- 1.0 kHz. to 40.0 MHz Operation
- Very Low Dark Current
- Optically clear package (Packaged Version)
- Sequential or Frame Operation
- Completely integrated Timing and Control
- Replaces CCD systems, not just the sensor
- Active area is 7.988 mm x 125 microns

FUNCTIONAL BLOCK DIAGAM



Electro-Oprical Characersitics

Parameter	Min	Typical	Max	Units
Supply Voltage (see note 5)	2.80	5.0	5.25	V
Supply Current (see note 1)	8	14	20	mA
Input High Logic Level	2.7			V
Input Low Logic Level			0.6	V
Clock Frequency/Pixel Read Rate (see note 3)	1.0	1000	40000	kHz
External Load	5000			Ohms
Output Voltage at Saturation (see note 5)	2.8	3.3	4.0	V
Output Voltage at Dark	0.64	0.74	0.84	V
Conversion Gain		3.2		$\mu v/e^-$
Full Well		800		ke^-
Dynamic Range	80			dB
Pixel Non-Uniformity Dark		±0.5		%
Linearity (see note2)		1.0		%
Output due to Dark Current (see note 4)	2	19	38	mV/s
Relative Humidity	0		90	%
Operating Temperature	0	25	50	°C

Notes
1. Including Load Resistor
2. Pixel average from 5% - 75% Saturation
3. Specs. Given at pixel read rates of 1 MHz at 24 deg. C At greater read rates, MTF and S/N begin to degrade.
4. At 24 °C.
5. At Supply voltages less than Saturation Voltage, Vo is clipped by supply, no load applied.
6. Temporal rms noise @ 1 Mhz erc and 500khz video band width filter applied, values are typical and may vary. Higher S/N ratios are obtainable with lower erc and bandwidths.

Absolute maximum ratings, T_A = 25°C unless otherwise noted, see Note 1, below. †

Supply voltage range, V_{DD}---------- 0 V to 5.25 V
Digital input current range, I ---------- –20 mA to 20 mA
Operating case temperature range, T_C (see Note 2)---------- –10°C to 70°
Operating free-air temperature range, T_A ---------- 0°C to 50°C
Storage temperature range ---------- –20°C to 85°C
Humidity range, Rh ---------- 0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds----- 255°C

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated under "recommended operating conditions" is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.
NOTES: 1. Voltage values are with respect to the device GND terminal.
2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

PIN DESCRIPTION – PHOTO-SURF™ (16 pin LCC) Package

1	VO	Output	Video Output
2 ,11	AVDD		Analog Power
3, 10	AGND		Analog Ground ref.
4	RM	Input	Reserved for Future use – tie to pin 6, DGND
5	DVDD	Input	Digital Power
6	DGND	Input	Digital Ground ref.
7	CLK	Input	Clock
8, 9	N/C		No connection
12	DATA	Input	Start Readout
13	RST	Input	Reset
14	M0	Input	Bin select bit 0
15	M1	Input	Bin Select bit 1
16	SHT	Input	Shutter

OPERATION AND TIMING

Resolution selection via binning.

Select the desired resolution with the following table;

M0	M1	Resolution	Effective pixel size
0	0	1024	7.8 x 125 microns
1	0	512	15.6 x 125 microns
0	1	256	31.2 x 125 microns
1	1	128	64.4 x 125 microns

The effective imager length is 7.988 mm irregardless of the selected binned resolution. Internally, the device has 1024 pixels. When the binned resolution is set to 512, pixels 1 and 2 photo diodes are averaged and output as a single pixel, pixels 3 and 4 are averaged and output as a single value, and so on. If set to 256 resolution, then pixels 1 through 4 are averaged and output as a single value, 5 through 8 are averaged and output as a single value, and so on.

TIMING

The device allows the user to control the integration time. Note – be sure to tie pin 4 (RM) to DGND.

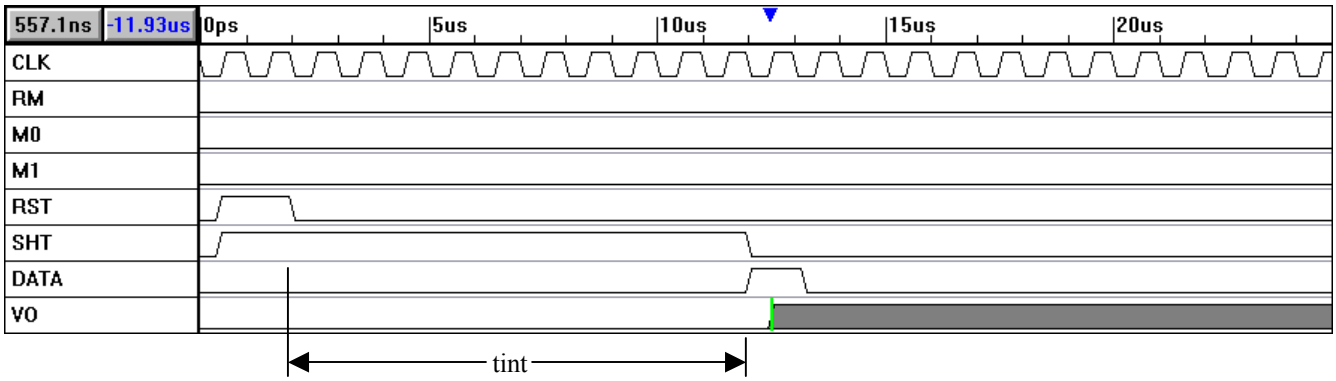


Figure 1 - Start of Frame timing diagram.

Device Reset:
The first 2.0 µs as shown above indicate how to reset the imager. Both the RST input and the SHT input must be simultaneously high for at least 1.0 µs to properly reset the imager. The imager can be held in reset indefinitely by keeping both inputs high.

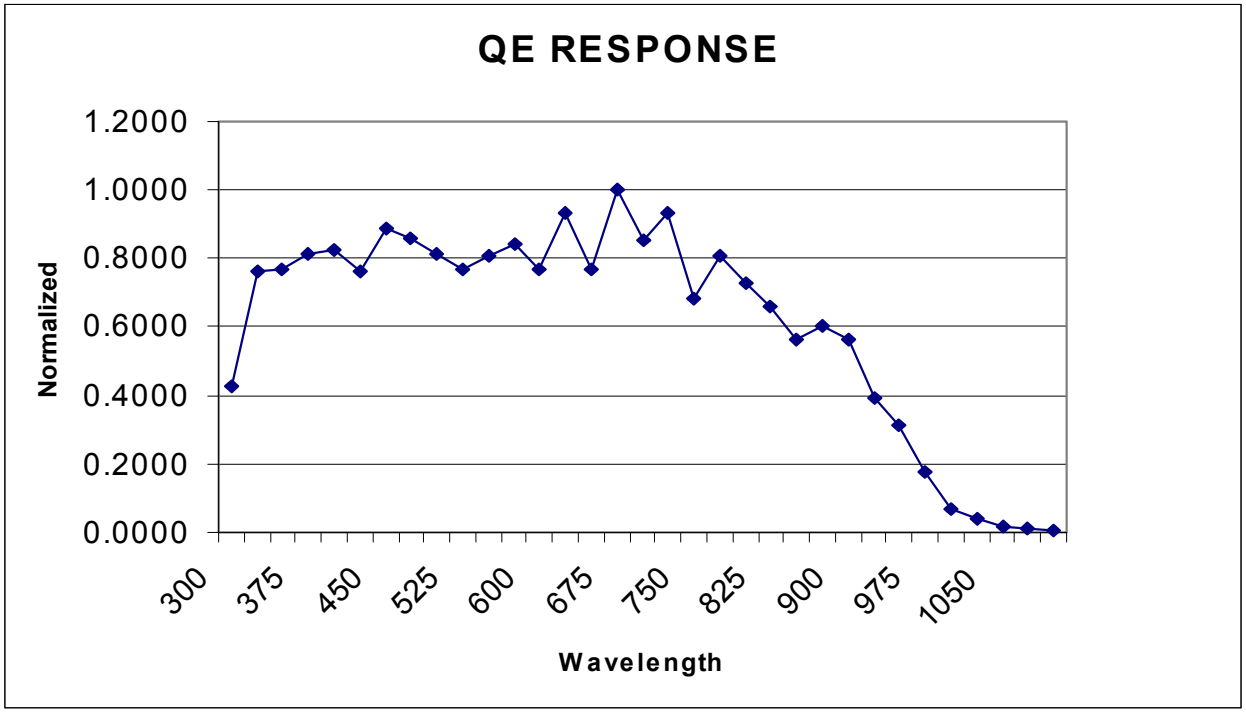
Integration:
Once RST input goes low, the pixel begins to integrate. Integration continues until SHT goes low. The diagram shows the pixel integrating for 10.0 µs.

Readout:
Readout will then begin on the first rising edge of CLK after the DATA input is set high. DATA must be brought low prior to the next rising CLK edge, otherwise pixel 1 is again output.

Binning:
By setting the M0 and M1 inputs as indicated in the Binning table above, different effective resolutions can be realized, with the effective pixel area increasing in the table above. The internal control logic takes care that only one pixel is output per CLK period. So if the imager is binned for 256 resolution, then only 256 additional clock cycles are needed to read out the imager once DATA is set.

NOTES TO TIMING DIAGRAMS

1. Clock duty cycle should be 50%.
2. XXX Clock cycles for the number of pixels to read, starting at the first pixel.
3. t int represents integration time.
4. RST pulse always resets internal counter, thus next pixel output is the first pixel.



Note: Data below 350nm not measured, but device is sensitive to 200 nm. Shown for un-encapsulated device.

MECHANICAL DIMENSIONS –PHOTO-SURF™ PACKAGE

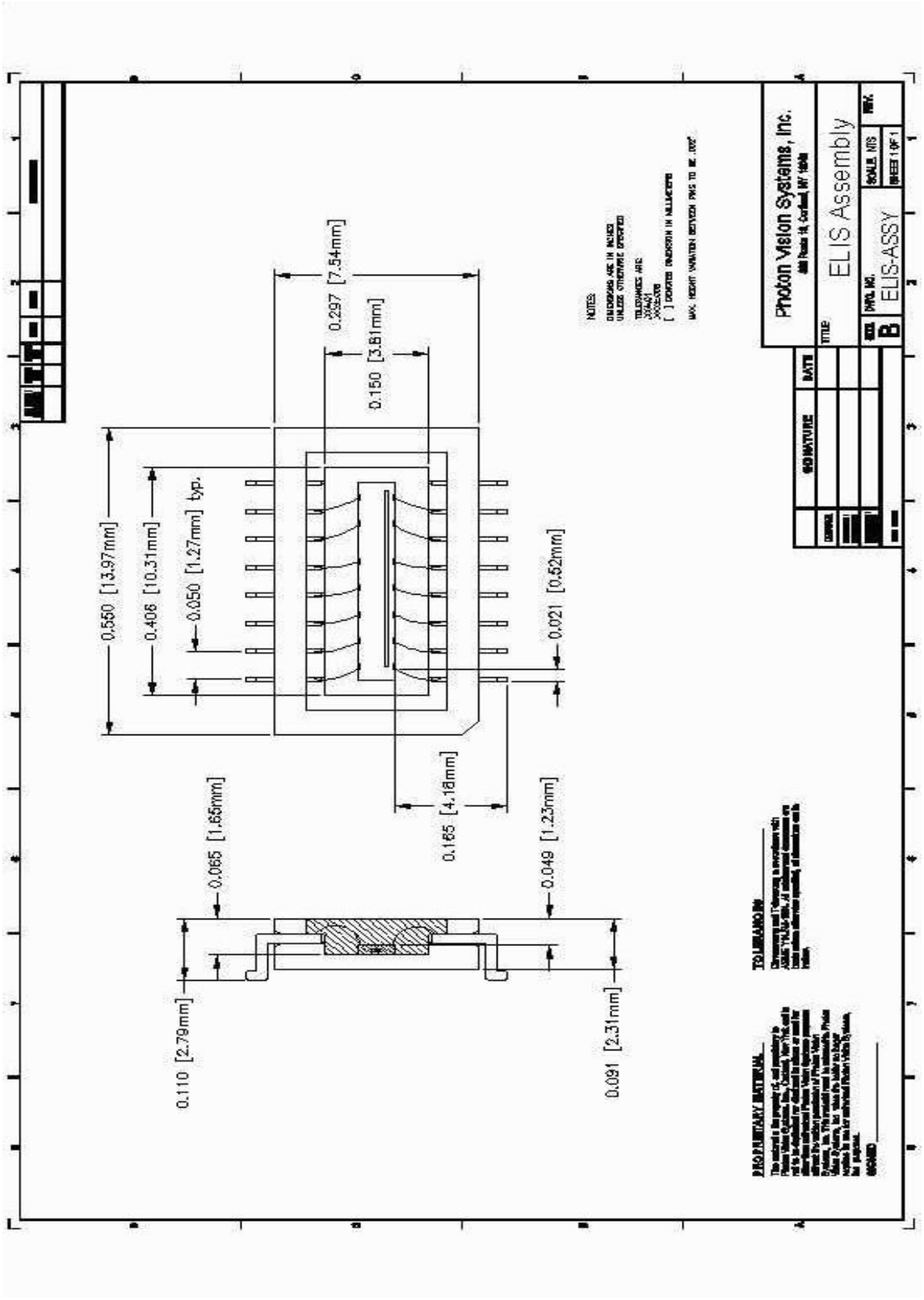


Figure 2 - 16 pin PHOTO-SURF™ Package. Dimensions in millimeters. FOR REFERENCE ONLY.
NOTE: Encapsolant transmission is 99% from 400 to 900 nm, 50% at 350 nm, 0% at 325nm.
Other encapsolants available to allow 75% transmission at 300nm. Contact us for details.

ORDERING INFORMATION

These devices are offered in two package configurations, A Chip Scale Ball Grid Array and a leadlecc Chip Carrier.

ELIS-L Leadless Chip Carrier (LCC)
ELIS-B Chip Scale (BGA)

Contact the factory or your local authorized representative for availability.

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