élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1504C, EL1505C

Differential Line Driver

Features

- Complete ADSL differential driver
- 45 V_{P-P} differential output drive into 200Ω
- -60 dBc typical output distortion at full output at 2 MHz
- Drives 8 single-ended video loads, or 4 S-VHS loads, or 4 differential video loads
- Power surface-mount package

Applications

- ADSL line interface
- HDSL line driver
- Video distribution amplifier
- Video twisted-pair line driver

Ordering Information

Part No	Temp. Range	Package	Outline #
EL1504CM	-40°C to +85°C	20-Pin SOL	MDP0027
EL1505CM	-40°C to +85°C	16-Pin SOL	MDP0027

General Description

The EL1504/5C contains two wideband high-voltage drivers. It is designed to drive 45 V_{P-P} signals at 2 MHz into a 200Ω load differentially with very low distortion.

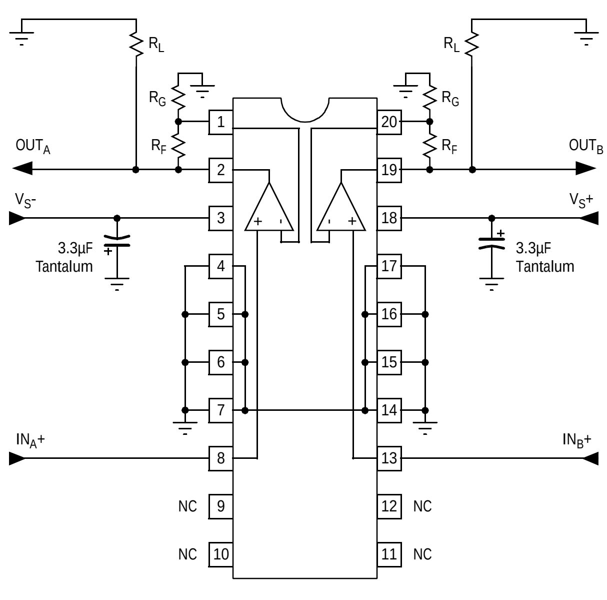
Both amplifiers are of the current-feedback type, giving high slew rates while consuming moderate power. They retain frequency response over a wide range of externally set gains.

The EL1504/5C operate on ±5V to ±15V supplies, and maintain their bandwidths and linearities over the supply range.

The EL1504C, in a 20-Pin Fused Lead SOIC package, has eight center pins which are used as ground connections and heat spreaders. This facilitates the use of external heatsinking to increase the power handling of the device.

The EL1505C, in a 16-Pin SOIC package, is designed for applications which do not require full power and where a smaller PCB footprint is desirable.

Connection Diagram



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Differential Line Driver

Absolute Maximum Ratings (T_A = 25°C)

V_S	V_S+ to V_S- Supply Voltage	33V
V_S+	V_S+ Voltage to Ground	-0.3V to +33V
V_S-	V_S- Voltage to Ground	-33V to 0.3V
V_{IN}	Driver Input Voltage	V_S+ to V_S-
I_{IN}	Current into any Input	8 mA
I_{OUT}	Output Current from Driver (Static)	75 mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Temperature Range	-40°C to +85°C
T_S	Storage Temperature Range	-60°C to +150°C
T_J	Maximum Internal Die Temperature	150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Characteristics

V_S = ±15V, R_F = 1KΩ, R_L = 75Ω, T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Min	Typ	Max	Units
DC Characteristics					
V_{OS}	Input Offset Voltage	-30		30	mV
ΔV_{OS}	V_{OS} Mismatch	-10		10	mV
I_B+	Non-Inverting Input Bias Current	-10		10	µA
I_B-	Inverting Input Bias Current	-40		40	µA
ΔI_B-	I_B- Mismatch	-36		36	µA
R_{OL}	Transimpedance, V_{OUT} from -12V to +12V	0.4	1.6		MΩ
V_{OUT}	Loaded Output Swing	±12.0	±13		V
I_S	Supply Current, All Outputs at 0V		25	35	mA
AC Characteristics					
BW	-3 dB Bandwidth of Amplifiers (R_F = 680Ω)		63		MHz
THD	Total Harmonic Distortion f = 2 MHz, V_S = ±15V, V_{OUT} = 22.5 V_{P-P} f = 2 MHz, V_S = ±9V, V_{OUT} = 10.5 V_{P-P} f = 300 kHz, V_S = ±5V, V_{OUT} = 6 V_{P-P}		 -60 -66 -71		 dBc dBc dBc
dG	Differential Gain Error, Standard NTSC Test A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.17		%
dθ	Differential Phase Error, Standard NTSC Test A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.06		°
SR	Slewrate, V_{OUT} from -10V to +10V Measured at ±15V	500	1000		V/µsec
e_N	Input Noise Voltage		3.3		nV/√Hz
i_N	Input Noise Current		18		pA/√Hz

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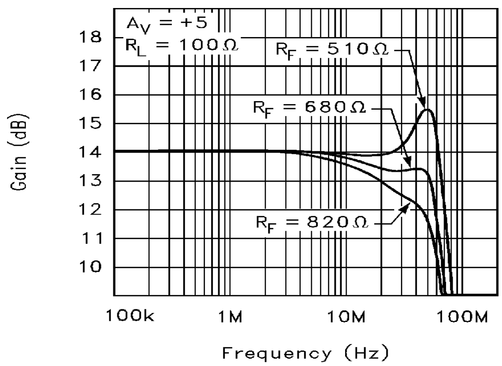
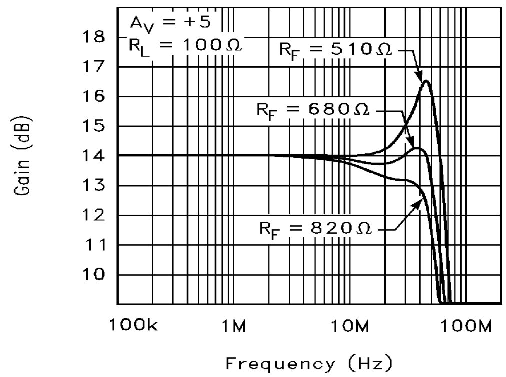
Typical Performance Curves

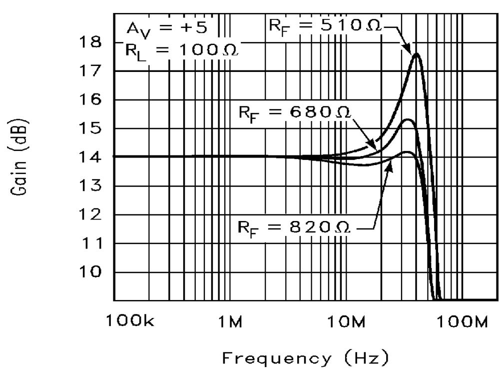
Frequency Response vs R_F
$V_S = \pm 15V$



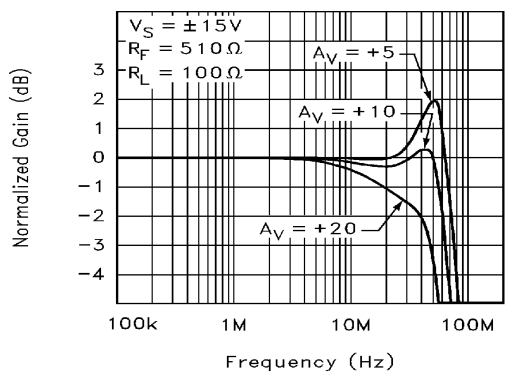
Frequency Response vs R_F
$V_S = \pm 9V$



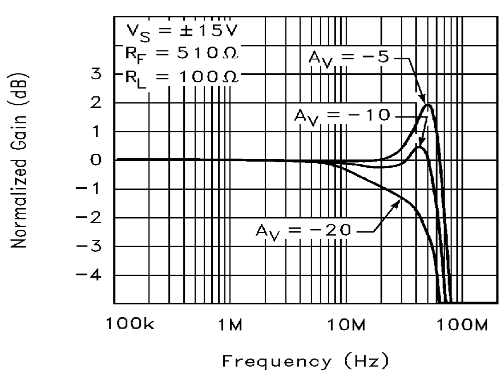
Frequency Response vs R_F
$V_S = \pm 5V$



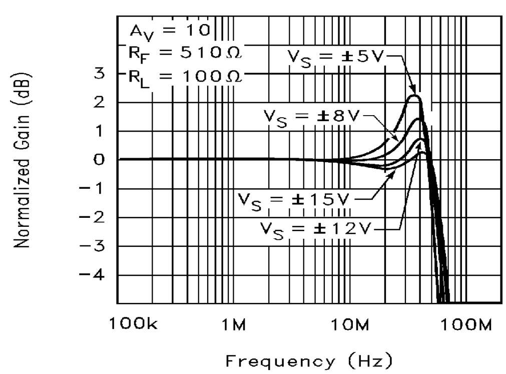
Frequency Response vs Gain (Non-Inverting)



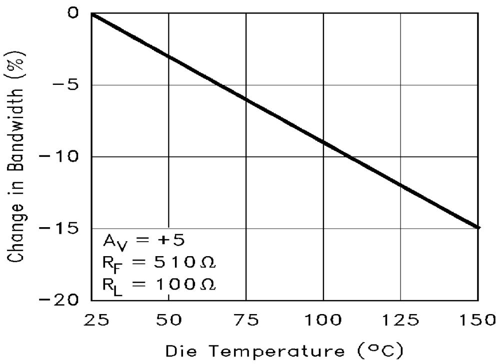
Frequency Response vs Gain (Inverting)



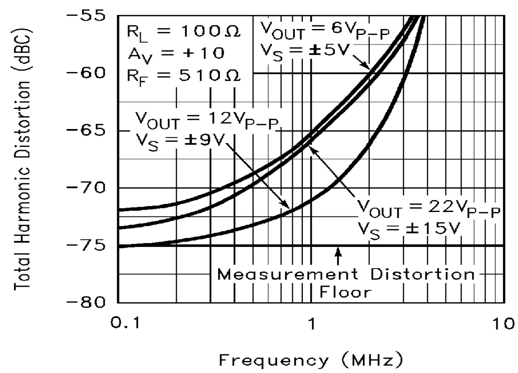
Frequency Response vs Supply Voltage



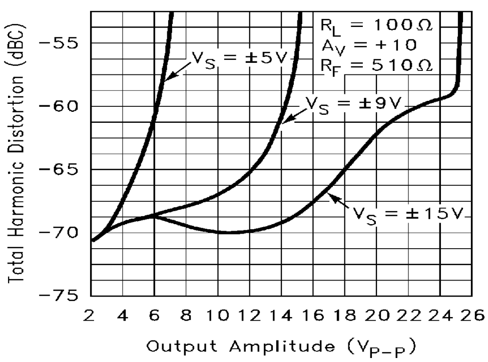
Bandwidth vs Temperature



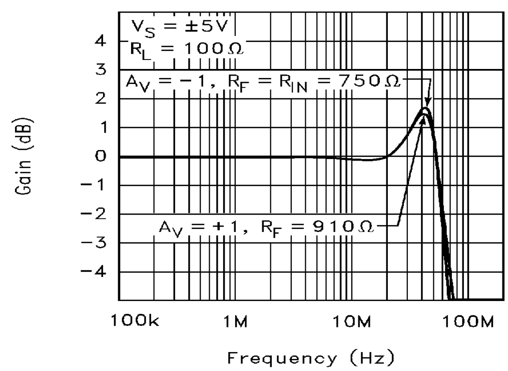
Harmonic Distortion vs Frequency (Single Amplifier)



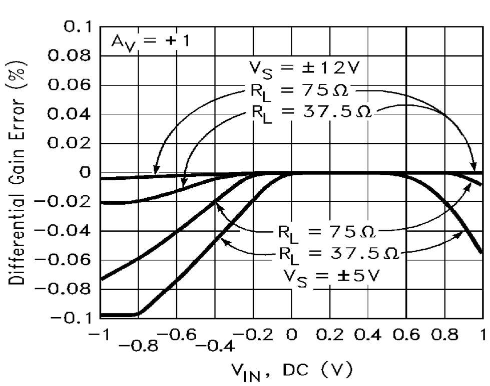
Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)



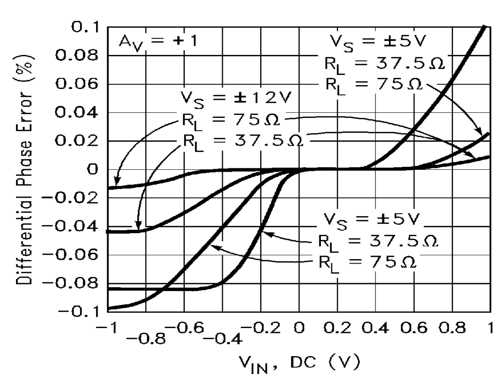
Frequency Response Equalized for Gains of +1 and -1



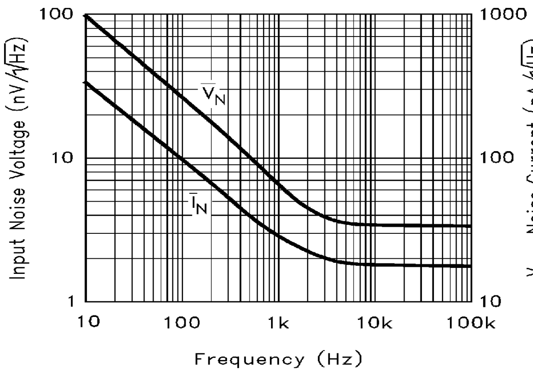
Differential Gain Error vs DC Input Offset



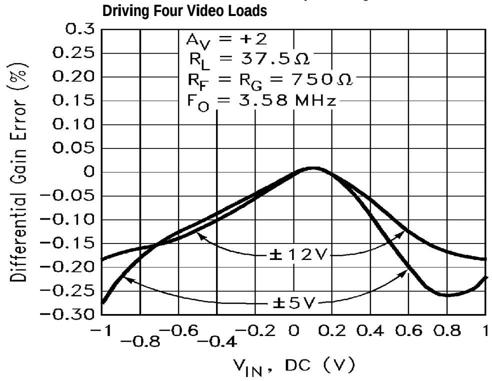
Differential Phase Error vs DC Input Offset



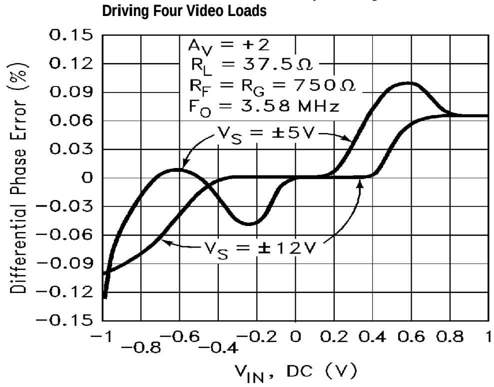
Input Noise Voltage and Current vs Frequency



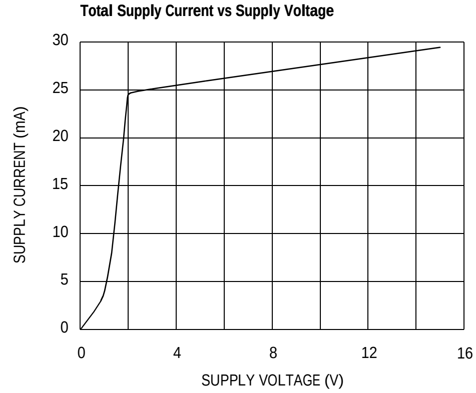
Differential Gain Error vs DC Input Voltage Driving Four Video Loads



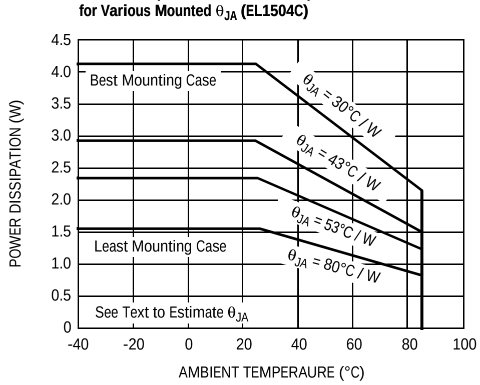
Differential Phase Error vs DC Input Voltage Driving Four Video Loads



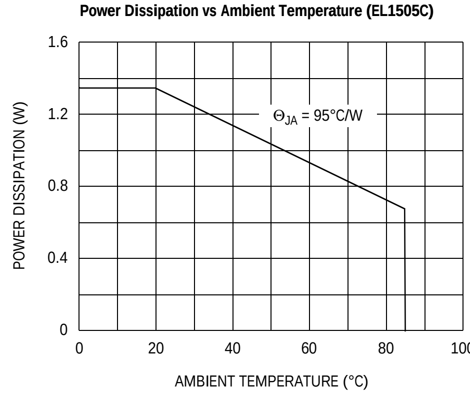
Total Supply Current vs Supply Voltage



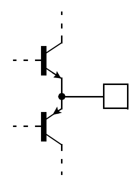
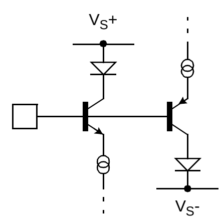
Power Dissipation vs Ambient Temperature for Various Mounted θ_{JA} (EL1504C)



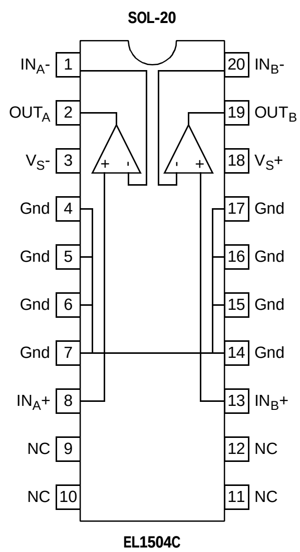
Power Dissipation vs Ambient Temperature (EL1505C)

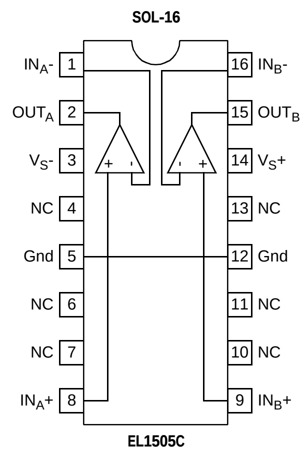


Pin Description

EL1504C	EL1505C	Pin Name	Function	Circuit
1	1	IN_A-	Inverting Input Channel A	 Circuit 1
2	2	OUT_A	Output of Channel A	(Reference Circuit 1)
3	3	V_S-	Negative Supply	
		GND	Ground Connection	
8	8	IN_A+	Non-Inverting Input Channel A	 Circuit 2
		NC	Not Connected	
13	9	IN_B+	Non-Inverting Input Channel B	(Reference Circuit 2)
18	14	VS+	Positive Supply	(Reference Circuit 2)
19	15	OUT_B	Output of Channel B	(Reference Circuit 1)
20	16	IN_B-	Inverting Input Channel B	(Reference Circuit 1)

Pin Configurations





EL1504C, EL1505C

Differential Line Driver

Applications Information

The EL1504/5C consists of two power line drivers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 4 MHz and produce low distortion levels.

Here is a typical interface circuit:

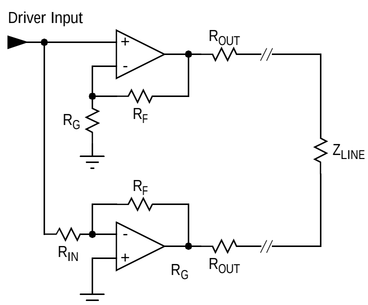


Figure 1. Typical Line Interface Connection

The amplifiers are wired one in positive gain and the other in negative gain configuration to generate a differential output for a single-ended input. The drivers will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver. The Typical Performance Curves section of this data sheet has a plot of driver responses matched at gains of +1 and -1 using feedback resistors of 910Ω and 750Ω, respectively.

If a differential signal is available to the drive amplifiers, they may be wired so:

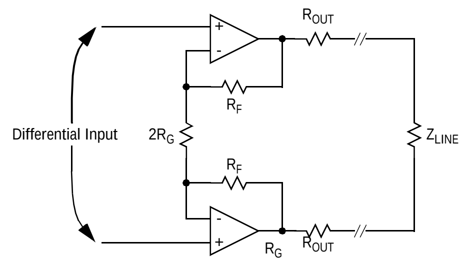


Figure 2. Drivers Wired for Differential Input

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The drivers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100 nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4" of unshielded wiring, or 6" of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Resistive sources greater than 2 kΩ will cause the driver to exhibit increased harmonic distortion. Most amplifier output stages are much lower in impedance and give no problem.

Power Supplies & Dissipation

The EL1504/5C works well over the ±5V to ±15V supply range. Frequency response varies only slightly, and output drive capability is constant. The major supply voltage issue is power dissipation. The internal dissipation P_D for an EL1504/5C running on supply voltages of $\pm V_S$ and delivering a DC output voltage V_O into a load of R_L is:

$$P_D = 2 \times V_S \times I_S + 2 \times (V_S - V_O) \times V_O / R_L$$

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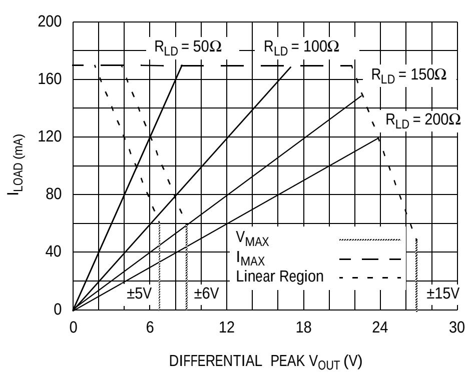
The first term of the equation is the quiescent dissipation and the second term is the dissipation due to both amplifiers driving a load. If outputs are sinusoidal signals of V_O volts per amplifier peak-to-peak rather than DC the dissipation is:

$$P_D = 2 \times V_s \times I_s + 2 \times \frac{\sqrt{\frac{V_s^2 \times V_o^2}{8} - \frac{V_s \times V_o^3}{3\pi} + \frac{3 \times V_o^4}{128}}}{R_L}$$

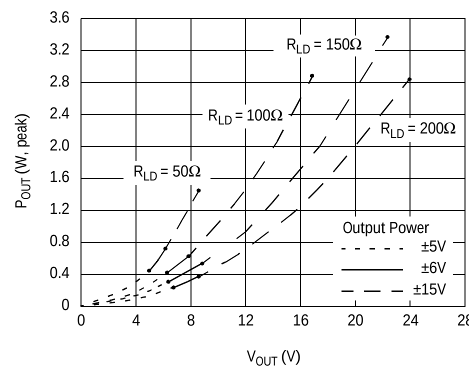
where R_L refers to the load seen by one amplifier connected in the differential configuration described in the previous page. The following graphs refer to R_{LD} which is the differential load seen by both amplifiers.

Load Lines for Various Loads



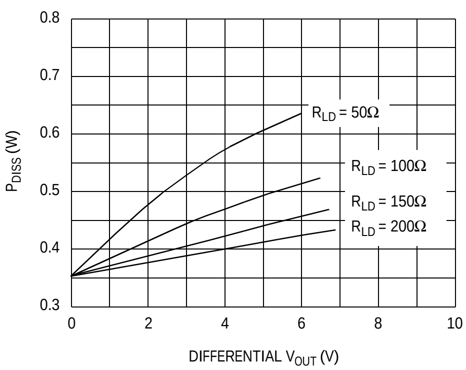
The graph above shows the output current capability of a differentially connected driver pair with different V_S, V_{OUT} and R_{LD}. The area between the horizontal, vertical and diagonal lines represents the linear operating region of the device. The upper horizontal line is the maximum current handling capability of the device and is limited by the linearity of the output transistors. The vertical lines are the peak output voltage swings with different supply voltages limited by clipping. The diagonal lines result from the series resistance of the output transistors.

Output Power for a Given Load

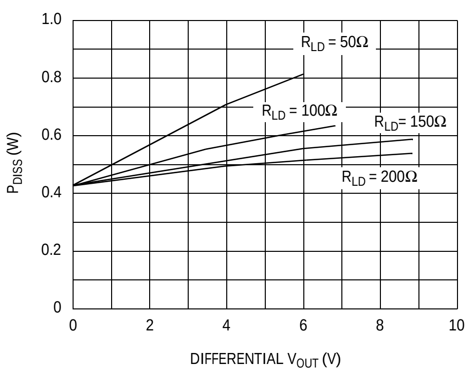


The graph above shows the peak power available as the output swing is varied for different power supplies. The different line styles represent the maximum power which can be reached for a given supply voltage. The dots delineate the ±5V, ±6V, and ±15V regions on each curveIt is interesting to note that the 100Ω load and the 200Ω load cases both produce similiar power output for a supply voltage of ±15V and that more power can be obtained by using a 150Ω load. By referring back to the first graph we can see that the 150Ω load would be the best choice because that load line intersects the linear region of output operation as opposed to the 100Ω load line which intersects the maximum current line.

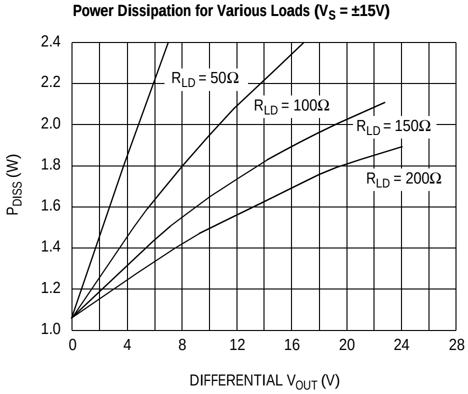
Power Dissipation for Various Loads (V_S = ±5V)



Power Dissipation for Various Loads (V_S = ±6V)



Power Dissipation for Various Loads (V_S = ±15V)



The preceeding three graphs show the internal dissipation of the device for various supply voltages and loads. Note that these curves are calculated for a continuous sine wave at worst case supply current (I_S=35mA) using the equation mentioned before and since ADSL transmissions signals have a large peak to average power ratio, AC dissipation is more likely to be 25% of continuous maximum output level. By consulting the curves, a choice can be made between the EL1504C or EL1505C for different values of V_{OUT} and R_{LD}. Note that 50Ω and 100Ω loads are not practical loads for a 15V supply as even small output swings exceed the maximum dissipation of the device. Maximum dissipation also depends on the ambient temperature T_A - the graphs shown were calculated at T_A= 85°C, but the dissipation can be calculated for any T_A from the following equation.

For a given θ_{JA}, the maximum P_D is

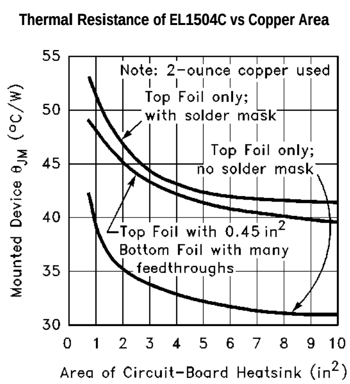
$$P_D = \frac{(T_{MAX} - T_A)}{\theta_{JA}}$$

where T_{MAX} = 150°C, the maximum die temperature in a plastic package, T_A is the ambient air temperature and θ_{JA} is the thermal resistance of the package in question. When the package is mounted on a heatsink, θ_{JA} is refered to as θ_{JM}.

The 20 lead EL1504C package will exhibit a θ_{JA} of 80°C/W with no assistance from circuit board heatsinks. This will suffice for the lowest supply voltages and output levels. The best θ_{JM} that can be obtained is about 30°C/W, and a practical layout would produce 43°C/W.

More detail is available from the Elantec application note *Measuring the Thermal Resistance of Power Surface-Mount Packages*.

This plot summarizes the note's results:



The θ_{JA} for the EL1505C is fixed at 95°C/W and so the applications of the EL1505C are limited to the lower supply voltages and higher loads.

EL1504C PCB Design

The 20-lead SO Power Package (EL1504C) is designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JM}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask should be cut away from the EL1504C to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

EL1505C Considerations

Because the EL1505C package does not have any special method for conducting heat away from the package, care must be taken to ensure that the maximum dissipation is not exceeded. The ambient temperature in the enviroment in which the device is to be used, the supply voltage and the desired output current to drive the required load all must be taken into account. The table below shows some possible configurations.

Possible Load Configurations

V_S	Diff V_{OUT} (Peak)	Diff R_{LOAD}	I_{OUT} (Peak)	P_{OUT} (Peak)	P_{DISS} (RMS)
±5V	5V	50Ω	100mA	500mW	629mW
±5V	6.5V	100Ω	65mA	423mW	517mW
±5V	6.8V	150Ω	45mA	308mW	464mW
±5V	6.8V	200Ω	34mA	231mW	436mW
±6V or +12V	5.99V	50Ω	120mA	718mW	821mW
±6V or +12V	7.88V	100Ω	79mA	620mW	662mW
±6V or +12V	8.8V	150Ω	59mA	516mW	592mW
±6V or +12V	8.8V	200Ω	44mA	387mW	549mW
±15V	20.21V	100Ω	202mA	4.084W	2.586W
±15V	22.58V	150Ω	151mA	3.398W	2.141W
±15V	23.98V	200Ω	120mA	2.876W	1.895W

For loads other than the ones mentioned above, the associated graphs in the previous sections can be used to determine the required copper board area and whether a load is feasible or not.

Output Loading

While the drive amplifiers can output in excess of 250 mA, the internal metallization is not designed to carry more than 75 mA of steady DC current and there is no current-limit mechanism. This allows safely driving peak sinusoidal currents of π x 75 mA, or 236 mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25 pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Power Supplies

The power supplies should be well bypassed close to the EL1504/5C. A 3.3µF tantalum capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1504/5C demonstration board, and documentation can be obtained from the factory.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage and gain settings. The drivers can be used for a wide range of gains. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1 dB peaking) for different supply voltages and gains:

Optimum Driver Feedback Resistor for Various Gains and Supply Voltages

Supply Voltage	Driver Voltage Gain				
	-1	+1	2.5	5	10
±5V	750Ω	910Ω	750Ω	680Ω	620Ω
±9V	680Ω	820Ω	680Ω	620Ω	510Ω
±15V	620Ω	750Ω	620Ω	510Ω	470Ω

Driving Video Loads

Each driver can drive four double-terminated video loads while operating on ±5V supplies. Larger supply voltages slightly improve differential gain and phase distortions, which are around 0.2% and 0.1° for single-ended outputs with the standard NTSC test.

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Differential Line Driver

General Disclaimer

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