élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1503C

High Power Differential Line Driver

Features

- High power ADSL driver
- 39.2V_{P-P} differential output drive into 22Ω
- 42.4V_{P-P} differential output drive into 65Ω
- Driver $2^{nd}/3^{rd}$ harmonics of -66dBc/-72dBc at 2V_{P-P} into 100Ω differential
- Supply current of 12.5mA per amplifier
- Supply current control
- Power saving modes
- Standard surface-mount packages

Applications

- ADSL line driver
- HDSL2 line driver
- Video distribution amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1503CM	-40°C to +85°C	20-Pin SO	MDP0027
EL1503CL	-40°C to +85°C	24-Pin LPP	MDP0046

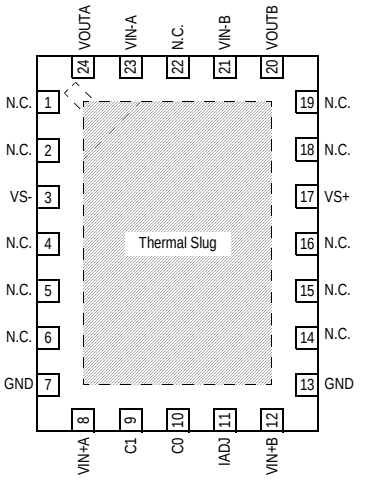
General Description

The EL1503C ADSL Line Driver contains two wideband high-voltage drivers which are ideally suited for both ADSL and HDSL2 applications. They can supply a 39.2V_{P-P} signal into a 22Ω load while exhibiting very low distortion. The EL1503C also has a number of power saving features. The IADJ pin can be used to set the maximum supply current and the C_0 and C_1 pins can be used to digitally vary the supply current to one of four modes. These modes include full power, low power, terminate only and power down.

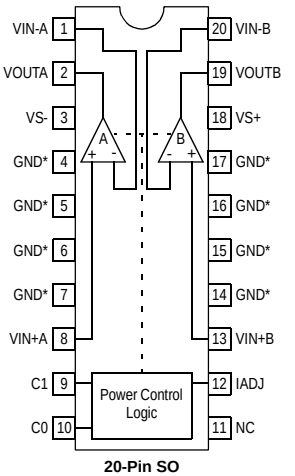
The EL1503C uses current-feedback type amplifiers, which achieve a high slew rate while consuming moderate power. They retain their frequency response over a wide range of externally set gains. The EL1503C operates on ±5V to ±12V supplies and consumes only 12.5mA per amplifier.

The device is supplied in a standard form factor, 20-pin SO package as well as the small footprint (4x5mm) 24-pin LPP. Center pins on each side of the 20-pin package are used as ground connections and heat spreaders. The LPP package has the potential for a low θ_{JA} (<40°C/W) and dissipates heat by means of a thermal pad that is soldered onto the PCB. Both package options are specified for operation over the full -40°C to +85°C temperature range.

Connection Diagrams



24-Pin LPP Top View



20-Pin SO

* GND pins are heat spreaders

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Absolute Maximum Ratings (T_A = 25°C)

Values beyond absolute maximum ratings can cause the device to be prematurely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_S+ to V_S- Supply Voltage	26.4V
V_S+ Voltage to Ground	-0.3V to +26.4V
V_S- Voltage to Ground	-26.4V to 0.3V
Input C0/C1 to Ground	7V
Driver V_{IN}+ Voltage	V_S- to V_S+
Current into Any Input	8mA
Output Current from Driver (Static)	100mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-60°C to +150°C
Operating Junction Temperature	-40°C to +150°C
Power Dissipation	See Curves
ESD Voltage	2kV

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

V_S = ±12V, R_F = 1.5kΩ, R_L= 65Ω, IADJ =C0 = C1 = 0V, T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Conditions	Min	Typ	Max	Unit
Supply Characteristics						
I_S+(Full Power)	Positive Supply Current per Amplifier	All Outputs at 0V, C0 = C1 = 0V	10	12.5	16	mA
I_S-(Full Power)	Negative Supply Current per Amplifier	All Outputs at 0V, C0 = C1 = 0V	-15	-11.5	-9	mA
I_S+(Low Power)	Positive Supply Current per Amplifier	All Outputs at 0V, C0 = 5V, C1 = 0V	7	9	11.5	mA
I_S-(Low Power)	Negative Supply Current per Amplifier	All Outputs at 0V, C0 =5V, C1 = 0V	-10.5	-8	-6	mA
I_S+(Terminate)	Positive Supply Current per Amplifier	All Outputs at 0V, C0 = 0V, C1 = 5V	4	5.1	7	mA
I_S-(Terminate)	Negative Supply Current per Amplifier	All Outputs at 0V, C0 = 0V, C1 = 5V	-6	-4	-3	mA
I_S+(Power Down)	Positive Supply Current per Amplifier	All Outputs at 0V, C0 = C1 = 5V	0.75	1.05	1.7	mA
I_S-(Power Down)	Negative Supply Current per Amplifier	All Outputs at 0V, C0 = C1 = 5V	-0.5	-0.25	0.07	mA
I_{GND}	Gnd Supply Current per Amplifier	All Outputs at 0V		-1		mA
Input Characteristics						
V_{OS}	Input Offset Voltage		-30		30	mV
ΔV_{OS}	V_{OS} Mismatch		-15		15	mV
I_B+	Non-Inverting Input Bias Current		-15		15	µA
I_B-	Inverting Input Bias Current		-50		50	µA
ΔI_B-	I_B- Mismatch		-30		30	µA
R_{OL}	Transimpedance		0.4	0.8		MΩ
e_N	Input Noise Voltage			4.5		nV√Hz
i_N	-Input Noise Current			13		pA√Hz
V_{IH}	Input High Voltage	C0 & C1 inputs	2.7			V
V_{IL}	Input Low Voltage	C0 & C1 inputs			0.8	V
I_{IH1}	Input High Current for C1	C1 = 5V	1.5		8	µA
I_{IH0}	Input High Current for C0	C0 = 5V	0.75		4	µA
I_{IL}	Input Low Current for C1or C0	C1 = 0V, C0 = 0V	-1		1	µA
Output Characteristics						
V_{OUT}	Loaded Output Swing	R_L = 65Ω	±10.3	±10.6		V
		R_L = 22Ω	±9.3	±9.8		V
I_{OL}	Linear Output Current	A_V =5, R_L=10Ω, f=100kHz, THD=-60dBc		450		mA
I_{OUT}	Output Current	V_{OUT} = 1V, R_L = 1Ω		1		A

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Electrical Characteristics

V_S = ±12V, R_F = 1.5kΩ, R_L= 65Ω, IADJ =C0 = C1 = 0V, T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Conditions	Min	Typ	Max	Unit
Dynamic Performance						
BW	-3 dB Bandwidth	A_V = +5		80		MHz
HD2	2nd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{p-p}$		-66		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = $2V_{p-p}$		-61		dBc
HD3	3rd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{p-p}$		-77		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = $2V_{p-p}$		-72		dBc
SR	Slewrate	V_{OUT} from -8V to +8V Measured at ±4V	700	1100		V/µsec

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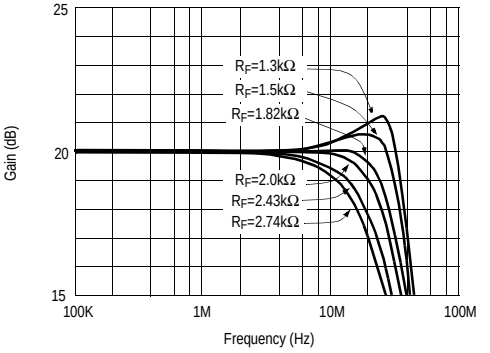
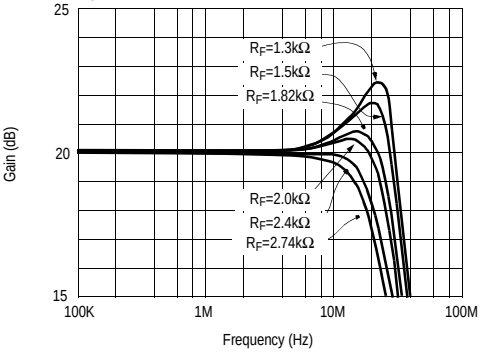
Performance Curves

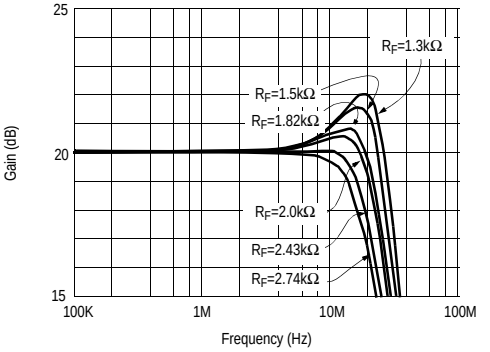
Driver Differential Frequency Response vs R_F
V_S=±12V, A_V=10, R_L=100Ω, Full Power Mode



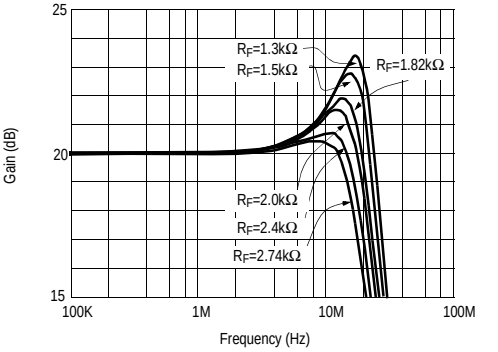
Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=10, R_L=100Ω, Full Power Mode



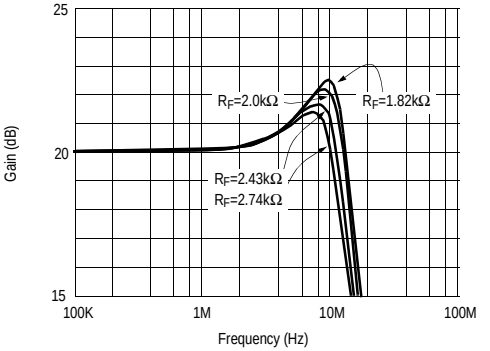
Driver Differential Frequency Response vs R_F
V_S=±12V, A_V=10, R_L=100Ω, 2/3 Power Mode



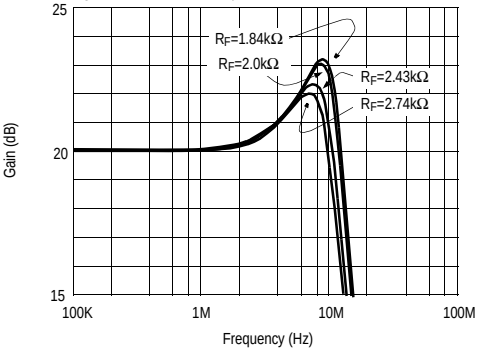
Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=10, R_L=100Ω, 2/3 Power Mode



Driver Differential Frequency Response vs R_F
V_S=±12V, A_V=10, R_L=100Ω, Terminate Mode

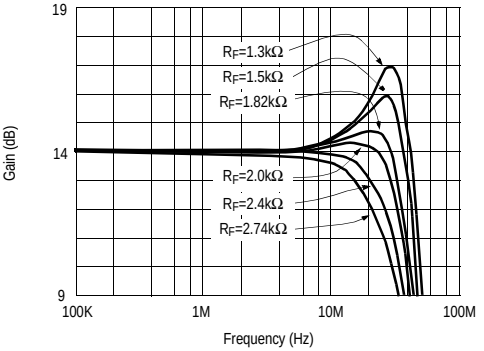


Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=10, R_L=100Ω, Terminate Mode

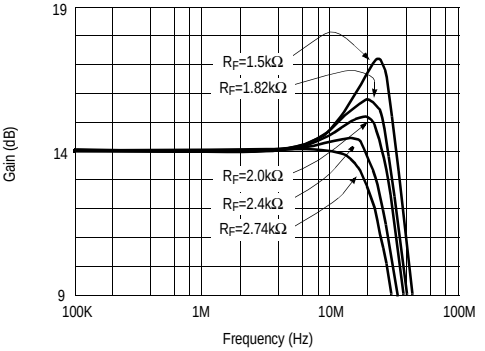


Performance Curves

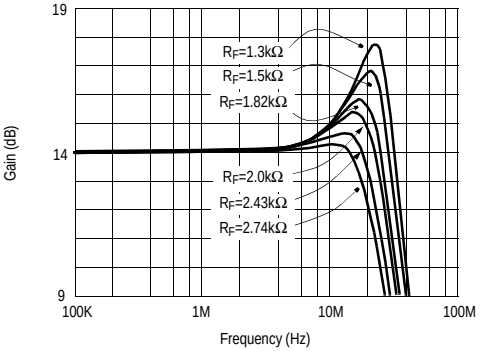
Driver Differential Frequency Response vs R_F
V_S=±12V, A_V=5, R_L=100Ω, Full Power Mode



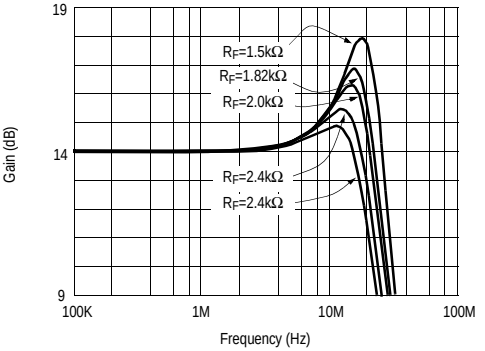
Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=5, R_L=100Ω, Full Power Mode



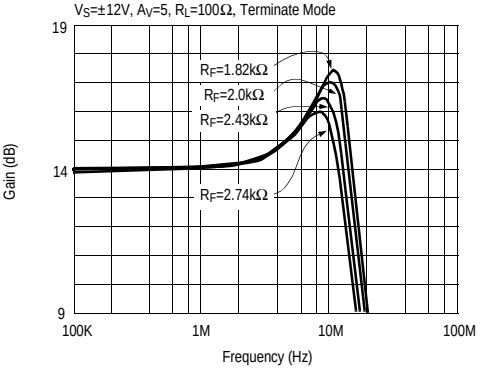
Driver Differential Frequency Response vs R_F
V_S=±12V, A_V=5, R_L=100Ω, 2/3 Power



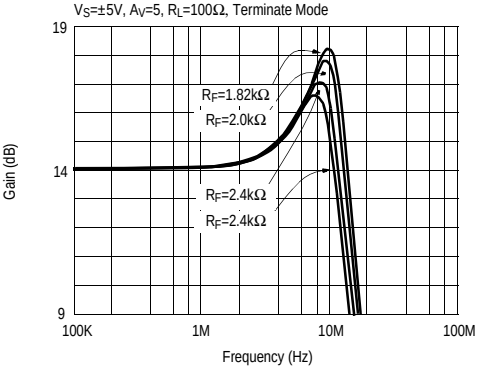
Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=5, R_L=100Ω, 2/3 Power Mode



Driver Differential Frequency Response vs R_F
V_S=±12V, A_V=5, R_L=100Ω, Terminate Mode



Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=5, R_L=100Ω, Terminate Mode



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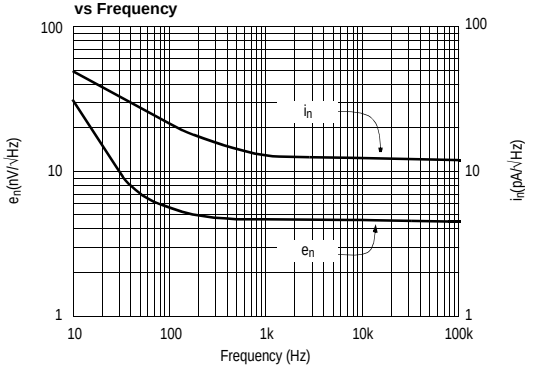
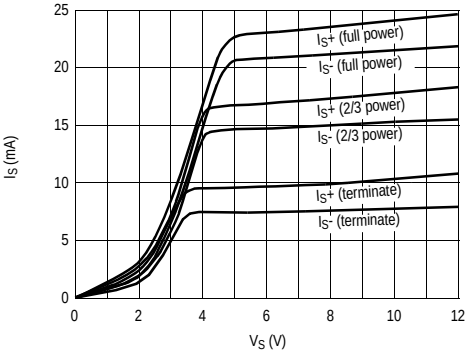
High Power Differential Line Driver

Performance Curves

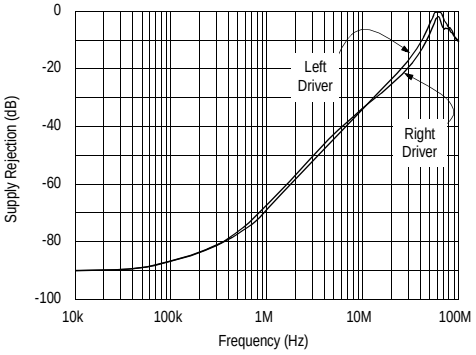
Driver Input Voltage and Feedback Current Noise vs Frequency



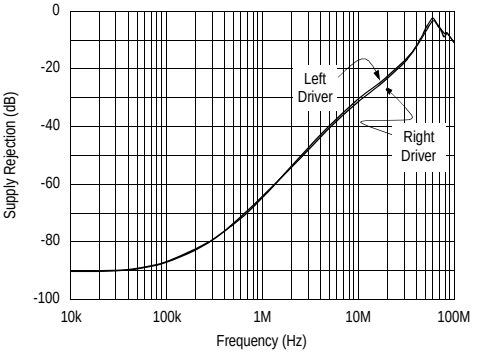
Supply Current vs Supply Voltage



Positive Supply Rejection vs Frequency

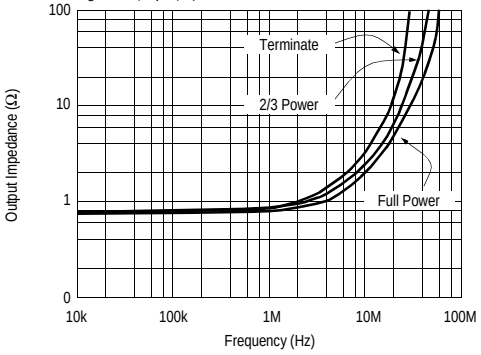


Negative Supply Rejection vs Frequency



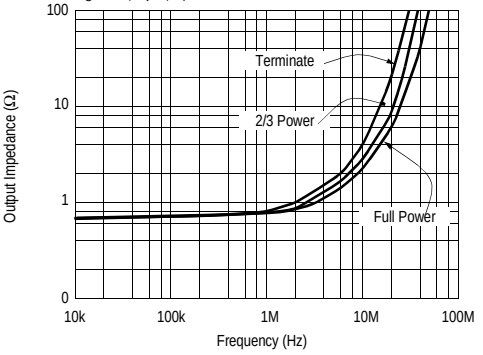
Output Impedance vs Frequency

V_S =±12V, A_V=1, R_F=1.5k



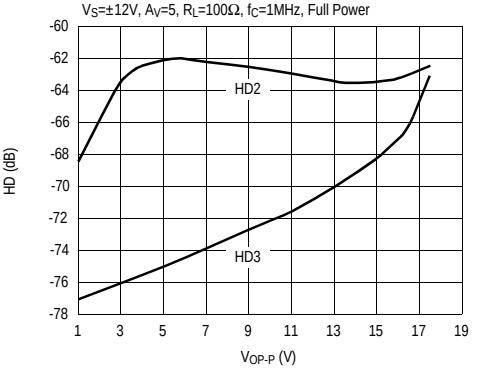
Output Impedance vs Frequency

V_S =±5V, A_V=1, R_F=1.5k

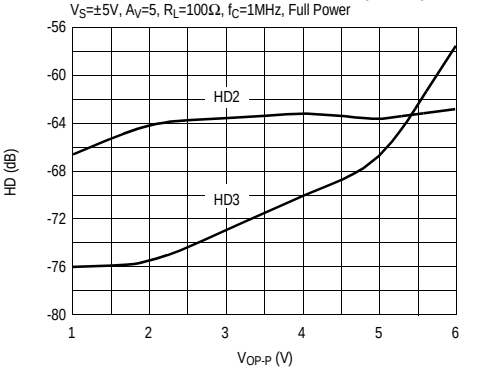


Performance Curves

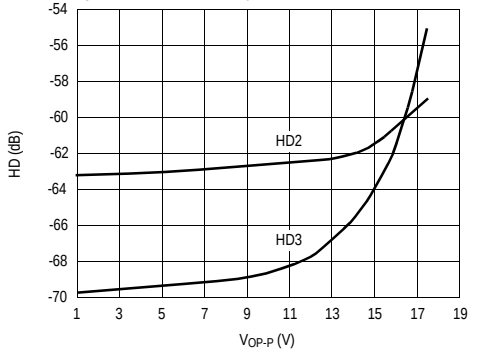
Differential Harmonic Distortion vs Output Amplitude
V_S=±12V, A_V=5, R_L=100Ω, f_C=1MHz, Full Power



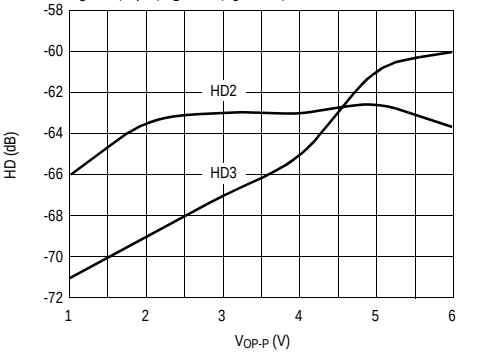
Differential Harmonic Distortion vs Output Amplitude
V_S=±5V, A_V=5, R_L=100Ω, f_C=1MHz, Full Power



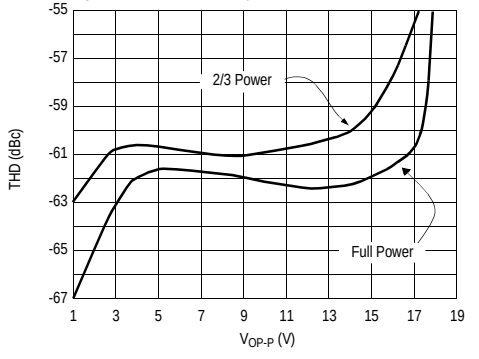
Differential Harmonic Distortion vs Output Amplitude
V_S=±12V, A_V=5, R_L=100Ω, f_C=1MHz, 2/3 Power



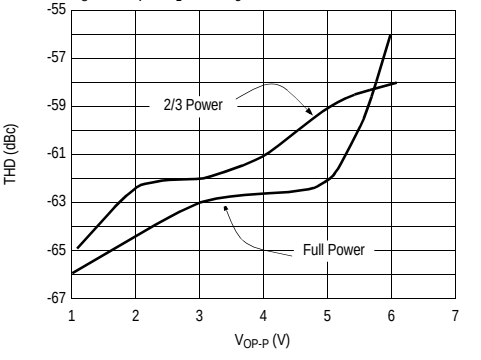
Differential Harmonic Distortion vs Output Amplitude
V_S=±5V, A_V=5, R_L=100Ω, f_C=1MHz, 2/3 Power



Differential Total Harmonic Distortion vs Output Amplitude
V_S=±12V, A_V=5, R_L=100Ω, f_C=1MHz



Differential Total Harmonic Distortion vs Output Amplitude
V_S=±5V, A_V=5, R_L=100Ω, f_C=1MHz



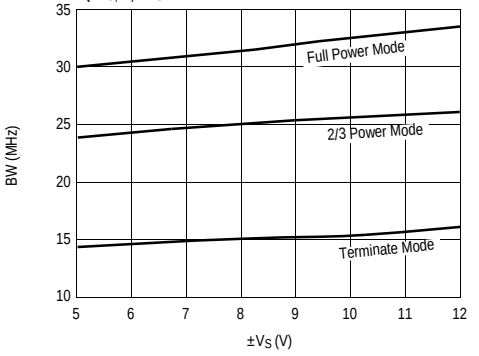
EL1503C

High Power Differential Line Driver

Performance Curves

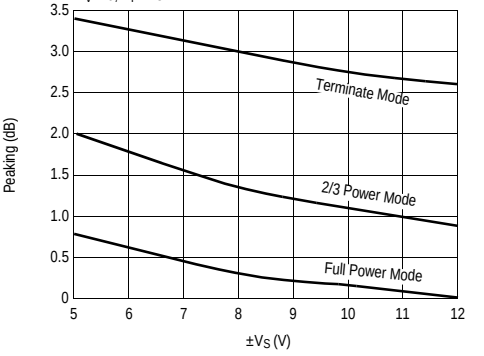
Differential Bandwidth vs Supply Voltage

A_V=10, R_F=1.82kΩ



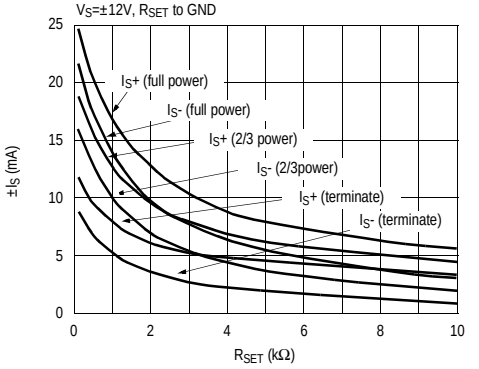
Differential Peaking vs Supply Voltage

A_V=10, R_F=1.82kΩ



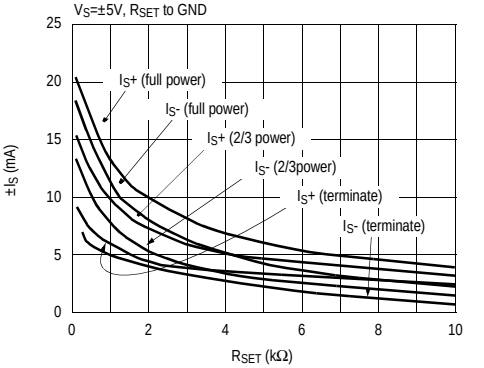
I_S vs R_{SET}

V_S=±12V, R_{SET} to GND



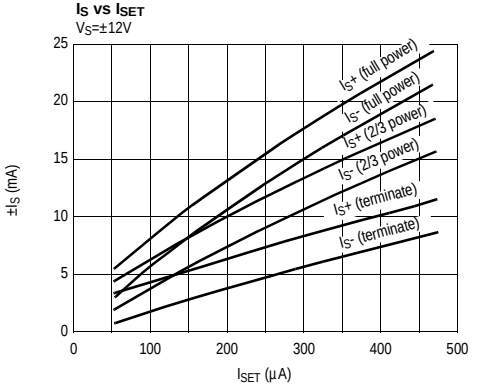
I_S vs R_{SET}

V_S=±5V, R_{SET} to GND



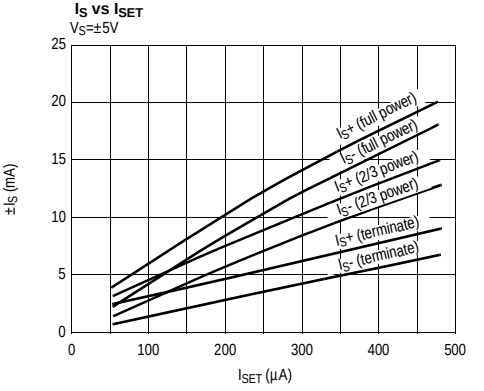
I_S vs I_{SET}

V_S=±12V



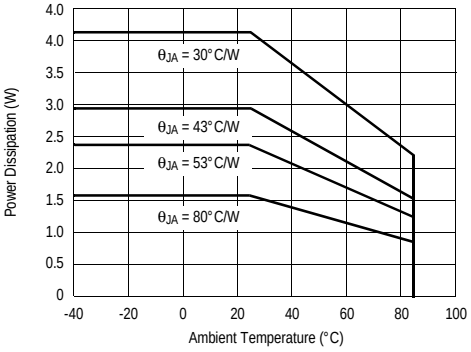
I_S vs I_{SET}

V_S=±5V

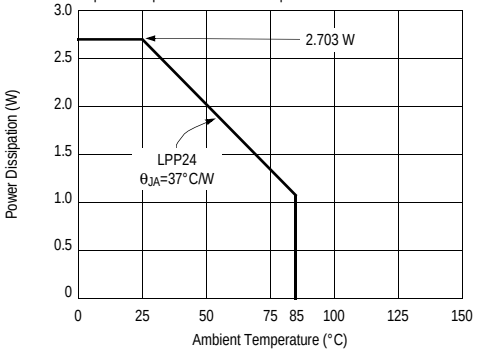


Performance Curves

Power Dissipation vs Ambient Temperature for Various Mounted θ_{JA}s, 20-Pin SO



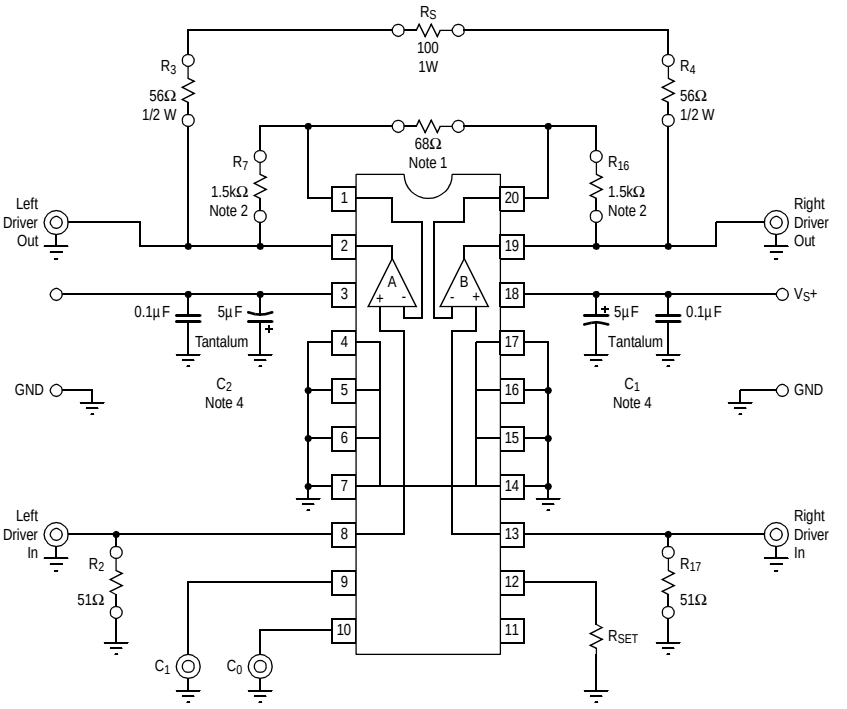
24-Pin LPP Power Dissipation and Thermal Resistance Using JEDEC JESD51-7-High Effective Thermal Conductivity (4-Layer) Test Board, LPP
Exposed Diepad Soldered to PCB per JESD51-5



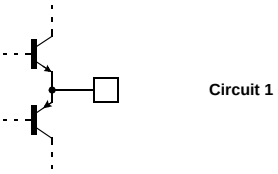
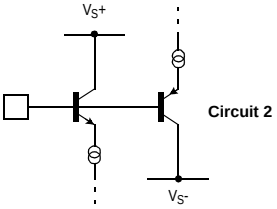
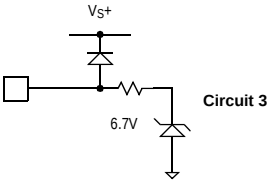
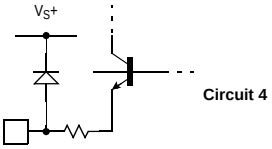
EL1503C

High Power Differential Line Driver

Test Circuit



Pin Description

20-Pin SO	24-Pin LPP	Pin Name	Function	Circuit
1	23	V_{IN}-A	Channel A Inverting Input	 Circuit 1
2	24	V_{OUT}A	Channel A Output	(Reference Circuit 1)
3	3	V_S-	Negative Supply	
4, 5, 6, 7	7	GND	Ground Connection	
8	8	V_{IN}+A	Channel A Non-Inverting Input	 Circuit 2
9	9	C1	Current Control Bit 1	 Circuit 3
10	10	C0	Current Control Bit 0	(Reference Circuit 3)
11	1, 2, 4, 5, 6, 14, 15, 16, 18, 19, 22	NC	Not Connected	
12	11	I_{ADJ}	Supply Current Control Pin	 Circuit 4
13	12	V_{IN}+B	Channel B Non-Inverting Input	(Reference Circuit 2)
14, 15, 16, 17	13	GND	Ground Connection	
18	17	V_S+	Positive Supply	
19	20	V_{OUT}B	Channel B Output	(Reference Circuit 1)
20	21	V_{IN}-B	Channel B Inverting Input	(Reference Circuit 1)

EL1503C

High Power Differential Line Driver

Applications Information

The EL1503C consists of two high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 4MHz and produce low distortion levels. A typical interface circuit is shown in Figure 1.

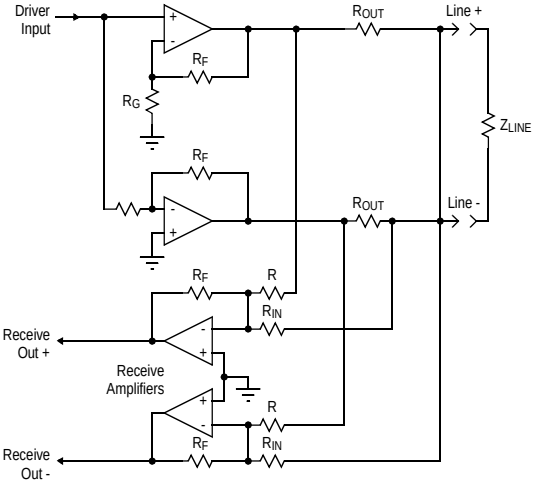


Figure 1. Typical Line Interface Connection

The amplifiers are wired with one in positive gain and the other in a negative gain configuration to generate a differential output for a single-ended input. They will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver.

If a differential signal is available to the drive amplifiers, they may be wired so:

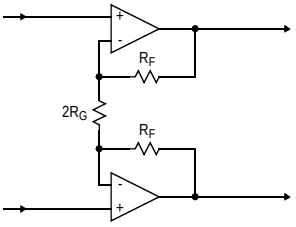


Figure 2. Drivers Wired for Differential Input

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further,

DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The EL1503C amplifiers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100 nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4" of unshielded wiring, or 6" of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Power Supplies & Dissipation

Due to the high power drive capability of the EL1503C, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the EL1503C has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the EL1503C is not constant with varying outputs. In reality, 7mA of the 12.5mA needed to power each driver is converted in to output current. Therefore, in the equation below we should subtract the average output current, I_O, or 7mA, whichever is the lowest. We'll call this term I_X.

Therefore, we can determine a quiescent current with the equation:

$$P_{Dquiescent} = V_S \times (I_S - 2I_X)$$

where:

V_S is the supply voltage (V_S+ to V_S-),

I_S is the maximum quiescent supply current (I_S+ + I_S-)

I_X is the lesser of I_O or 7mA (generally I_X = 7mA)

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage required from the EL1503C is close to the maximum available output swing. There is a trade of however with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with the following equation:

$$P_{Dtransistors} = 2 \times \overline{I_O}\left(\frac{V_S}{2} - \overline{V_O}\right)$$

where:

V_S is the supply voltage (V_S+ to V_S-),

V_O is the average output voltage per channel

I_O is the average output current per channel

The overall power dissipation (P_{DISS}) is obtained by adding $P_{Dquiescent}$ and $P_{Dtransistor}$.

Then, the θ_{JA} requirement needs to be calculated. This is done using the equation:

$$\theta_{JA} = \frac{(T_{JUNCT} - T_{AMB})}{P_{DISS}}$$

where:

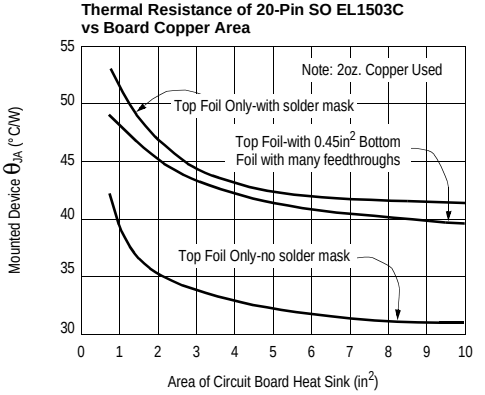
T_{JUNCT} is the maximum die temperature (150°C)

T_{AMB} is the maximum ambient temperature

P_{DISS} is the dissipation calculated above

θ_{JA} is the junction to ambient thermal resistance for the package when mounted on the PCB

This θ_{JA} value is then used to calculate the area of copper needed on the board to dissipate the power. The graph below shows various θ_{JA} for different board areas.



Single Supply Operation

The EL1503C can also be powered from a single supply voltage. When operating in this mode, the GND pins can still be connected directly to GND. To calculate power dissipation, the equations in the previous section should be used, with V_S equal to half the supply rail.

EL1503C PCB Design

A separate application note details the 24-pin LPP PCB design considerations. The 20-pin SO Power Package is designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JA}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask should be cut away from the EL1503C to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

Output Loading

While the drive amplifiers can output in excess of 500mA transiently, the internal metallization is not designed to carry more than 100mA of steady DC current and there is no current-limit mechanism. This allows safely driving rms sinusoidal currents of 2 x 100mA, or 200mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Power Supplies

The power supplies should be well bypassed close to the EL1503C. A 3.3µF tantalum capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1503C demonstration board, and documentation can be obtained from the factory.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency

response (1 dB peaking) for different supply voltages and gains:

Optimum Driver Feedback Resistor for Various Gains and Supply Voltages

Supply Voltage	Driver Voltage Gain		
	2.5	5	10
±5V	**2.7K**	**2.2K**	**2.0K**
±12V	**2.2K**	**1.6K**	**1.4K**

Power Control Function

The EL1503C contains two forms of power control operation. Two digital inputs, C0 and C1, can be used to control the supply current of the EL1503C drive amplifiers. As the supply current is reduced, the EL1503C will start to exhibit slightly higher levels of distortion and the frequency response will be limited. The 4 power modes of the EL1503C are set up as shown in the table below

Power Modes of the EL1503C

C1	C0	Operation
0	0	I_S Full Power Mode (CO or CP)
0	1	2/3 I_S Power Mode (CO or CP)
1	0	1/3 I_S Terminate only mode
1	1	Power down

Another method for controlling the power consumption of the EL1503C is to connect a resistor from the I_{ADJ} pin to ground. When this pin is grounded (the normal state), the supply current per channel is as per the specifications table on page 2. When a resistor is inserted, the supply current is scaled according to the "R_{SET} vs I_S" graphs on page 7 in the Performance Curves section.

Both methods of power control can be used simultaneously. In this case, positive and negative supply currents (per amp) are given by the equations below:

$$I_S+ = 1mA + (\overline{C_1} \times 2/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)} + (\overline{C_0} \times 1/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)}$$

$$I_S- = 0 + (\overline{C_1} \times 2/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)} + (\overline{C_0} \times 1/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)}$$

EL1503C

High Power Differential Line Driver

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