élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1502C

High Power Differential Line Driver/Receiver

Features

- Complete ADSL differential driver and receiver
- $54V_{p-p}$ output drive into 100Ω differential
- $50V_{p-p}$ output drive into 50Ω differential
- Driver $2^{nd}/3^{rd}$ harmonics of -70dBc/-75dBc at $2V_{p-p}$ into 100Ω
- Low supply current - 12.5mA per drive amplifier and 5mA per receive amplifier
- Standard surface-mount package

Applications

- ADSL line driver
- HDSL2 line driver
- Video distribution amplifier

Ordering Information

Part No	Temp. Range	Package	Outline #
EL1502CM	-40°C to +85°C	20-Lead SO	MDP0027

General Description

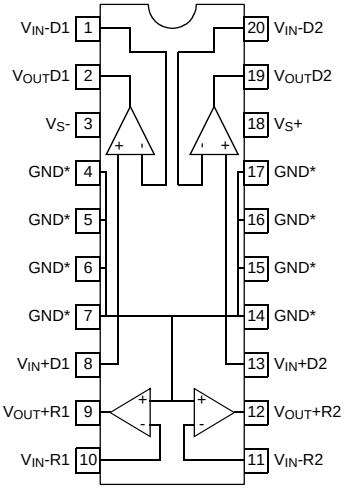
The EL1502C is a complete transceiver solution for high speed data transmission over twisted pair wires. It contains two wideband, high-voltage drivers and two low-noise receive amplifiers. The EL1502C is ideally suited for both ADSL and HDSL2 applications, in which it can supply a $50V_{p-p}$ signal into a 50Ω differential load while exhibiting very low distortion. The receive amplifiers also have very low distortion and low-noise for superior reception of small signals.

The line drivers of the EL1502C are current-feedback type amplifiers, which achieve a high slew rate while consuming moderate power. They retain their frequency response over a wide range of externally set gains. The receive amplifiers are of the voltage-feedback type and can be used to implement a hybrid coupler or filter functions using external passive components.

The EL1502C operates on ±5V to ±15V supplies. It retains its bandwidth and linearity over the complete supply range.

The device is supplied in a standard form factor, 20-pin SOIC package. The eight center package pins of the package are used as ground connections and heat spreaders, allowing for operation up to the maximum ambient temperature of 85°C.

Connection Diagrams



20-Pin Wide Body SOIC

* Gnd pins are heat spreaders

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Absolute Maximum Ratings (T_A = 25 °C)

Values beyond absolute maximum ratings can cause the device to be pre-maturely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_S+ to V_S- Supply Voltage	33V
V_S+ Voltage to Ground	-0.3V to +33V
V_S- Voltage to Ground	-33V to 0.3V
Driver V_{IN}+ Voltage	V_S- to V_S+
Current into any Input	8 mA
Output Current from Driver (Static)	100 mA
Output Current from Receiver (Static)	15 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-60°C to +150°C
Operating Junction Temperature-	40°C to +150°C
Maximum Power Dissipation	See Curves
ESD Rating	2kV

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

V_S = ±15V, R_F (drivers and receivers) =1.5kΩ, R_L(driver) = 65Ω, R_L(receiver) =200Ω. T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Conditions	Min	Typ	Max	Units
Supply Characteristics						
I_S+	Positive Supply Current	All Outputs at 0V	30	36	45	mA
I_S-	Negative Supply Current	All Outputs at 0V	-43	-34	-27	mA
Driver Input Characteristics						
V_{OS}	Input Offset Voltage		-30		30	mV
ΔV_{OS}	V_{OS} Mismatch		-10		10	mV
I_B+	Non-Inverting Input Bias Current		-10		10	µA
I_B-	Inverting Input Bias Current		-40		40	µA
ΔI_B-	I_B- Mismatch		-20		20	µA
R_{OL}	Transimpedance,	V_{OUT} from -12V to +12V	0.4	1.6		MΩ
e_N	Input Noise Voltage			3.3		nV/√Hz
i_N	-Input Noise Current			18		pA/√Hz
Driver Output Characteristics						
V_{OUT}	Loaded Output Swing	RL = 65Ω	±13.3	±13.6		V
		RL = 22Ω	±12	±12.7		V
I_{OUT}	Output Current	V_{OUT} = 1V, R_L = 1Ω		1		A
Driver Dynamic Performance						
BW	-3 dB Bandwidth	A_V = +5		80		MHz
HD2	2nd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{p-p}$		-70		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = $2V_{p-p}$		-67		dBc
HD3	3rd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{p-p}$		-75		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = $2V_{p-p}$		-73		dBc
SR	Slewrate	V_{OUT} from -10V to +10V Measured at ±5V	800	1200		V/µsec
Receiver Input Characteristics						
V_{OS}	Input Offset Voltage		-10		10	mV
ΔV_{OS}	V_{OS} Mismatch		-10		10	mV

Electrical Characteristics

V_S = ±15V, R_F (drivers and receivers) =1.5kΩ, R_L(driver) = 65Ω, R_L(receiver) =200Ω. T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Conditions	Min	Typ	Max	Units
I_B-	Input Bias Current		-7		-1	µA
AV_{OL}	Open Loop Gain		4000	10000		V/V
e_N	Input Noise Voltage			4.3		nV/√Hz
Receiver Output Characteristics						
V_{OUT}	Loaded Output Swing		±10	±12		V
I_{OUT}	Output Current			40		mA
Receiver Dynamic Performance						
BW	-3 dB Bandwidth	A_V = -2		70		MHz
HD2	2nd Harmonic Distortion	f_C = 1MHz, R_L = 500Ω,V_{OUT} = $2V_{p-p}$		-71		dBc
HD3	3rd Harmonic Distortion	f_C = 1MHz, R_L = 500Ω,V_{OUT} = $2V_{p-p}$		-70		dBc
SR	Slewrate	V_{OUT} from -4V to +4V Measured at ±2.5V	50	75		V/µsec

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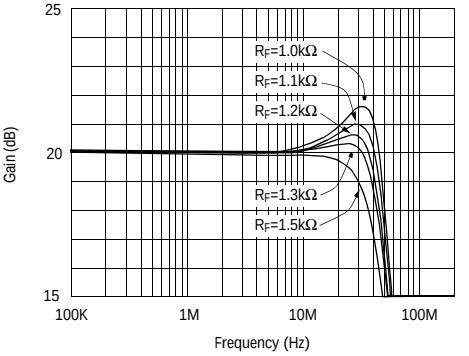
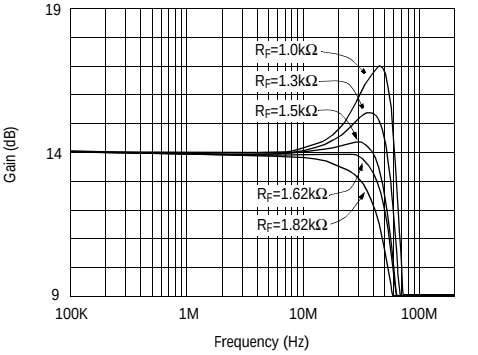
Performance Curves

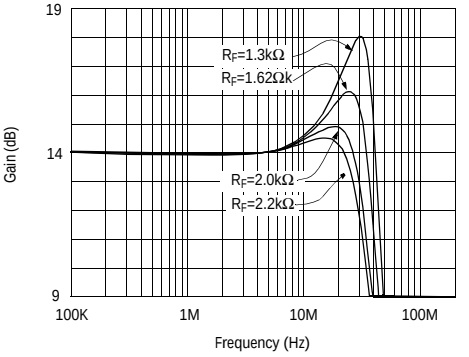
Driver Differential Frequency Response vs R_F
V_S=±15V, A_V=10, R_L=100Ω



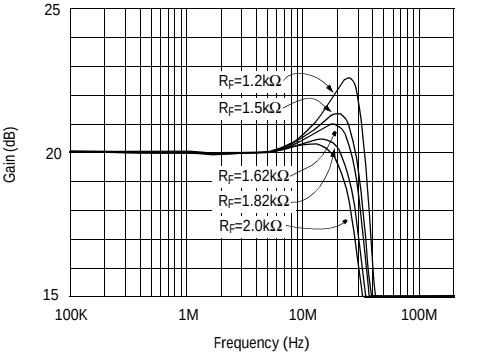
Driver Differential Frequency Response vs R_F
V_S=±15V, A_V=5, R_L=100Ω



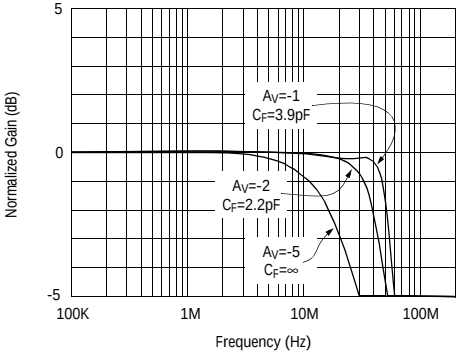
Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=5, R_L=100Ω



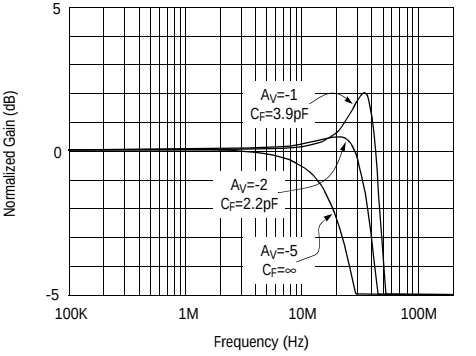
Driver Differential Frequency Response vs R_F
V_S=±5V, A_V=10, R_L=100Ω



Normalized Receiver Frequency Response vs Gain at
V_S=±15V, R_L=200Ω, C_L=10pF, R_F=1kΩ

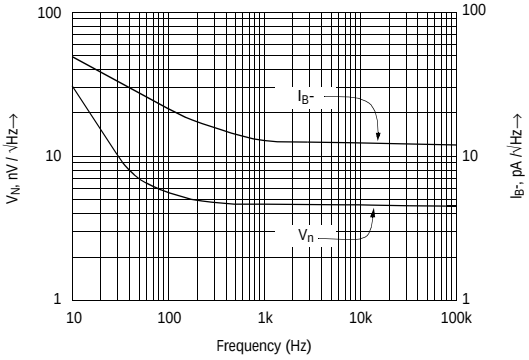


Normalized Receiver Frequency Response vs Gain at
V_S=±5V, R_L=200Ω, C_L=10pF, R_F=1kΩ

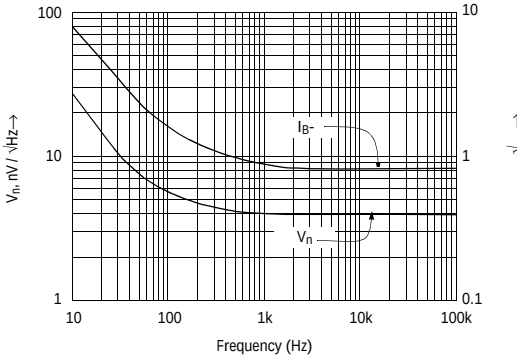


Performance Curves (cont.)

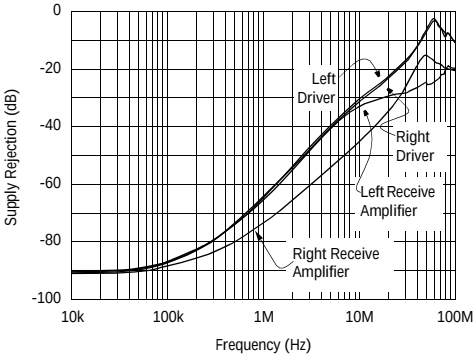
Driver Input Voltage and Feedback Current Noise vs Frequency



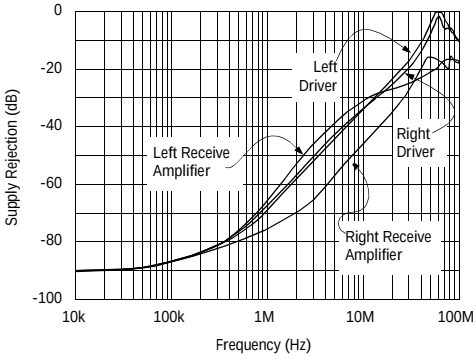
Receiver Amplifier Input Voltage and Feedback Current Noise vs Frequency



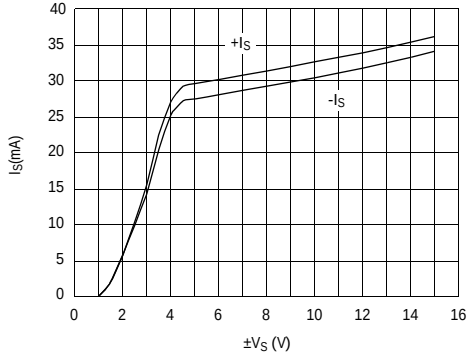
Negative Supply Rejection



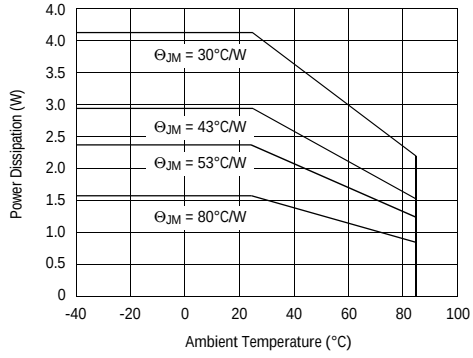
Positive Supply Rejection



Supply Current vs Supply Voltage



Power Dissipation vs Ambient Temperature for Various Mounted Θ_{JM}'s



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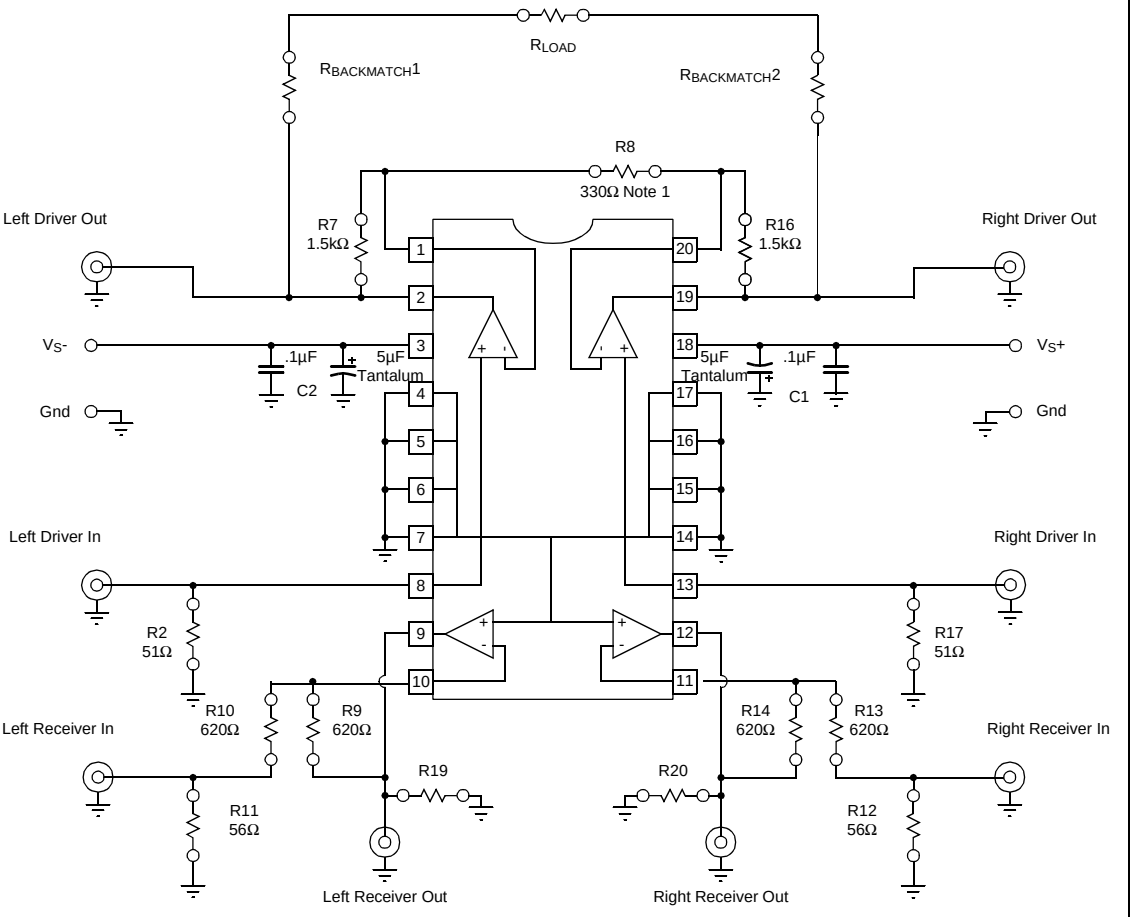
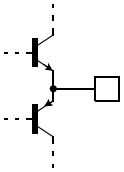
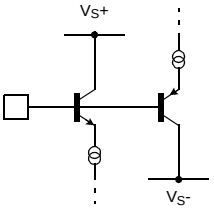
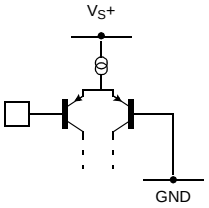
Test Circuit



Pin Description

EL1502C	Pin Name	Function	Circuit
1	V_{IN}-D1	Inverting Input Driver 1	 Circuit 1
2	V_{OUT}D1	Output of Driver 1	(Reference Circuit 1)
3	V_S-	Negative Supply	
4-7	GND	Ground Connection	
8	V_{IN}+D1	Non-Inverting Input Driver 1	 Circuit 2
9	V_{OUT}+R1	Output of Receive Channel 1	(Reference Circuit 1)
10	V_{IN}-R1	Non-Inverting Input Receiver l	 Circuit 3
11	V_{IN}-R2	Non-Inverting Input Receiver 2	(Reference Circuit 3)
12	V_{OUT}+R2	Output of Receiver 2	(Reference Circuit 1)
13	V_{IN}+D2	Non-Inverting Input Driver 2	(Reference Circuit 2)
14-17	GND	Ground Connection	
18	V_S+	Positive Supply	
19	V_{OUT}D2	Output of Driver 2	(Reference Circuit 1)
20	V_{IN}-D2	Inverting Input Driver 2	(Reference Circuit 1)

EL1502C

High Power Differential Line Driver/Receiver

Applications Information

The EL1502C consists of two power line drivers and two receiver amplifiers that can be connected for full duplex differential line transmission and reception. The amplifiers are designed to be used with signals up to 4 MHz and produce low distortion levels. A typical interface circuit is shown in Figure 1.

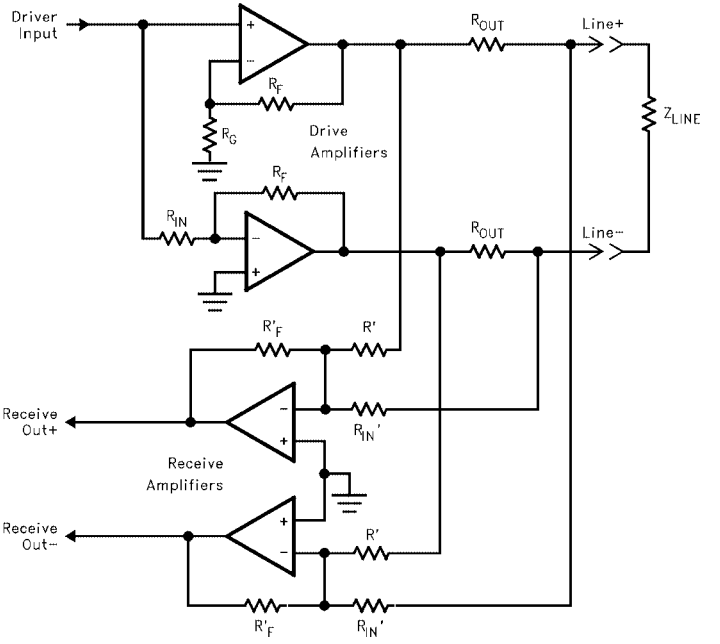


Figure 1. Typical Line Interface Connection

The drive amplifiers above are wired with one in positive gain and the other in a negative gain configuration to generate a differential output for a single-ended input. The drivers will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver.

The receiver amplifiers are wired as a hybrid coupler in the circuit. They reject the drivers' output signal (to the matching accuracy of the line impedance and resistors) while passing the signal coming from the line. Their outputs are still differential signals and can be converted to single-ended form by using a wideband instrumentation amplifier such as the EL4430. In a simplistic analysis we set $R_{OUT} = Z_{LINE}/2$ and $R' = 2*R_{IN}'$. Signals coming in from the line convert to currents through the R_{IN}'s and pass through the receive amplifiers. Driver outputs pass through the R' resistors and produce signal currents, but they are cancelled by opposite-polarity currents through the R_{IN}' resistors.

The actual value of R_{OUT} is increased from $Z_{LINE}/2$ to make its value in parallel with R_{IN}' equal to $Z_{LINE}/2$ and better match the line. For proper hybrid balance, R' is increased to compensate for R_{OUT}'s adjustment. For $Z_{LINE} = 130\Omega$ and $R_{IN}' = 510\Omega$, we set $R_{OUT} = 74.5\Omega$ and $R' = 1.17\ k\Omega$.

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For operating frequencies below 1 MHz, or in cases where the hybrid rejection of the drive signal is not very critical, the receive amplifiers can be wired to provide a single-ended hybrid coupler output:

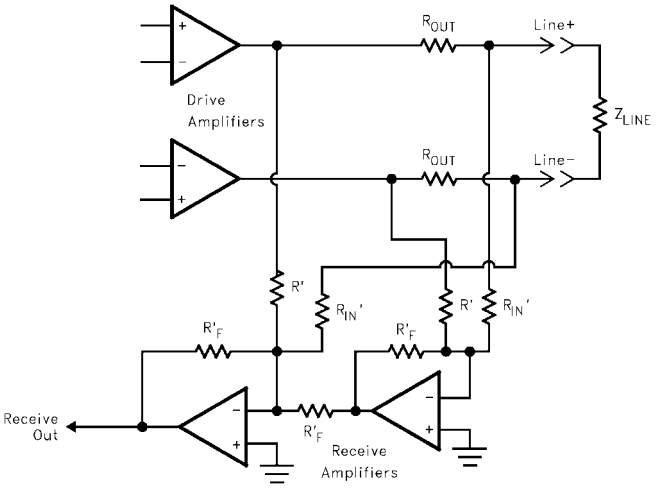


Figure 2. Receive Amplifiers Providing Hybrid and Differential Conversion

Common-mode rejection is as good as resistor and line impedance match, as before, but there is a 4ns time mismatch due to cascading the receive amplifiers. Thus, rejection of common-mode interference will degrade above 1 MHz.

If a differential signal is available to the drive amplifiers, they may be wired so:

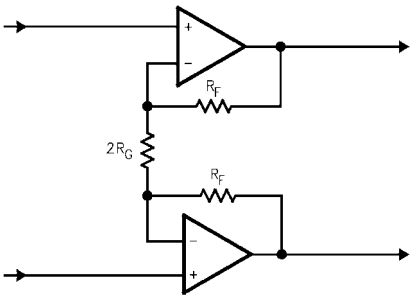


Figure 3. Drivers Wired for Differential Input

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The drivers and receivers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100 nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4" of unshielded wiring, or 6" of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Power Supplies & Dissipation

Due to the high power drive capability of the EL1502C, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the EL1502C has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the EL1502C is not constant. In reality, 7mA of the 12.5mA needed to power each driver, is converted in to output current. Therefore, in the equation below we should subtract the average output current, I_O, or 7mA, whichever is the lowest. We'll call this term I_X.

Therefore, we can determine a quiescent current with the equation:

$$P_{Dquiescent} = V_S \times (I_S - 2I_X)$$

where:

V_S is the supply voltage (V_S+ to V_S-),

I_S is the maximum quiescent supply current and

I_X is the lesser of I_O or 7mA (Generally I_X = 7mA).

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage on the line is equivalent to the peak minimum peak voltage available from the EL1502C. There is a trade of however with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with the following equation:

$$P_{Dtransistors} = 2 \times \overline{I_O}\left(\frac{V_S}{2} - \overline{V_O}\right)$$

where:

V_S is the supply voltage (V_S+ to V_S-),

V_O is the average output voltage per channel and

I_O is the average output current per channel.

The overall power dissipation (P_{DISS}) is obtained by adding $P_{Dquiescent}$ and $P_{Dtransistor}$.

Then, the θ_{ja} requirement needs to be calculated. This is done using the equation:

$$\theta_{ja} = \frac{(T_{MAX} - T_{AMB})}{P_{DISS}}$$

where:

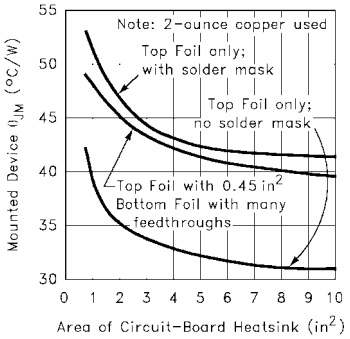
T_{MAX} is the maximum die temperature (150°C)

T_{AMB} is the maximum ambient temperature and

P_{DISS} is the dissipation calculated above.

This θ_{ja} value is then used to calculate the area of copper needed on the board to dissipate the power. The graph below shows various θ_{ja} for different board areas.

Thermal Resistance of EL1502C vs Copper Area



Single Supply Operation

The EL1502C can also be powered from a single supply voltage. When operating in this mode, the GND pins must be biased at the halfway voltage point. Due to a variation in the positive and negative supply current however, the two resistors needed to generate this point are not of equal value. The supply current on the negative pin requires 2mA less than that of the positive supply.i.e. the GND pins source 2mA.

EL1502C PCB Design

The 20-lead SO Power Package is designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JM}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask should be cut away from the EL1502C to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

Output Loading

While the drive amplifiers can output in excess of 500 mA transiently, the internal metallization is not designed to carry more than 100 mA of steady DC current and there is no current-limit mechanism. This allows safely driving rms sinusoidal currents of 2 x 100 mA, or 200 mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25 pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Power Supplies

The power supplies should be well bypassed close to the EL1502C. A 3.3µF tantalum capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1502C demonstration board, and documentation can be obtained from the factory.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The receive amplifiers are connected in inverting mode and will produce a narrow range of characteristics, but the drivers can be used for a wide range of gains. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor

values that produce an optimal driver frequency response for different supply voltages and gains:

Optimum Driver Feedback Resistor for Various Gains and Supply Voltages

Supply Voltage	Driver Voltage Range		
	2.5	5	10
±5V	**2.7K**	**2.2K**	**2.0K**
±12V	**2.2K**	**1.6K**	**1.4K**
±15V	**2.0K**	**1.6K**	**1.5K**

EL1502C

High Power Differential Line Driver/Receiver

General Disclaimer

Specifications contained in this data sheet are in effect as of the publication date shown. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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October 12, 1999

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