

Features

- Pentium® II Compatible
- 5 bit DAC Controlled Output Voltage
- Greater than 90% Efficiency
- 4.5V to 12.6V Input Range
- Dual NMOS Power FET Drivers
- Fixed frequency, Current mode Control
- Adjustable Oscillator with External Sync. Capability
- Synchronous Switching
- Internal Soft Start
- User Adjustable Slope Compensation
- Pulse by Pulse Current Limiting
- 1% Output Accuracy
- Power Good Signal
- Output Power Down

Applications

- Pentium® II Voltage Regulation Modules (VRM's)
- PC Motherboards
- Synchronous Rectification

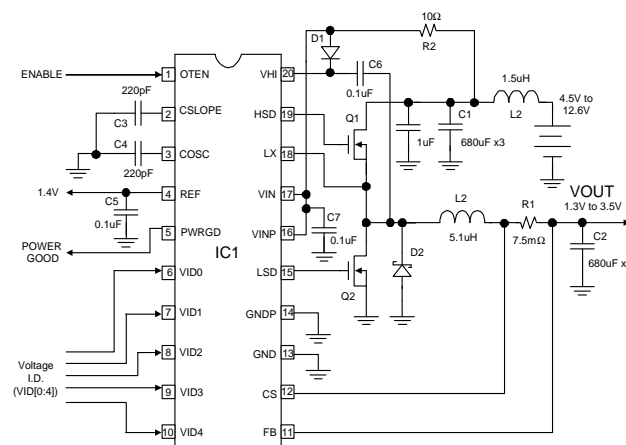
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7571C	0°C to +70°C	20-Pin SOIC	MDP0027

General Description

The EL7571C is a flexible, high efficiency, current mode, PWM step down controller. It incorporates five bit DAC adjustable output voltage control which conforms to the Intel Voltage Regulation Module (VRM) Specification for Pentium® II class processors. The controller employs synchronous rectification to deliver efficiencies greater than 90% over a wide range of supply voltages and load conditions. The on-board oscillator frequency is externally adjustable, or may be slaved to a system clock, allowing optimization of RFI performance in critical applications. For maximum flexibility, the control section may be powered from either 5V or 12V supplies. Additionally the high side FET driver supports boot strapped operation. Accordingly, system operation is possible from either a single 5V rail, a single 12V rail or dual supply rails with the controller operating from 12V and the power FET's from 5V.

Connection Diagram



Q1, Q2: Siliconix, Si4410, x 2

C1: United Chemi-Con, LXF16VB681M10X20LL, 680uF x 3

C2: United Chemi-Con, LXF16VB681M10X20LL, 680uF x 6

L1: Pulse Engineering, PE-53700, 5.1uH

L2: Micrometals, T30-26, 7T AWG #20, 1.5uH

R1: Dale, WSL-2512, 15mΩ, x 2

D1: BAV99

D2: IR, 32CTQ030

EL7571C

Programmable DC/DC Converter

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage:	-0.5V to 14V	Operating Temperature Range:	0°C to +70°C
Input Pin Voltage:	-0.3V below Ground, +0.3V above Supply	Operating Junction Temperature:	125°C
VHI	<27V	Peak Output Current:	3A
Storage Temperature Range:	-65°C to +150°C	Power Dissipation:	SOIC 500mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^\circ\text{C}$ and QA sample tested at $T_A = 25^\circ\text{C}$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^\circ\text{C}$ for information purposes only.

DC Electrical Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{V}$ unless otherwise specified

Parameter	Description	Condition	Min.	Typ.	Max.	Test Level	Units
V_{IN}	Input Voltage Range		4.5		12.6	I	V
V_{UVLO_HI}	Under Voltage Lockout High Threshold	Positive going input voltage	3.6	4	4.4	I	V
V_{UVLO_LO}	Under Voltage Lockout Low Threshold	Negative going input voltage	3.15	3.5	3.85	I	V
V_{OUT}	Output Voltage	See VID table	1.3		3.5	I	V
V_{REF}	Reference Voltage		1.386	1.4	1.414	I	V
V_{ILIM}	Current Limit Voltage	$V_{ILIM} = (V_{CS} - V_{FB})$	125	154	175	I	mV
V_{IREV}	Current Reversal Threshold	$V_{IREV} = (V_{CS} - V_{FB})$	-40	-5	15	I	mV
V_{PGH}	Power Good Upper Threshold	$V_{OUT} = 2.05\text{V}$	9.5	13	16.5	I	%
V_{PGL}	Power Good Lower Threshold	$V_{OUT} = 2.05\text{V}$	-16.5	-13	-9.5	I	%
V_{OTEN_LO}	Power Down Input Low Level	$I_{IN} = -10\mu\text{A}$	0		1.5	I	V
V_{OTEN_HI}	Power Down Input High Level		$(V_{IN} - 1.5)$		V_{IN}	I	V
V_{ID_LO}	Voltage I.D. Input Low Level		0		1.5	I	V
V_{ID_HI}	Voltage I.D. Input High Level		$(V_{IN} - 1.5)$		V_{IN}	I	V

Rev. 1A

Tuesday, April 01, 1997

EL7571C

Programmable DC/DC Converter

DC Electrical Characteristics

$T_A=25^{\circ}\text{C}$, $V_{IN}=5\text{V}$ unless otherwise specified

Parameter	Description	Condition	Min.	Typ.	Max.	Test Level	Units
V_{OSC}	Oscillator Voltage Swing			0.85		V	V
V_{PWRGD_LO}	Power Good Output Low Level	$I_{OUT}=1\text{mA}$			0.5	I	V
R_{DS_ON}	HSD, LSD Switch On-Resistance	$V_{IN}, V_{INP}=12\text{V}$, $I_{OUT}=100\text{mA}$, (VHI-LX)=12V		4.8	6	I	Ω
R_{FB}	FB Input Impedance			9.5		V	$k\Omega$
R_{CS}	CS Input Impedance			115		V	$k\Omega$
I_{VIN}	Quiescent Supply Current	$V_{OTEN} > (V_{IN}-0.5)\text{V}$		1.2	2	I	mA
$I_{VIN-DIS}$	Supply Current in Output Disable Mode	$V_{OTEN} < 1.5\text{V}$		0.76	1	I	mA
$I_{SOURCE/SINK}$	Peak Driver Output Current	$V_{IN}, V_{INP}=12\text{V}$, Measured at HSD, LSD, (VHI-LX)=12V		2.5		IV	A
I_{RAMP}	CSLOPE Ramp Current	High Side Switch Active	8.5	14	20	I	μA
I_{OSC_CHARGE}	Oscillator Charge Current	$1.2 > V_{OSC} > 0.35\text{V}$		50		V	μA
$I_{OSC_DISCHARGE}$	Oscillator Discharge Current	$1.2 > V_{OSC} > 0.35\text{V}$		2		V	mA
I_{REF_MAX}	VREF Output Current				25	IV	μA
I_{VID}	VID Input Pull up Current		3	5	7	I	μA
I_{OTEN}	OTEN Input Pull up Current		3	5	7	I	μA

AC Electrical Characteristics

$T_A=25^{\circ}\text{C}$, $V_{IN}=5\text{V}$ unless otherwise specified

Parameter	Description	Condition	Min.	Typ.	Max.	Test Level	Units
f_{OSC}	Nominal Oscillator Frequency	$C_{OSC}=330\text{pF}$	160	200	240	I	kHz
f_{CLK}	Clock Frequency		50	500	1000	IV	kHz
t_{OTEN}	Shutdown Delay	$V_{OTEN} > 1.5\text{V}$	100			V	ns
t_{SYNC}	Sync. Pulse Width		10		50	IV	ns
T_{START}	Soft Start Period	$V_{OUT}=3.5\text{V}$		$100/f_{CLK}$		V	μs
D_{MAX}	Maximum Duty Cycle			97		V	%

Rev. 1A

Tuesday, April 01, 1997

EL7571C

Programmable DC/DC Converter

Pin Description

Pin No.	Pin Name	Pin Type	Function
1	OTEN	I	Chip enable input, internal pull up (5 μ A typical). Active high.
2	CSLOPE	I	With a capacitor attached from CSLOPE to GND, generates the voltage ramp compensation for the PWM current mode controller. Slope rate is determined by an internal 14uA pull up and the CSLOPE capacitor value. V_{CSLOPE} is reset to ground at the termination of the high side cycle.
3	COSC	I	Multi-function pin: with a timing capacitor attached, sets the internal oscillator rate f_{CLK} ; when pulsed low for a duration t_{SYNC} synchronizes device to an external clock.
4	REF	O	Band gap reference output. Decouple to GND with 0.1uF.
5	PWRGD	O	Power good, open drain output. Set low whenever the output voltage is <i>not</i> within +/-10% of the programmed value.
6	VID0	I	Bit 0 of the output voltage select DAC. Internal pull up sets input high when not driven.
7	VID1	I	Bit 1 of the output voltage select DAC. Internal pull up sets input high when not driven.
8	VID2	I	Bit 2 of the output voltage select DAC. Internal pull up sets input high when not driven.
9	VID3	I	Bit 3 of the output voltage select DAC. Internal pull up sets input high when not driven.
10	VID4	I	Bit 4 of the output voltage select DAC. Internal pull up sets input high when not driven.
11	FB	I	Voltage regulation feedback input. Tie to VOUT for normal operation.
12	CS	I	Current Sense. Current feedback input of PWM controller and over current comparator input. Current Limit threshold set at +154mV with respect to FB. Connect sense resistor between CS and FB for normal operation.
1	GND	S	Ground
14	GNDP	S	Power ground for low side FET driver. Tie to GND for normal operation.
15	LSD	O	Low side gate drive output.
16	VINP	S	Input supply voltage for low side FET driver. Tie to VIN for normal operation.
17	VIN	S	Input supply voltage for control circuit.
18	LX	I	Negative supply input for high side FET driver.
19	HSD	O	High side gate drive output. Driver ground referenced to LX. Driver supply may be bootstrapped to enhance low controller input voltage operation.
20	VHI	I	Positive supply input for high side FET driver.

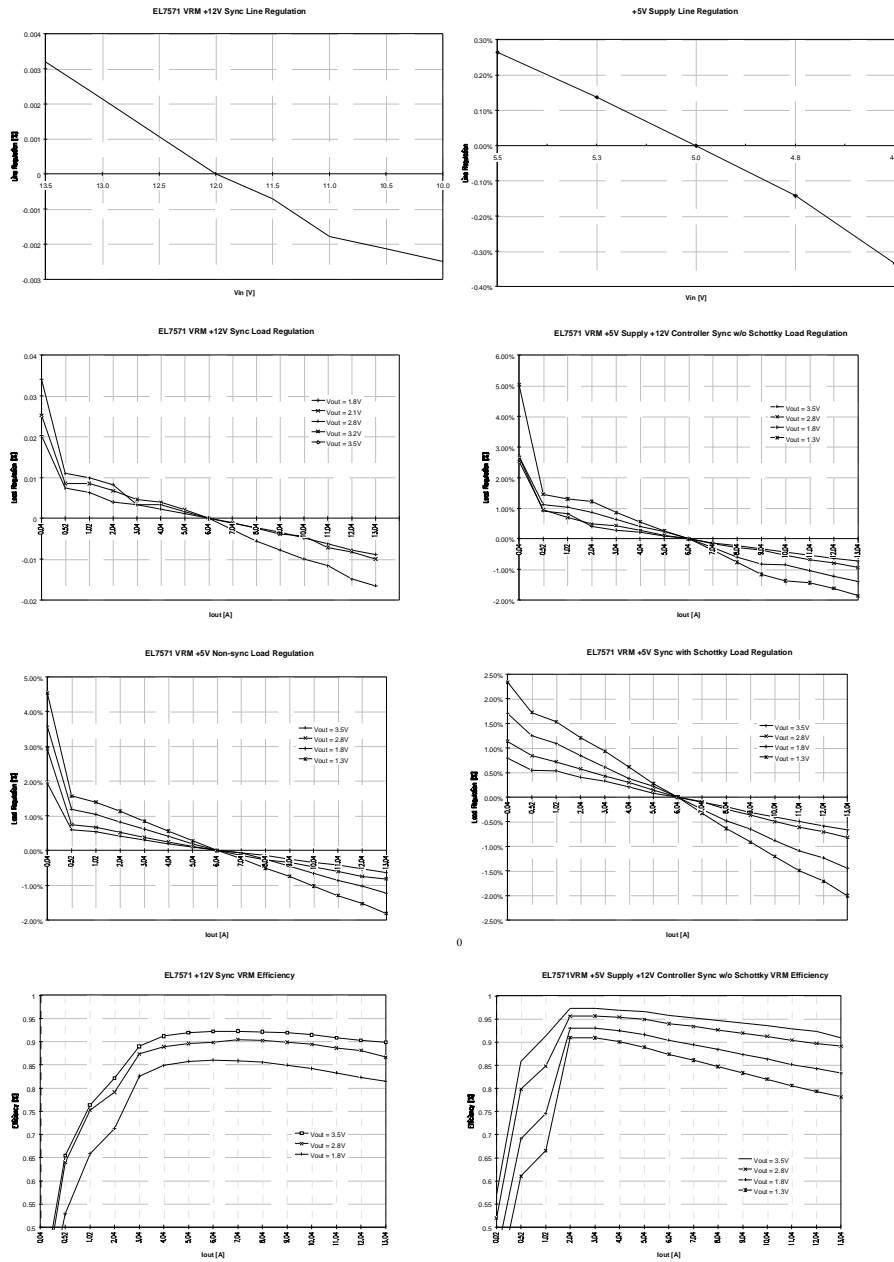
Rev. 1A

Tuesday, April 01, 1997

EL7571C

Programmable DC/DC Converter

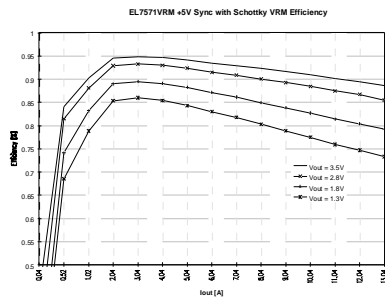
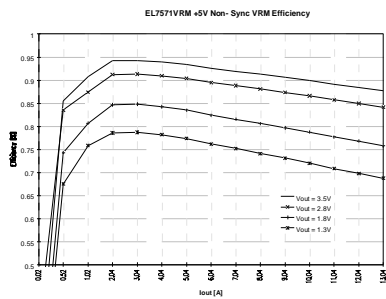
Typical Performance Curves - contact factory for additional curves



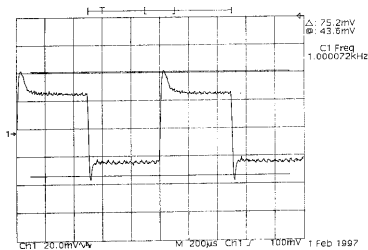
Rev. 1A
Tuesday, April 01, 1997

EL7571C

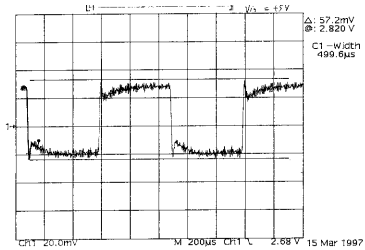
Programmable DC/DC Converter



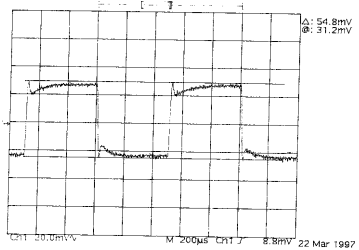
12V Transient Response



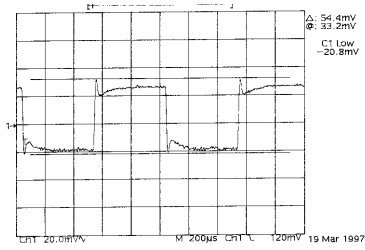
5V Non-sync Transient Response



5V Sync Transient Response



5V Input 12V Controller Trans. Resp.



Rev. 1A

Tuesday, April 01, 1997

Circuit Description

General

The EL7571 is a fixed frequency, current mode, pulse width modulated (PWM) controller with an integrated high precision reference and a 5 bit Digital-to-Analog Converter (DAC). The device incorporates all the active circuitry required to implement a synchronous step down (buck) converter which conforms to the Intel Pentium® II VRM specification. Complementary switching outputs are provided to drive dual NMOS power FET's in either synchronous or non-synchronous configurations, enabling the user to realize a variety of high efficiency and low cost converters.

Reference

A precision, temperature compensated band gap reference forms the basis of the EL7571. The reference is trimmed during manufacturing and provides 1% set point accuracy for the overall regulator. AC rejection of the reference is optimized using an external bypass capacitor (CREF).

Main Loop

A current mode PWM control loop is implemented in the EL7571. This configuration employs dual feedback loops which provide both output voltage and current feedback to the controller. The resulting system offers several advantages over traditional voltage control systems, including simpler loop design, pulse by pulse current limiting, rapid response to line variation and good load step response. Current feedback is performed by sensing voltage across an external shunt resistor. Selection of the shunt resistance value sets the level of current feedback and thereby the load regulation and current limit levels. Consequently, operation over a wide range of output currents is possible. The reference output is fed to a 5 bit DAC with step weighting conforming to the Intel VRM Specification. Each DAC input includes an internal current pull up which directly interfaces to the VID outputs of a Pentium® II class microprocessor. The heart of the controller is a triple-input direct summing differential comparator, which sums voltage feedback, current feedback and compensating ramp signals together.

The relative gains of the comparator input stages are weighted. The ratio of voltage feedback to current feedback to compensating ramp defines the load regulation and open loop voltage gain for the system, respectively. The compensating ramp is required to maintain large signal system stability for PWM duty cycles greater than 50%. Compensation ramp amplitude is user adjustable and is set with a single external capacitor (CSLOPE). The ramp voltage is ground referenced and is reset to ground whenever the high side drive signal is low. In operation, the DAC output voltage is compared to the regulator output, which has been internally attenuated. The resulting error voltage is compared with the compensating ramp and current feedback voltage. PWM duty cycle is adjusted by the comparator output such that the combined comparator inputs sum to zero. A weighted comparator scheme enhances system operation over traditional voltage error amplifier loops by providing cycle-by-cycle adjustment of the PWM output voltage, eliminating the need for error amplifier compensation. The dominant pole in the loop is defined by the output capacitance and equivalent load resistance, the effect of the output inductor having been canceled due to the current feedback. An output enable (OUTEN) input allows the regulator output to be disabled by an external logic control signal.

Auxiliary Comparators

The current feedback signal is monitored by two additional comparators which set the operating limits for the main inductor current. An over current comparator terminates the PWM cycle independently of the main summing comparator output whenever the voltage across the sense resistor exceeds 154mV. For a 7.5mΩ resistor this corresponds to a nominal 20A current limit. Since output current is continuously monitored, cycle-by-cycle current limiting results. A second comparator senses inductor current reverse flow. The low side drive signal is terminated when the sense resistor voltage is less than -5mV, corresponding to a nominal reverse current of -0.67A, for a 7.5mΩ sense resistor. Additionally, under fault conditions, with the regulator output over voltage, inductor current is prevented from ramping to a high level in the reverse direction. This prevents parasitic boost action of the local power supply when the fault is removed and potential damage to circuitry connected to the local

Rev. 1A

Tuesday, April 01, 1997

EL7571C

Programmable DC/DC Converter

supply.

Oscillator

A system clock is generated by an internal relaxation oscillator. Operating frequency is simple to adjust using a single external capacitor (COSC). The ratio of charge to discharge current in the oscillator is well defined and sets the maximum duty cycle for the system at around 96%.

Soft Start

During start up, potentially large currents can flow into the regulator output capacitors due to the fast rate of change of output voltage caused during start up, although peak inrush current will be limited by the over current comparator. However an additionally internal switch capacitor soft start circuit controls the rate of change of output voltage during start up by overriding the voltage feedback input of the main summing comparator, limiting the start up ramp to around 1ms under typical operating conditions. The soft start ramp is reset whenever the output enable (OUTEN) is reset or whenever the controller supply falls below 3.5V

Watchdog

A system watchdog monitors the condition of the controller supply and the integrity of the generated output voltage. Modern logic level power FET's rapidly increase in resistivity ($r_{ds_{on}}$) as their gate drive is reduced below 5V. To prevent thermal damage to the power FET's under load, with a reduced supply voltage, the system watchdog monitors the controller supply (VIN) and disables both PWM outputs (HSD, LSD) when the supply voltage drops below 3.5V. When the supply voltage is increased above 4V the watchdog initiates a soft start ramp and enables PWM operation. The difference between enable and disable thresholds introduces hysteresis into the circuit operation, preventing start up oscillation. In addition, output voltage is also monitored by the watchdog. As called out by the Intel Pentium® II VRM specification, the watchdog power good output (PWRGD) is set low whenever the output voltage differs from its selected value by more than +/-13%. PWRGD is an open drain output. A third watchdog function disables PWM output switching during over voltage fault

conditions, disabling both external FET drives, whenever the output voltage is greater than 13% of its' selected value, thereby anticipating reverse inductor current ramping and conforming to the VRM over voltage specification, which requires the regulator output to be disabled during fault conditions. Switching is enabled after the fault condition is removed.

Output Drivers

Complementary control signals developed by the PWM control loop are fed to dual NMOS power FET drivers via a level shift circuit. Each driver is capable of delivering nominal peak output currents of 2A at 12V. To prevent shoot through in the external FET's, each driver is disabled until the gate voltage of the complementary power FET has fallen to less than 1V. Supply connections for both drivers are independent, allowing the controller to be configured with a boot strapped high side drive. Employing this technique a single supply voltage may be used for both power FET's and controller. Alternatively, the application may be simplified using dual supply rails with the power FET's connected to a secondary supply voltage below the controller's, typically 12V and 5V. For applications where efficiency is less important than cost, applications can be further simplified by replacing the low side power FET with a Schottky diode, resulting in non-synchronous operation.

Applications Information

The EL7571 is designed to meet the Intel 5 bit VRM specification. Refer to the VID decode table for the controller output voltage range.

The EL7571 may be used in a number different converter topologies. The trade-off between efficiency, cost, circuit complexity, line input noise, transient response and availability of input supply voltages will determine which converter topology is suitable for a given application. The following table lists some of the differences between the various configurations:

Rev. 1A

Tuesday, April 01, 1997

Converter Topologies

Topology	Diagram	Efficiency	Cost	Complexity	Input Noise	Transient Response
5V only Non-synch	figure 1	92%	low	low	high	good
5V only Sync	figure 2	95%	high	moderate	high	good
5V & 12V Non-synch	figure 3	92%	lowest	lowest	high	good
5V & 12V Sync	figure 4	95%	high	moderate	high	good
12V only Sync	Connection Diagram	92%	high	moderate	low	fair

Circuit schematics and Bills of Material (BOM's) for the various topologies are provided at the end of the datasheet. If your application requirements differ from the included examples, the following design guide lines should be used to select the key component values. Refer to the front page connection diagram for component locations

Output Inductor, L1

Two key converter requirements may be used to determine inductor value:

- I_{min} - minimum output current; the current level at which the converter enters the discontinuous mode of operation (refer to application note #18 for a detailed discussion of discontinuous mode),
- I_{max} - maximum output current

Although many factors influence the choice of the inductor value, including efficiency, transient response and ripple current, one practical way of sizing the inductor is to select a value which maintains continuous mode operation, i.e. inductor current positive for all conditions. This is desirable to optimize load regulation and light load transient response. When the minimum inductor ripple current just reaches zero and with the mean ripple current set to I_{min} , peak inductor ripple current is twice I_{min} , independent of duty cycle. The minimum inductor value is given by:

$$L1_{min} = \frac{(V_{in} - V_{out}) \cdot T_{on}}{I_{peak}} = \frac{(V_{in} - V_{out}) \cdot V_{out}}{V_{in} \cdot f_{sw} \cdot 2 \cdot I_{min}}$$

Where:

I_{peak} = peak ripple

V_{in} = input voltage

V_{out} = output voltage

I_{min} = minimum load

t_{on} = top switch on time

f_{sw} = switching frequency

Since inductance value tends to decrease with current, ripple current will generally be greater than 2 I_{min} .

Once the minimum output inductance is determined, an off the shelf inductor with current rating greater than the maximum DC output current required can be selected. **Pulse Engineering** and **Coil Craft** are two manufacturers of high current inductors. For converter designers who want to design their own high current inductors, for experimental purposes or to further reduce cost, we recommend the **Micrometals Powdered Iron Cores** data sheet and applications note as a good reference and starting point.

Current Sense Resistor, R1

Inductor current is monitored indirectly via a low value resistor R1. The voltage developed across the current sense resistor is used to set the maximum operating current, the current reversal threshold and the system load regulation. There are two criteria for selecting the resistor value and type. Firstly, the

Rev. 1A

Tuesday, April 01, 1997

EL7571C

Programmable DC/DC Converter

minimum value is limited by the maximum output current. The EL7571 current limit comparator has a typical threshold of 154mV and 125mV minimum. When the voltage across the sense resistor exceeds this threshold, the conduction cycle of the top switch terminates immediately, providing pulse by pulse current limiting. A resistor value must be selected which guarantees operation under maximum load. That is:

$$R1 = \frac{V_{oc_min}}{I_{max}}$$

Where:

Voc_min = minimum over current voltage threshold

I_{max} = maximum output current

Secondly, since the load current passes directly through the sense resistor, its' power rating must be sufficient to handle the power dissipated during maximum load (current limit) conditions. Thus:

$$P_d = I_{max}^2 \cdot R1$$

Where:

P_d = power dissipated in current sense resistor

P_d must be less than the power rating of the current sense resistor. High current applications may require parallel sense resistors to dissipate sufficient power. Two popular current sense resistor are currently available: the WSL-2512 series of Power Metal Strip Resistors from **Dale Electronics** and **Magnann Copper** wire. The trade-off between the two types of resistors are cost, space, packaging and performance. Although Power Metal Strip Resistors are relatively expensive, they are available in surface mount packaging with tighter tolerances. Consequently less board space is used to achieve a more accurate current sense. Alternatively, Magnann copper wire has looser tolerance and higher parasitic inductance. This results in a less accurate current senses but at a much lower cost. Ultimately the selection of the type of current sense element must be made on an application by application basis.

Input Capacitor, C1

In a buck converter, where the output current is greater than 10A, significant demand is placed on the input capacitor. Under steady state operation, the

Rev. 1A

Tuesday, April 01, 1997

high side FET conducts current only when it is switched "on" and conducts zero current when it is turned "off". The result is a current square wave drawn from the input supply. Most of this input ripple current is supplied from the input capacitor C1. The current flow through C1's equivalent series resistance (ESR) can heat up the capacitor and cause premature failure. Maximum input ripple current occurs when the duty cycle is 50%, a current of I_{out}/2 RMS. Worst case power dissipation is:

$$P_d = \left(\frac{I_{out}}{2} \right)^2 \cdot ESR_{in}$$

Where:

ESR_{in} = input capacitor ESR

For safe and reliable operation, P_d must be less than the capacitor's data sheet rating.

Input Inductor, L2

The input inductor (L2) isolates switching noise, due to the buck converter input ripple current, from the input supply line. This inductor is critical in high current applications where the ripple current is similarly high. An excessively large input inductor degrades the converter's transient response by limiting the maximum rate of change of current at the converter input. A 1.5uH input inductor is sufficient in most applications.

Output Capacitor, C2

During steady state operation, output ripple current is much less than the input ripple current. Consequently output capacitor power dissipation is less of a concern than the input capacitor's. However, low ESR is still required for applications with very low output ripple voltage or tight transient response requirements. Output ripple voltage is given by:

$$V_{rip} = I_{rip} \cdot ESR_{out}$$

Where:

I_{rip} = output ripple current

ESR_{out} = output capacitor ESR

During a transient response, the output voltage spike is determined by the ESR and equivalent series inductance (ESL) of the output capacitor in addition to the rate of change and magnitude of the load current step. The output voltage transient is given by:

$$\Delta V_{out} = ESR_{out} \cdot \Delta I_{out} + ESL \cdot \frac{di}{dt}$$

Where:

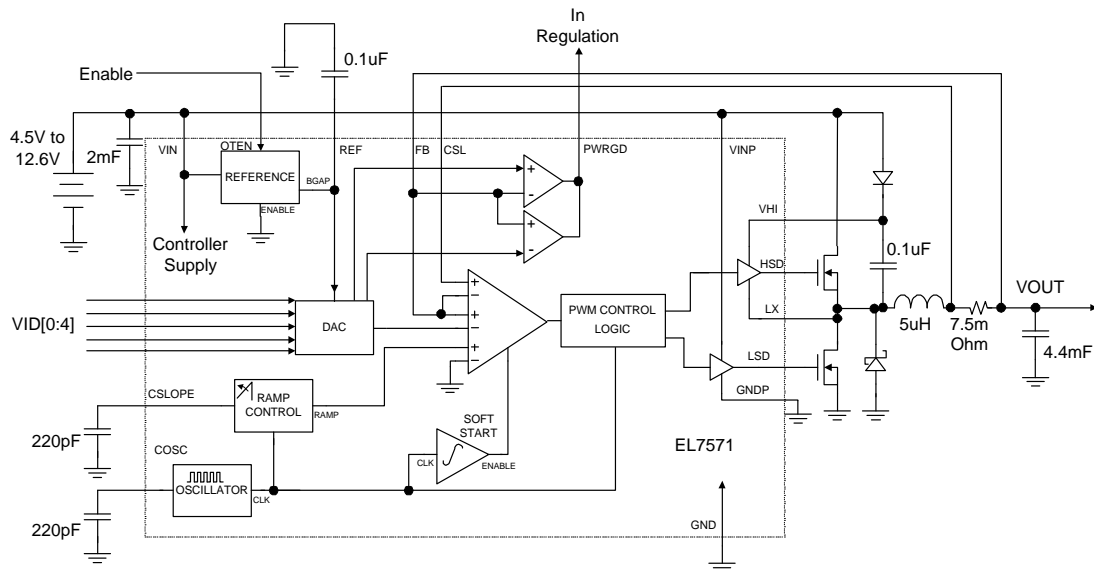
ESR_{out} = output capacitor ESR

ESL = output capacitor ESL

ΔI_{out} = output current step

di/dt = rate of change of output current

Block Diagram



Rev. 1A

Tuesday, April 01, 1997

EL7571C

Programmable DC/DC Converter

Voltage ID Code Output Voltage Settings

VID4	VID3	VID2	VID1	VID0	Vout
0	1	1	1	1	1.3
0	1	1	1	0	1.35
0	1	1	0	1	1.4
0	1	1	0	0	1.45
0	1	0	1	1	1.5
0	1	0	1	0	1.55
0	1	0	0	1	1.6
0	1	0	0	0	1.65
0	0	1	1	1	1.7
0	0	1	1	0	1.75
0	0	1	0	1	1.8
0	0	1	0	0	1.85
0	0	0	1	1	1.9
0	0	0	1	0	1.95
0	0	0	0	1	2.0
0	0	0	0	0	2.05
1	1	1	1	1	NO CPU
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

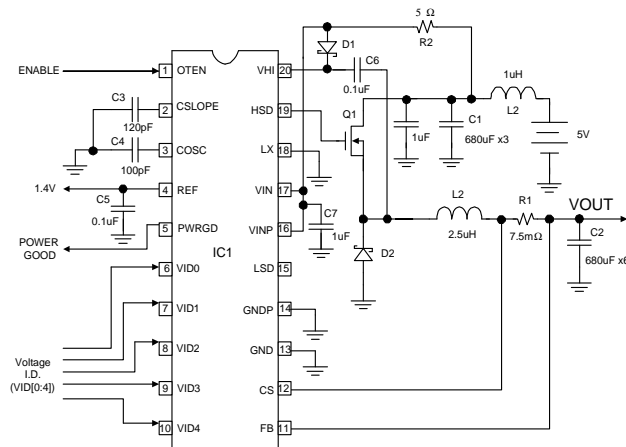
Application Circuits

To assist the evaluation of EL7571, several VRM applications have been developed. The boards may be configured to operate in a variety of modes. These are described in the converter topologies table in the datasheet. The 5V VRM can operate with either a 5V or 12V controller input to use a 5V supply and 5V power input with a 12V controller input. When a 5V power input is used with a 12V controller input, R3 must be inserted and the track connecting R2 and +5V supply cut. Additionally, the track connecting pin 18 to the output inductor must also be cut, and pin 18 connected to ground via a jumper from pin 18 to pin 14.

EL7571C

Programmable DC/DC Converter

Figure 1. 5V Input, Boot-Strapped Non-Synchronous DC-DC Converter



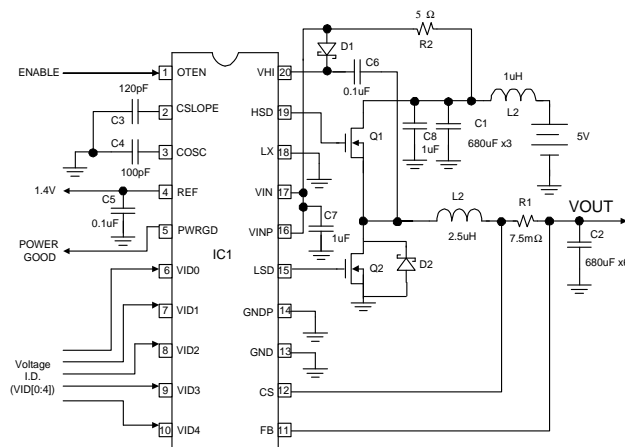
EL7571 5V VRM Bill of Materials - 5V Non Sync Solution

Component	Manufacturer	Part Number	Value	Units
C1	United Chemi-Con	LXF16VB681M10X20LL	680uF	3
C2	United Chemi-Con	LXF16VB681M10X20LL	680uF	6
C3		Chip Capacitors	120pF	1
C4		Chip Capacitors	100pF	1
C5, C6, C7		Chip Capacitor	0.1uF	3
D1	GI	Schottky diode, SS12GICT-ND	-	1
IC1	Elantec	EL7571CM	-	1
L1	Pulse Engineering	PE-53681	2.5uH	1
L2	Micrometals	T30-26, 7T AWG #20	1uH	1
R1	DALE	WSL-2512	15mΩ	2
R2		Chip Resistor	5Ω	1
D2	IR	IR32CTQ030	-	1
Q1	Siliconix	Si4410	-	2

EL7571C

Programmable DC/DC Converter

Figure 2. 5V Input Boot-Strapped Synchronous DC-DC Converter



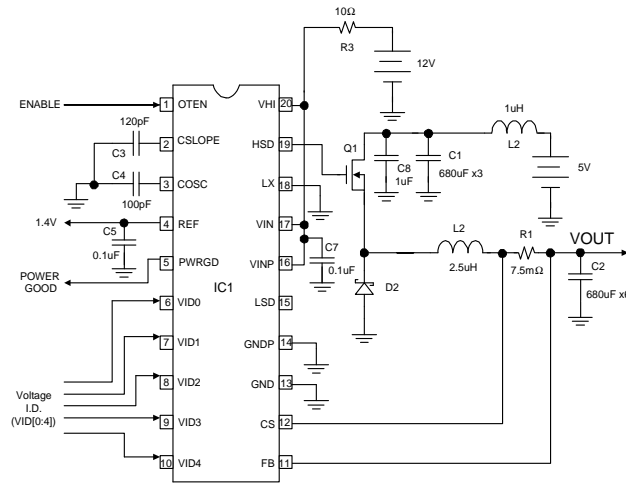
EL7571 5V VRM Bill of Materials - 5V Sync Solution

Component	Manufacturer	Part Number	Value	Units
C1	United Chemi-Con	LXF16VB681M10X20LL	680uF	3
C2	United Chemi-Con	LXF16VB681M10X20LL	680uF	6
C3		Chip Capacitor	120pF	1
C4		Chip Capacitors	100pF	1
C5, C6		Chip Capacitor	0.1uF	2
C7, C8		Chip Capacitor	1uF	2
D1	GI	Schottky Diode SS12GICT-ND		1
IC1	Elantec	EL7571CM	-	1
L1	Pulse Engineering	PE-53681	2.5uH	1
L2	Micrometals	T30-26, 7T AWG #20	1uH	1
R1	DALE	WSL-2512	15mΩ	2
R2		Chip Resistor	5Ω	1
D2	IR	32CTQ030		1
Q1, Q2	Siliconix	Si4410	-	2 each

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Programmable DC/DC Converter

Figure 3. 5V Input, 12V Controller, Non-Synchronous DC-DC Controller



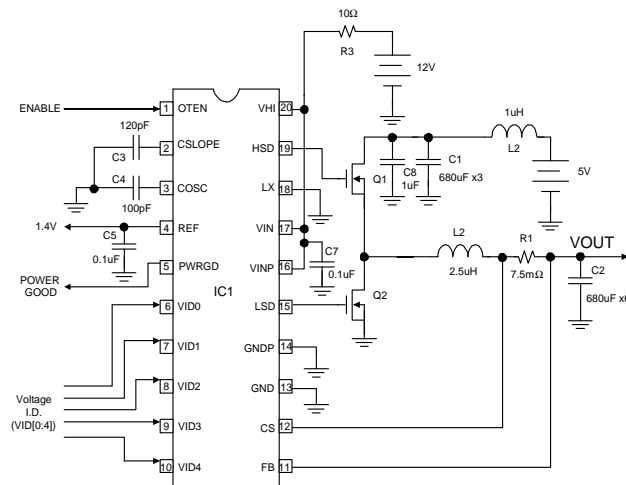
EL7571 5V VRM Bill of Materials - 5V Input, 12V Controller Non Sync Solution

Component	Manufacturer	Part Number	Value	Units
C1	United Chemi-Con	LXF16VB681M10X20LL	680uF	3
C2	United Chemi-Con	LXF16VB681M10X20LL	680uF	6
C3		Chip Capacitors	120pF	1
C4		Chip Capacitor	100pF	1
C5, C7		Chip Capacitor	0.1uF	2
C8		Chip Capacitor	1uF	1
IC1	Elantec	EL7571CM	-	1
L1	Pulse Engineering	PE-53681	2.5uH	1
L2	Micrometals	T30-26, 7T AWG #20	1uH	1
R1	DALE	WSL-2512	15mΩ	2
R3		Chip Resistor	10Ω	1
D2	IR	IR32CTQ030	-	1
Q1	Siliconix	Si4410	-	2

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Programmable DC/DC Converter

Figure 4. 5V Input, 12V Controller, Synchronous DC-DC Converter



EL7571 5V VRM Bill of Materials - 5V Input, 12V Controller Sync Solution

Component	Manufacturer	Part Number	Value	Units
C1	United Chemi-Con	LXF16VB681M10X20LL	680uF	3
C2	United Chemi-Con	LXF16VB681M10X20LL	680uF	6
C3		Chip Capacitor	120pF	1
C4		Chip Capacitor	100pF	1
C5, C7		Chip Capacitor	0.1uF	2
C8		Chip Capacitor	1uF	1
IC1	Elantec	EL7571CM	-	1
L1	Pulse Engineering	PE-53681	2.5uH	1
L2	Micrometals	T30-26, 7T AWG #20	1uH	1
R1	DALE	WSL-2512	15mΩ	2
R3		Chip Resistor	10Ω	1
Q1, Q2	Siliconix	Si4410	-	2 each