



1024Kx32 Static RAM CMOS, High Speed Module

FEATURES

- 1024Kx32 bit CMOS Static RAM
 - Access Times: 15, 20, and 25ns
 - Individual Byte Selects
 - Fully Static, No Clocks
 - TTL Compatible I/O
- High Density Package
 - 72 Pin ZIP, No. 175
 - 72 lead SIMM, No. 176 (Angle)
 - 72 lead SIMM, No. 356 (Straight)
 - Common Data Inputs and Outputs
- Single +3.3V (±10%) Supply Operation

DESCRIPTION

The EDI8F321024V is a high speed 32 megabit Static RAM module organized as 1024K by 32 bits. This module is constructed from eight 1024Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables ($\overline{E0}$ - $\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8F321024V is offered in a gold plated 72 pin ZIP and gold plated 72 lead SIMM packages, which enable 32 megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 3.3V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Pins PD0- PD3, are used to identify module memory density in applications where alternate modules can be interchanged.

FIG. 1

PIN CONFIGURATION AND BLOCK DIAGRAM

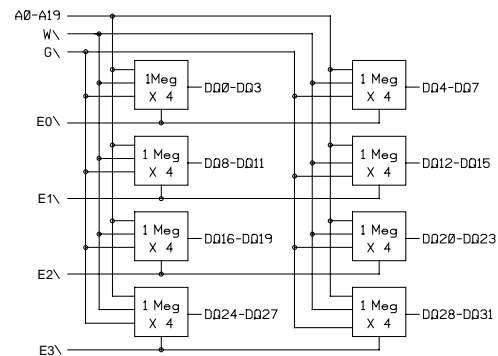
NC	□2	1	□NC
PD3	□4	3	□PD2
PD0	□6	5	□VSS
DQ0	□8	7	□PD1
DQ1	□10	9	□DQ8
DQ2	□12	11	□DQ9
DQ3	□14	13	□DQ10
VCC	□16	15	□DQ11
A7	□18	17	□A0
A8	□20	19	□A1
A9	□22	21	□A2
DQ4	□24	23	□DQ12
DQ5	□26	25	□DQ13
DQ6	□28	27	□DQ14
DQ7	□30	29	□DQ15
\overline{W}	□32	31	□VSS
A14	□34	33	□A15
$\overline{E0}$	□36	35	□E1
$\overline{E2}$	□38	37	□E3
A16	□40	39	□A17
VSS	□42	41	□G
DQ16	□44	43	□DQ24
DQ17	□46	45	□DQ25
DQ18	□48	47	□DQ26
DQ19	□50	49	□DQ27
A10	□52	51	□A3
A11	□54	53	□A4
A12	□56	55	□A5
A13	□58	57	□VCC
DQ20	□60	59	□A6
DQ21	□62	61	□DQ28
DQ22	□64	63	□DQ29
DQ23	□66	65	□DQ30
VSS	□68	67	□DQ31
A19	□70	69	□A18
NC	□72	71	□NC

PD0 AND PD2 = GROUND
PD1 AND PD3 = OPEN

8G321024V Pin Config.

PIN NAMES

A0-A19	Address Inputs
$\overline{E0}$ - $\overline{E3}$	Chip Enables
\overline{W}	Write Enable
\overline{G}	Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+3.3V±10%)
VSS	Ground
NC	No Connection



8G321024V Blk Dia.



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature TA (Ambient) Commercial.	0°C to +70°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	4.6 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	Vcc +0.3	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Typ	Max	Units
Operating Power Supply Current	ICC1	$\bar{W}, \bar{E} = \text{VIL}, I/O = 0\text{mA}, \text{Min Cycle}$			1280	mA
Standby (TTL) Power Supply Current	ICC2	$\bar{E} \geq \text{VIH}, \text{VIN} \leq \text{VIL} \text{ or } \text{VIN} \geq \text{VIH}$			480	mA
Full Standby Power Supply Current CMOS	ICC3	$\bar{E} \geq \text{VCC}-0.2\text{V}$ $\text{VIN} \geq \text{VCC}-0.2\text{V} \text{ or } \text{VIN} \leq 0.2\text{V}$			80	mA
Input Leakage Current	ILI	$\text{VIN} = 0\text{V to VCC}$	--	--	± 80	μA
Output Leakage Current	ILO	$\text{V I/O} = 0\text{V to VCC}$	--	--	± 20	μA
Output High Voltage	VOH	$\text{IOH} = -4.0\text{mA}$	2.4	--	--	V
Output Low Voltage	VOL	$\text{IOL} = 8.0\text{mA}$	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

TRUTH TABLE

\bar{E}	\bar{W}	\bar{G}	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2/ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	60	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	60	pF

These parameters are sampled, not 100% tested.



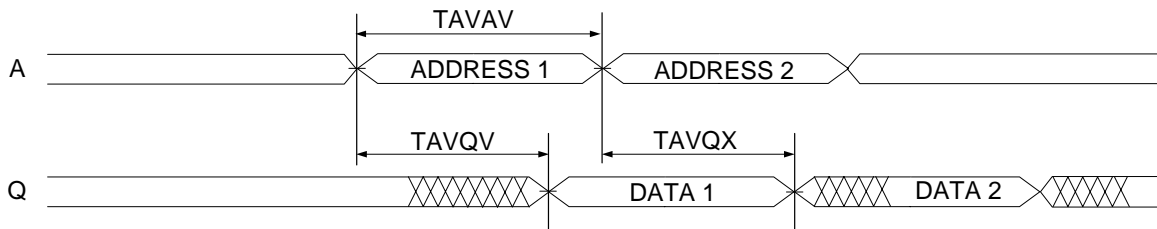
AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		15ns		25ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	15		25		20		ns
Address Access Time	TAVQV	TAA	15		25		20		ns
Chip Enable Access	TELQV	TACS	15		25		20		ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	7		10		10		ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE	7		8		8		ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	7		8		8		ns

Note 1: Parameter guaranteed, but not tested.

FIG. 2

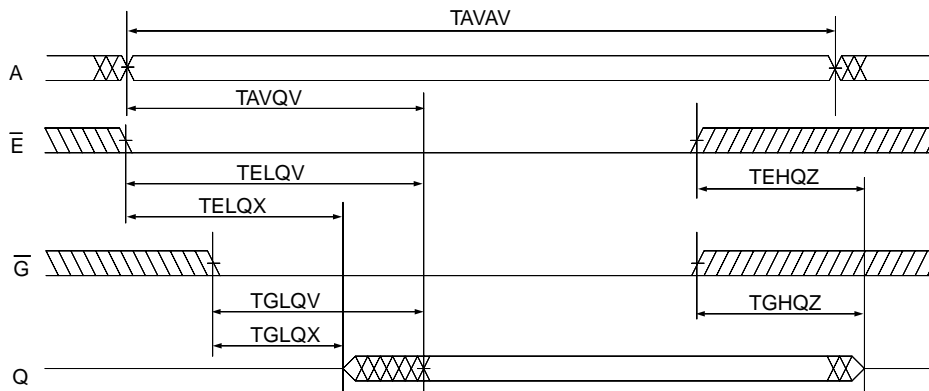
READ CYCLE 1 - \bar{W} HIGH, \bar{G} , \bar{E} LOW



8G321024V Rd Cyc1

FIG. 3

READ CYCLE 2 - \bar{W} HIGH



8G321024V Rd Cyc2



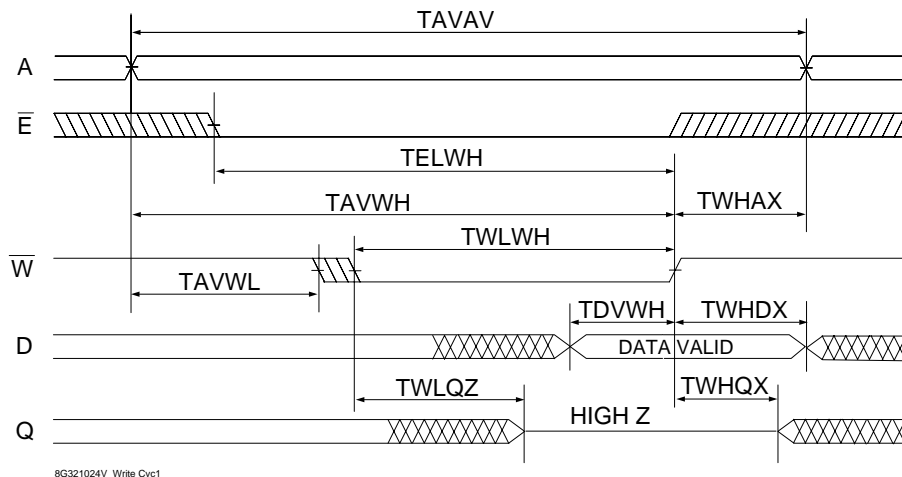
AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		15ns		25ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	15		25		20		ns
Chip Enable to End of Write	TELWH	TCW	10		15		15		ns
	TWLEH	TCW	10		15		15		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	10		15		15		ns
	TAVEH	TAW	10		15		15		ns
Write Pulse Width	TWLWH	TWP	12		15		15		ns
	TELEH	TWP	12		15		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TDH	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	7	0	9	0	8	ns
Data to Write Time	TDVWH	TDW	7		12		12		ns
	TDVEH	TDW	7		12		12		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

FIG. 4

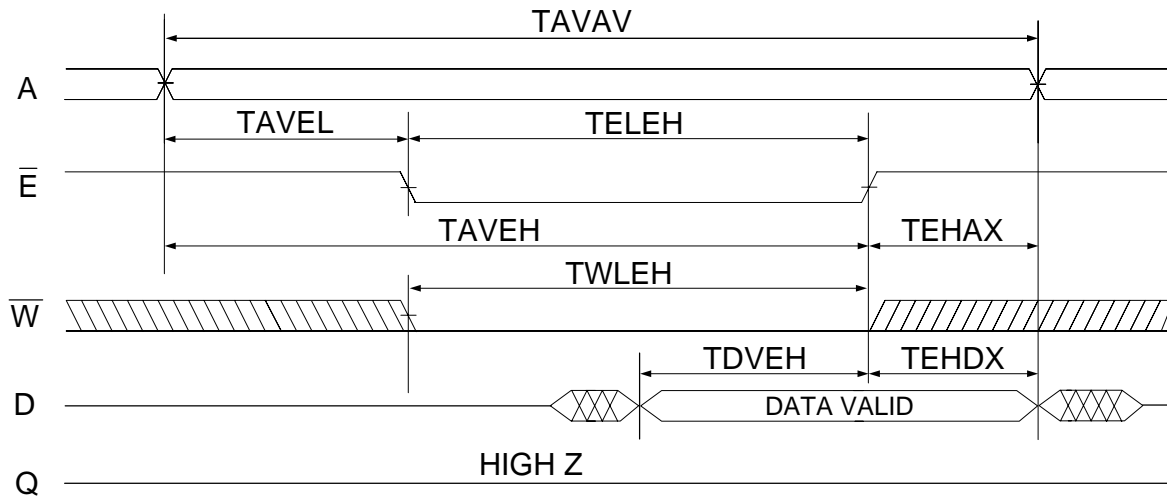
WRITE CYCLE 1 - \bar{W} CONTROLLED



8G321024V Write Cyc1



FIG. 5
WRITE CYCLE 2 - \bar{E} CONTROLLED



8G321024V Write Cyc2



ORDERING INFORMATION

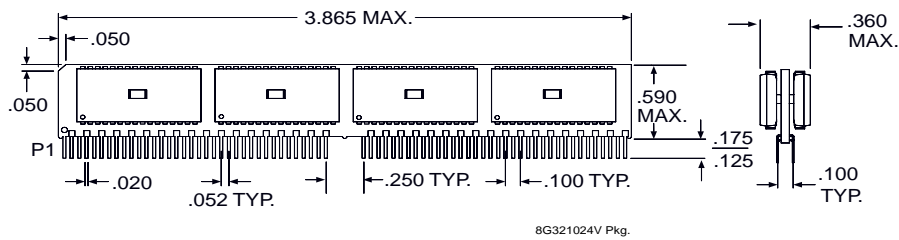
Part Number	Speed (ns)	Package No.
EDI8F321024V15MNC	15	176
EDI8F321024V25MNC	25	176
EDI8F321024V20MNC	20	176

Note: For gold SIMM option, change "EDIF" to "EDIG".

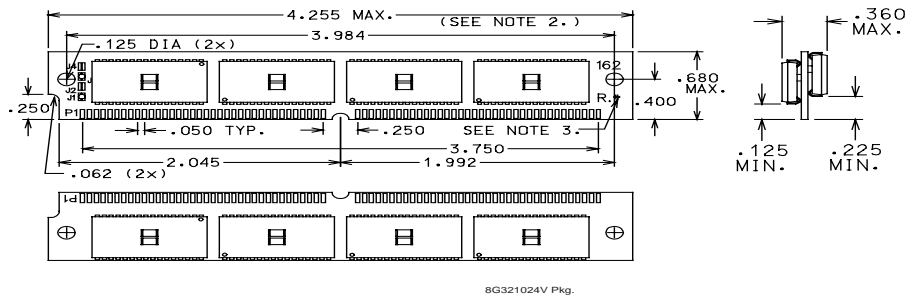
Part Number	Speed (ns)	Package No.
EDI8F321024V15MZC	15	175
EDI8F321024V20MZC	20	175
EDI8F321024V25MZC	25	175
EDI8F321024V15MMC	15	356
EDI8F321024V20MMC	20	356
EDI8F321024V25MMC	25	356

PACKAGE DESCRIPTIONS

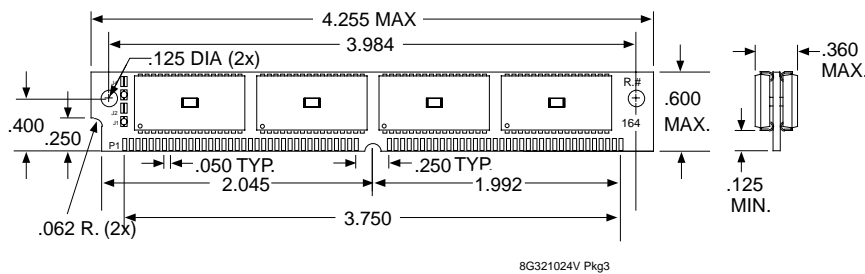
PACKAGE NO. 175: 72 PIN ZIP



PACKAGE NO. 176: 72 LEAD SIMM



PACKAGE NO. 356: 72 PIN GOLD SIMM



ALL DIMENSIONS ARE IN INCHES