WHITE ELECTRONIC DESIGNS

128K x 32 Static RAM CMOS, High Speed Module

FEATURES

- 128K x 32 bit CMOS Static RAM
  - Access Times: 10 and 12ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Package
  - JEDEC Standard Pinouts
  - 64 Pad SIMM, No. 38
  - 64 Pin ZIP, No. 39
  - Common Data Inputs and Outputs
- Single +3.3V (±10%) Supply Operation

DESCRIPTION

The EDI8F32128V is a high speed 4 megabit Static RAM module organized as 128K words by 32 bits. This module is constructed from four 128K x 8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables ($\overline{E0}$-$\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of enables.

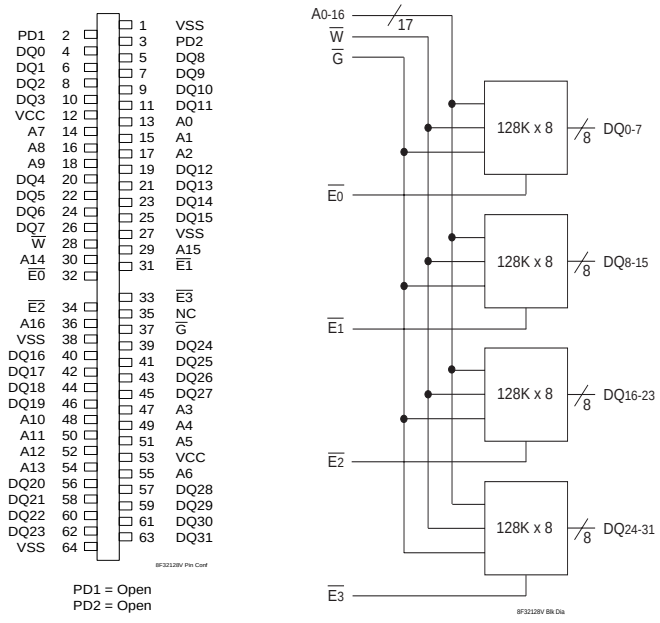
The EDI8F32128V is offered in 64 pin ZIP and 64 Pad SIMM packages, which enable four megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Two pins, PD1 and PD2, are used to identify module memory density in applications where alternate modules can be interchanged.

FIG. 1

PIN CONFIGURATIONS AND BLOCK DIAGRAM



PIN NAMES

$\overline{A0}$-$\overline{A16}$	Address Inputs
$\overline{E0}$-$\overline{E3}$	Chip Enables
$\overline{W}$	Write Enable
G	Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+3.3V±10%)
VSS	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature TA (Ambient) Commercial	0°C to +70°C
Storage Temperature	-55°C to +125°C
Power Dissipation	2.5 Watts
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	Vcc +0.3	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

Note: For T_{EHQZ}, T_{GHQZ} and T_{WLQZ}, CL = 5pF.

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max 12-25ns	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle		480	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL or VIN $\geq$ VIH		120	mA
Full Standby Power Supply Current CMOS	ICC3	$\overline{E} \geq$ VCC - 0.2V VIN $\geq$ VCC - 0.2V or VIN $\leq$ 0.2V		40	mA
Input Leakage Current	ILI	VIN = 0V to VCC		±20	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		±20	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	–	V
Output Low Voltage	VOL	IOL = 8.0mA	–	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2/ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

CAPACITANCE (F=1.0MHZ, VIN=VCC OR VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	45	pF

These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol JEDEC	Alt.	10ns Min	10ns Max	12ns Min	12ns Max	Units
Read Cycle Time	TAVAV	TRC	10		12		ns
Address Access Time	TAVQV	TAA		10		12	ns
Chip Enable Access	TELQV	TACS		10		12	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		5		6	ns
Output Hold from Address Change	TAVQX	TOH	3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		5	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		5		6	ns

Note 1: Parameter guaranteed, but not tested.

FIG. 2

READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

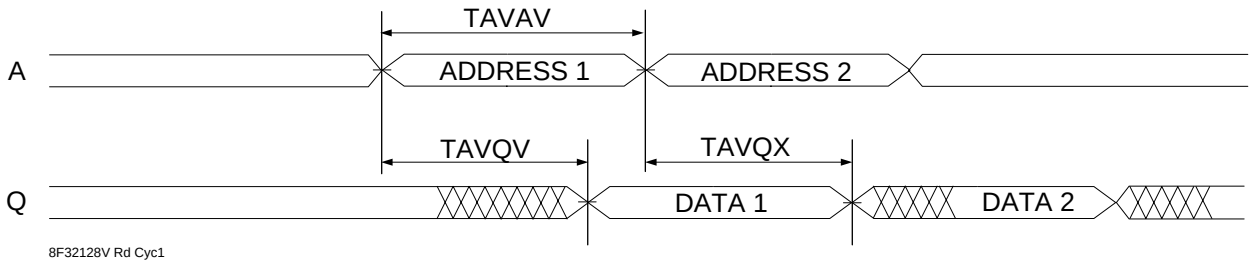
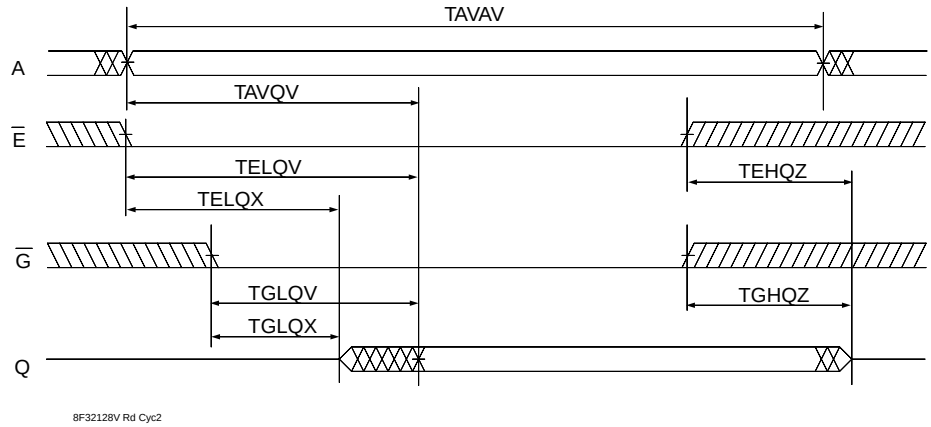


FIG. 3

READ CYCLE 2 - $\overline{W}$ HIGH



AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	10ns Min	10ns Max	12ns Min	12ns Max	Units
Write Cycle Time	TAVAV	TWC	10		12		ns
Chip Enable to End of Write	TELWH	TCW	7		8		ns
	TWLEH	TCW	7		8		ns
Address Setup Time	TAVWL	TAS	0		0		ns
	TAVEL	TAS	0		0		ns
Address Valid to End of Write	TAVWH	TAW	7		8		ns
	TAVEH	TAW	7		8		ns
Write Pulse Width	TWLWH	TWP	7		8		ns
	TELEH	TWP	7		8		ns
Write Recovery Time	TWHAX	TWR	0		0		ns
	TEHAX	TWR	0		0		ns
Data Hold Time	TWHDX	TDH	0		0		ns
	TEHDX	TDH	0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	ns
Data to Write Time	TDVWH	TDW	5		6		ns
	TDVEH	TDW	5		6		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		ns

Note 1: Parameter guaranteed, but not tested.

FIG. 4

WRITE CYCLE 1 - $\overline{W}$ CONTROLLED

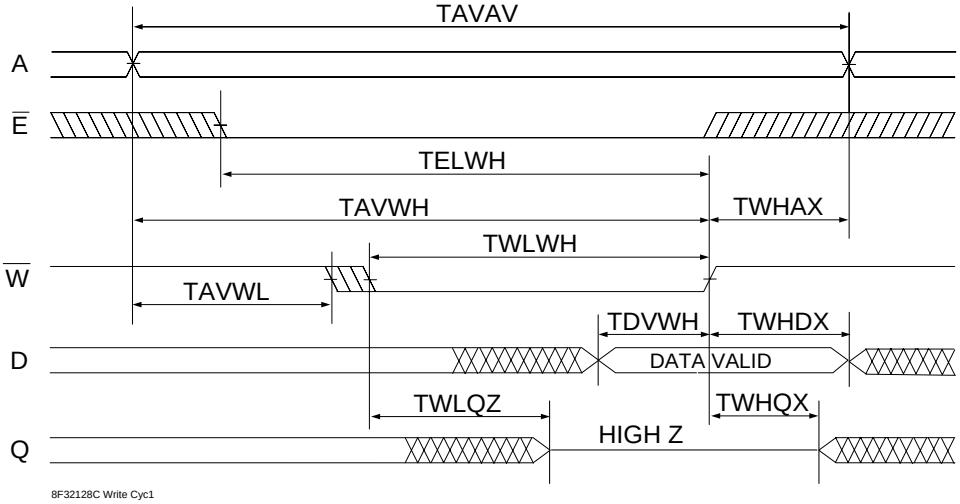
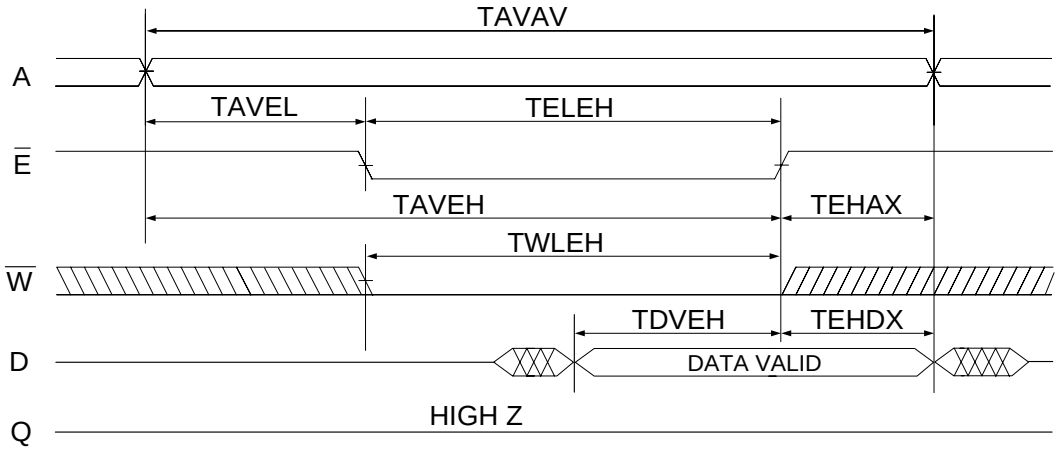


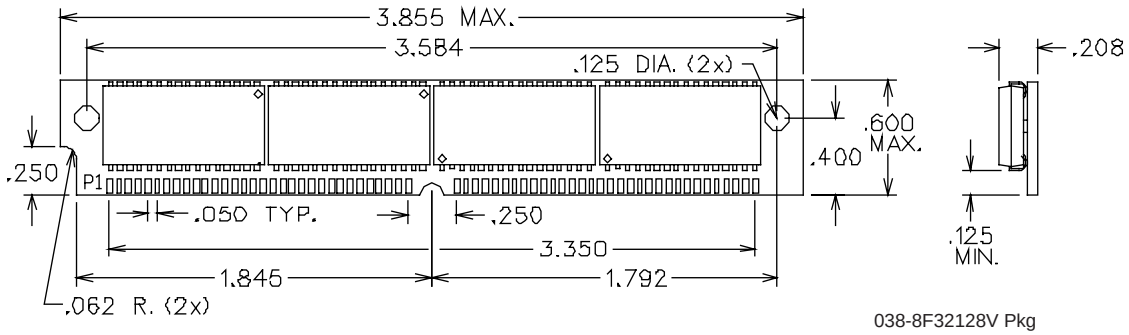
FIG. 5

WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



PACKAGE NO. 38

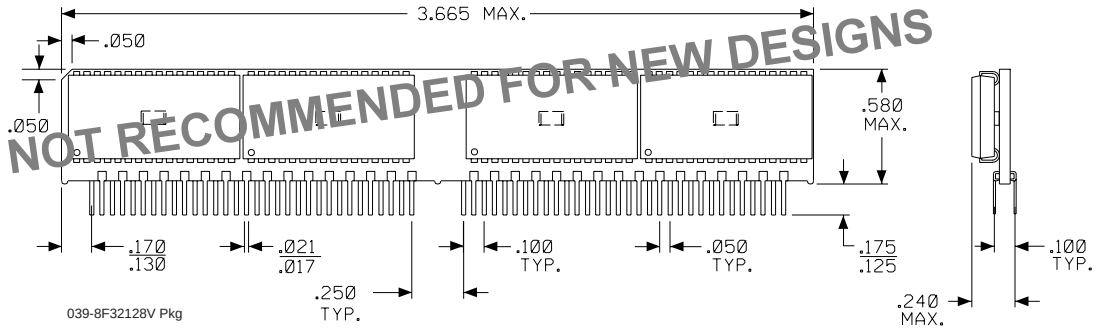
64 LEAD SIMM



038-8F32128V Pkg

PACKAGE NO. 39

64 PIN ZIP PLASTIC



039-8F32128V Pkg

ORDERING INFORMATION

Part Number	Speed (ns)	Package No.
EDI8F32128V10MMC	10	38
EDI8F32128V12MMC	12	38
EDI8F32128V10MZC	20	39
EDI8F32128V12MZC	25	39

Note: For Gold SIMM, change EDI8F to EDI8G.