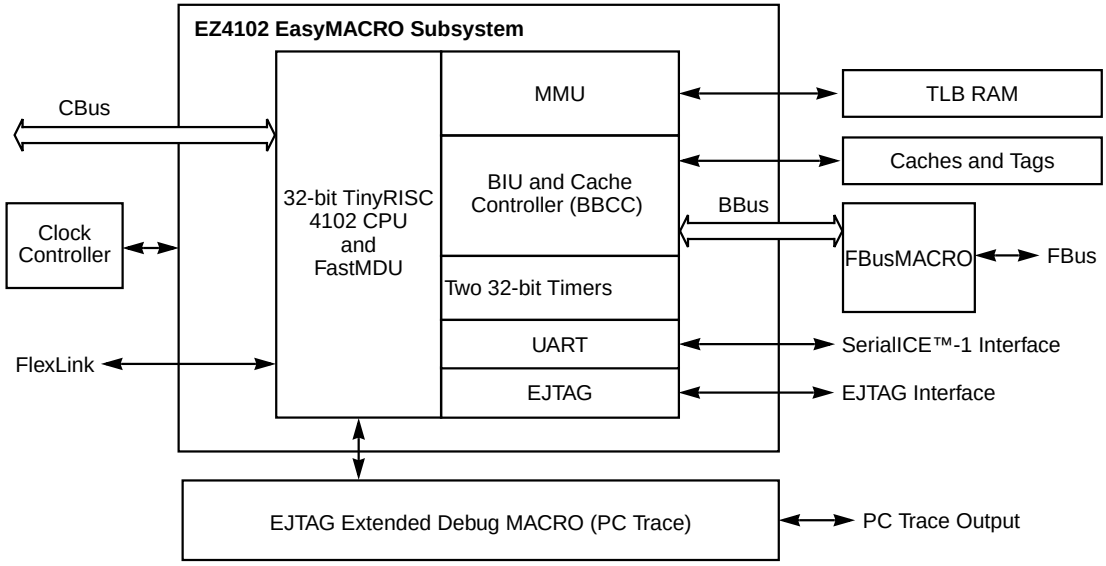
TinyRISC™ EZ4102 EasyMACRO Microprocessor

Preliminary Datasheet

The TinyRISC™ EZ4102 EasyMACRO subsystem is a compact, high-performance, 32-bit MIPS microprocessor subsystem implemented in LSI Logic's G11™ technology. The EZ4102 combines the TinyRISC CPU with the most commonly used blocks (such as a bus controller, MMU, and EJTAG) to simplify system-on-a-chip design and reduce time to market. A bus controller module (FBusMACRO) and RAMs are also available from LSI Logic to help speed your CoreWare® design.

The EZ4102 is appropriate for any embedded application that demands low power with code compression, and can be easily designed into a wide range of products. Figure 1 shows the EZ4102 and how it interfaces with system logic in a typical design.

Figure 1 EZ4102 in a Typical System



The EZ4102 is powered by either 2.5 V or 1.8 V. For 2.5 V operation, the EZ4102 is rated at 85 MHz (worst case conditions) with a performance of 85 MIPS peak and 68 MIPS sustainable. For 1.8 V operation, the EZ4102 is rated at 50 MHz (worst case conditions) with a performance of 50 MIPS peak and 40 MIPS sustainable. The EZ4102 utilizes G11

technology and implements a full-scan methodology to achieve very high fault coverage.

EZ4102 Overview and Features

Components

- MIPS R3000 CPU, executing MIPS I, MIPS II, and MIPS16 instructions
- EJTAG Interface and Controller
  - Nonintrusive debug
  - Real-time PC trace (requires Extended Debug MACRO)
  - Hardware breakpoints (requires Extended Debug MACRO)
- FastMDU
  - 5 cycle 32-bit to 64-bit multiply and accumulate
  - 34/35 cycle divide
- Basic BIU and Cache Controller (BBCC) with four write back buffers included
- Two 32-bit Timers
- MMU supports a 64-entry TLB RAM
- ICEport included for backward compatibility with SerialICE-1 debugger
- Caches:
  - 1 to 32 Kbytes of direct-mapped or set-associative I-Cache
  - 1 to 32 Kbytes of direct-mapped D-Cache

Technology

- LSI Logic's G11™ Technology with 0.18-µ L_{eff} (0.25-µ L_{drawn})
- 2.5 or 1.8 V operation

Features

- All configuration through EasyMACRO interfaces, no external logic needed
- Clock speed is 85 MHz at 2.5 V (85 MIPS peak and estimated 68 MIPS sustainable)
- 16-bit and 32-bit code can be mixed arbitrarily with full support on a subroutine basis
- Optional FBusMACRO (controller) available from LSI Logic to speed system development
- Models available: performance and software development, VHDL, Verilog, and gate level, timing-accurate models
- Compatible with the full range of MIPS, third-party software development, and system verification environment tools
- Implementation of full-scan methodology to achieve very high design fault coverage

EZ4102 Design Support

The EZ4102 EasyMACRO subsystem has all the necessary tools to develop a system on a chip, including:

- LSI Logic TinySIM™ architectural simulator
- Verilog and VHDL models
- System verification environment
- EJTAG on-chip debugger
- Third-party software support
- LR4102 microprocessor chip and evaluation kit for evaluation and prototyping

The EZ4102 supports the LSI Logic EJTAG interface, which enables software development and hardware design debugging from a remote host. EJTAG uses the EZ4102 EJTAG pins to provide a debug solution with breakpoint capability and real-time trace of the program counter (requires Extended Debug MACRO). A SerialICE-1 ICEport has also been added to the EZ4102 for backward compatibility with any existing TinyRISC designs.

The CoreWare program consists of three main elements:

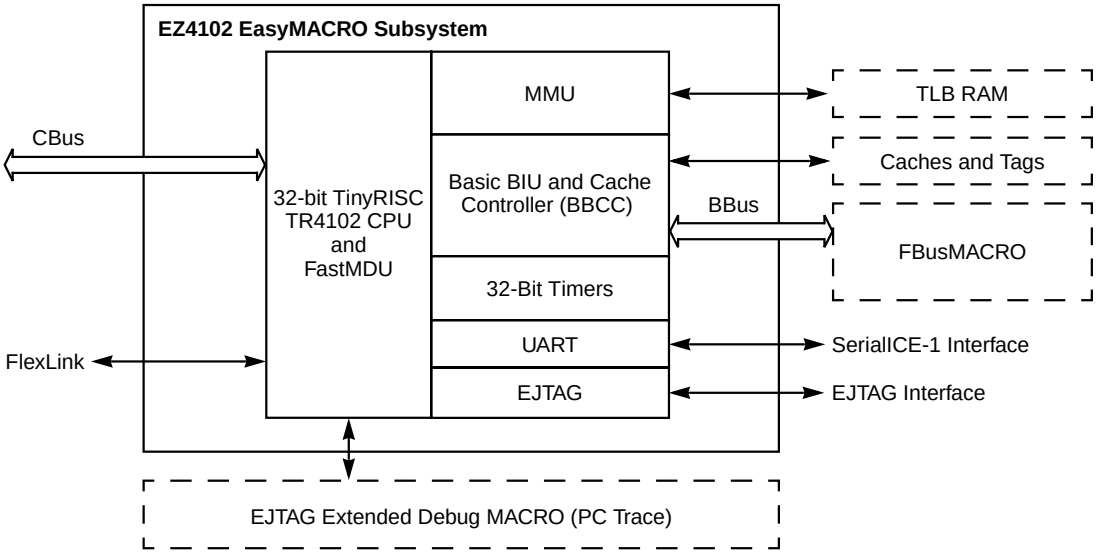
1. A library of cores
2. A design development and simulation package
3. Expert applications support

The CoreWare library contains a wide range of complex cores based on accepted and emerging industry standards from high-speed interconnect and digital video to DSP and MIPS microprocessors. LSI Logic provides a complete framework for device and system development and simulation. LSI Logic has advanced ASIC technologies that consistently produce Right-First-Time™ silicon. LSI Logic's in-house experts provide design support from system architecture definition through chip layout and test vector generation.

Block Diagram

Figure 2 is a block diagram of the TinyRISC EZ4102 EasyMACRO Microprocessor. Descriptions of the internal EZ4102 components follow the figure.

Figure 2 EZ4102 EasyMACRO Block Diagram



The TR4102 CPU performs all arithmetic, logical, shift, and address calculations. The CPU supports EJTAG debug and is closely coupled with the FastMDU. The FastMDU calculates all multiply and divide operations for the EZ4102 and provides 5 cycle 32 x 32 = 64 bit multiply and accumulate operations, 34/35 cycle divide, saturated math, and overflow indication.

The Basic BIU and Cache Controller (BBCC) controls the internal/external BBus arbitration and connects the EasyMACRO subsystem to the caches. Four Write Buffers are integrated with the BBCC in the EZ4102. The BBus connects the BBCC, the SerialICE-1 and EJTAG units, and the two internal timers with logic implemented inside the EZ4102.

The optional 32-bit FBusMACRO controls the FBus, a dedicated, multimaster bus that connects outside devices with the EZ4102 internal

components. The optional FBus controller allows seamless connection to a variety of devices, including EPROM, RAM, DRAM, SDRAM, and general purpose I/Os. The FBus also supports burst read (one cycle) and write, built-in arbitration for external FBus masters, and snooping of external write accesses to memory. The FBus connects to the BBus.

The Memory Management Unit (MMU) controls the Translation Look-Aside Buffer (TLB) RAM.

The two internal 32-bit Timers are controlled by the CPU. Each timer can count down from a preloaded value, roll over or stop at zero, or generate an interrupt on zero. The timers can also be used as a BBus Watchdog Timer to monitor BBus transactions.

The EJTAG Interface provides an on-chip debug scheme with breakpoint capability in an EJTAG compatible design. The EJTAG debugger provides real-time PC trace and hardware breakpoint capabilities (requires Extended Debug MACRO).

A SerialICE-1 Interface (UART) is also included in the EasyMACRO subsystem to promote backward compatibility with an existing TinyRISC design.

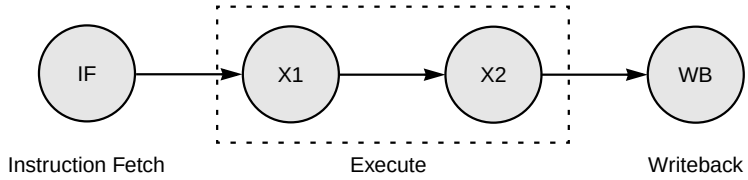
The CBus Interface passes data to and from the CPU. This interface connects the CPU to the MMU, the BBCC, and up to three optional coprocessors and on-chip memory implemented outside the EasyMACRO subsystem.

The FlexLink Interface allows the logic designer to insert specialized arithmetic instructions into the microprocessor EasyMACRO subsystem. The FlexLink interface can handle one-cycle and multicycle operations.

Pipeline Architecture

The EZ4102 implements a three-stage pipeline (Fetch, Execute, and Writeback) that uses a single adder for the ALU, the data address, and the instruction address. Sharing a single adder, as well as eliminating pipeline registers and bypass logic, dramatically reduces the circuitry required to implement the EasyMACRO microprocessor. The EZ4102 does not require a load delay slot. Figure 3 shows the microprocessor CPU three-stage pipeline.

Figure 3 EZ4102 Instruction Pipeline



The execution of a single EZ4102 instruction consists of the following three pipeline stages:

1. Instruction Fetch – The EZ4102 fetches the instruction (IF). If necessary, the core decompresses a 16-bit instruction into a 32-bit instruction.
2. Execute – The EZ4102 executes all ALU instructions, resolves conditional branches, and calculates Load and Store addresses (X1). The EasyMACRO microprocessor subsystem transfers Load and Store data from external memory or cache (performs memory accesses) and performs Move To/From Coprocessor operations in a second Execute (Stall) Cycle (X2).
3. Writeback – The EZ4102 writes the results into the Register File (WB).

Instruction Set Summary

Table 1 summarizes the 32-bit instruction set for the EZ4102. All instructions are MIPS I except those marked with a footnote. Tables 2 and 3 list the TinyRISC-specific CP0 and the Multiply/Divide instructions. Tables 4 and 5 list the MMU and the unimplemented MIPS II instructions. Table 6 provides a summary of the EZ4102 MIPS16 instruction set.

Table 1 EZ4102 Instruction Set Summary (32 bits)

Instruction	Description	Instruction	Description
Load/Store Instructions			
LB	Load Byte	SB	Store Byte
LBU	Load Byte Unsigned	SH	Store Halfword
LH	Load Halfword	SW	Store Word
LHU	Load Halfword Unsigned	SWL	Store Word Left
LW	Load Word	SWR	Store Word Right
LWL	Load Word Left	SYNC	Synchronize Shared Memory
LWR	Load Word Right		
Immediate Arithmetic Instructions			
ADDI	Add Immediate	ORI	OR Immediate
ADDIU	Add Immediate Unsigned	SLTI	Set on Less Than Immediate
ANDI	AND Immediate	SLTIU	Set on Less Than Immediate Unsigned
LUI	Load Upper Immediate	XORI	Exclusive OR Immediate

(Sheet 1 of 4)

Table 1 EZ4102 Instruction Set Summary (32 bits) (Cont.)

Instruction	Description	Instruction	Description
Three-Operand, Register-Type Arithmetic Instructions			
ADD	Add	SLT	Set on Less Than
ADDU	Add Unsigned	SLTU	Set on Less Than Unsigned
AND	Logical And	SUB	Subtract
NOR	Logical Nor	SUBU	Subtract Unsigned
OR	Logical Or	XOR	Exclusive Logical Or
Jump and Branch Instructions			
BCzF	Branch on Coprocessor z False (also listed under Coprocessor Instructions)	BLTZAL	Branch on Less Than Zero and Link
BCzT	Branch on Coprocessor z True (also listed under Coprocessor Instructions)	BNE	Branch on Not Equal
BEQ	Branch on Equal	J	Jump
BGEZ	Branch on Greater Than or Equal to Zero	JAL	Jump and Link
BGEZAL	Branch on Greater Than or Equal to Zero and Link	JALR	Jump and Link Register
BGTZ	Branch on Greater Than Zero	JALX	Jump and Link Exchange
BLEZ	Branch on Less Than or Equal to Zero	JR	Jump Register
BLTZ	Branch on Less Than Zero		

(Sheet 2 of 4)

Table 1 EZ4102 Instruction Set Summary (32 bits) (Cont.)

Instruction	Description	Instruction	Description
Branch Likely Instructions			
BCzFL[1]	Branch on Coprocessor z False Likely	BGTZL1	Branch on Greater Than Zero Likely
BCzTL1	Branch on Coprocessor z True Likely	BLEZL1	Branch on Less Than or Equal to Zero Likely
BEQL1	Branch on Equal Likely	BLTZALL1	Branch on Less Than Zero and Link Likely
BGEZALL1	Branch on Greater Than or Equal to Zero and Link Likely	BLTZL1	Branch on Less Than Zero Likely
BGEZL1	Branch on Greater Than or Equal to Zero Likely	BNEL1	Branch on Not Equal Likely
Trap Instructions			
TEQ1	Trap if Equal	TLT1	Trap if Less Than
TEQI1	Trap if Equal Immediate	TLTI1	Trap if Less Than Immediate
TGE1	Trap if Greater Than or Equal	TLTIU1	Trap if Less Than Immediate Unsigned
TGEI1	Trap if Greater Than or Equal Immediate	TLTU1	Trap if Less Than Unsigned
TGEIU1	Trap if Greater Than or Equal Immediate Unsigned	TNE1	Trap if Not Equal
TGEU1	Trap if Greater Than or Equal Unsigned	TNEI1	Trap If Not Equal Immediate

(Sheet 3 of 4)

Table 1 EZ4102 Instruction Set Summary (32 bits) (Cont.)

Instruction	Description	Instruction	Description
Coprocessor Instructions			
BCzF	Branch on Coprocessor z False (also listed under Jump and Branch Instructions)	LWCz	Load Word to Coprocessor z ($z \neq 0$)
BCzT	Branch on Coprocessor z True (also listed under Jump and Branch Instructions)	MTCz	Move To Coprocessor z
COPz	Coprocessor Operation	MFCz	Move From Coprocessor z
CTCz	Move Control to Coprocessor z	SWCz	Store Word from Coprocessor z ($z \neq 0$)
CFCz	Move Control from Coprocessor z		
Shift Instructions			
SLL	Shift Left Logical	SRAV	Shift Right Arithmetic Variable
SLLV	Shift Left Logical Variable	SRL	Shift Right Logical
SRA	Shift Right Arithmetic	SRLV	Shift Right Logical Variable
Special Control Instructions			
BREAK	Breakpoint	SYSCALL	System Call
EJTAG Debug Instructions			
SDBBP	Software Debug Breakpoint	DERET	Debug Exception Return
(Sheet 4 of 4)			

1. MIPS II instructions.

Table 2 EZ4102-Specific System Control Processor (CP0) Instructions (32 bits)

Instruction	Description	Instruction	Description
MFC0	Move from CP0	RFE	Restore from Exception
MTC0	Move to CP0	WAITI	Wait for Interrupt

Table 3 Multiply/Divide Instructions (32 bits)

Instruction	Description	Instruction	Description
MUL	Three-Operand Multiply	DIV	Divide
MULT	Multiply	DIVU	Divide Unsigned
MULTU	Multiply Unsigned	MFHI	Move From HI
MADD	Multiply Add	MFLO	Move From LO
MADDU	Multiply Add Unsigned	MTHI	Move To HI
MSUB	Multiply Subtract	MTLO	Move To LO
MSUBU	Multiply Subtract Unsigned		

Table 4 MMU TLB Instructions (32 bits)

Instruction	Description	Instruction	Description
TLBR	Read Indexed TLB Entry	TLBWI	Write Indexed TLB Entry
TLBWR	Write Random TLB Entry	TLBP	Probe TLB For Matching Entry

Table 5 Unimplemented MIPS II Instructions

Instruction	Description	Instruction	Description
COP1	All floating point instructions	ERET	Exception Return
LL	Load Linked Word	LDCz	Load Doubleword to Coprocessor
SC	Store Conditional Word	SDCz	Store Doubleword to Coprocessor

Table 6 EZ4102 Instruction Set Summary (MIPS16)

Instruction	Description	Instruction	Description
Load/Store Instructions			
LB	Load Byte	LW	Load Word
LBU	Load Byte Unsigned	SB	Store Byte
LH	Load Halfword	SH	Store Halfword
LHU	Load Halfword Unsigned	SW	Store Word
Arithmetic Instructions: ALU Immediate			
LI	Load Immediate	SLTIU	Set on Less Than Immediate Unsigned
ADDIU	Add Immediate Unsigned	CMPI	Compare Immediate
SLTI	Set on Less Than Immediate		
Arithmetic Instructions: Two/Three Operand, Register Type			
ADDU	Add Unsigned	AND	AND
SUBU	Subtract Unsigned	OR	OR
SLT	Set on Less Than	XOR	Exclusive OR
SLTU	Set on Less Than Unsigned	NOT	Not
CMP	Compare	MOVE	Move
NEG	Negate		
Multiply/Divide Instructions			
MULT	Multiply	DIVU	Divide Unsigned
MULTU	Multiply Unsigned	MFHI	Move From HI
DIV	Divide	MFLO	Move From LO

(Sheet 1 of 2)

Table 6 EZ4102 Instruction Set Summary (MIPS16) (Cont.)

Instruction	Description	Instruction	Description
Jump and Branch Instructions			
JAL	Jump and Link	BNEZ	Branch on Not Equal to Zero
JALX	Jump and Link Exchange	BTEQZ	Branch on T Equal to Zero
JR	Jump Register	BTNEZ	Branch on T Not Equal to Zero
JALR	Jump and Link Register	B	Branch Unconditional
BEQZ	Branch on Equal to Zero		
Shift Instructions			
SLL	Shift Left Logical	SLLV	Shift Left Logical Variable
SRL	Shift Right Logical	SRLV	Shift Right Logical Variable
SRA	Shift Right Arithmetic	SRAV	Shift Right Arithmetic Variable
Special Instructions			
EXTEND	Extend	BREAK	Breakpoint
EJTAG Debug Instructions			
SDBBP	Software Debug Breakpoint[1]		
(Sheet 2 of 2)			

1. This instruction is unique to the EZ4102.

Signal Descriptions

This section describes all signals that interact with the EZ4102 EasyMACRO microprocessor subsystem. These signals have been divided into the following tables:

Mnemonics for signals that are active LOW end with an ‘N’, and mnemonics for signals that are active HIGH end with a ‘P’.

In the descriptions that follow, the verb *assert* means to drive TRUE or active. The verb *deassert* means to drive FALSE or inactive.

Table 7 Global Interface and Miscellaneous Signals

Signal	I/O	Description
G_AMOFP	Output	FastMDU
G_BIG_ENDIANP	Input	CPU Big endian select
G_CACHE_CONFIGP[2:0]	Input	Controls to configure Cache/Tag size
G_CWAITIP	Output	CPU Wait Indicator
G_LOIDP[3:0]	Input	CPU Low ID nibble of CP0 PRID register (hardwire)
G_LOPRP[3:0]	Input	CPU Low REV nibble of CP0 PRID register (hardwire)
G_MAC_IBCMP	Input	FastMDU, Multiply-Accumulate instruction, TinyRISC backward compatibility mode
G_MMUENP	Input	MMU enable configuration bit
G_MRRP	Input	Modified Round Robin internal-bus algorithm selector
(Sheet 1 of 2)		

Table 7 Global Interface and Miscellaneous Signals (Cont.)

Signal	I/O	Description
G_PCLKP	Input	System clock
G_RESETN	Input	Synchronous system reset input
G_SATMP	Input	FastMDU Saturated math mode select
G_SCONFIG1P[31:0]	Output	BBCC System Configuration Register (SCR1)
G_SCONFIG2P[31:0]	Output	BBCC System Configuration Register (SCR2)
G_SCONFIG3P[31:0]	Output	BBCC System Configuration Register (SCR3)
G_SCR3_READP[31:0]	Input	Read-only bits for G_SCONFIG3P[31:0]
G_SCR2_RESETP[11:0]	Input	Copies into G_SCONFIG2P[11:0] during system reset
G_SCR2_STICKYP[3:0]	Input	Copies into G_SCONFIG2P[15:12], and value is sticky until reset by either system reset or CPU write zero
Scan Test Signals		
G_SCAN_ENABLEP	Input	Scan chain enable
G_SCAN_INP	Input	Scan chain input
G_SCAN_MODEP	Input	Scan test logic enable
G_SCAN_OUTP	Output	Scan chain output
G_SCAN_RAMWEP	Input	Scan mode RAM write control
Device ID Register Signals		
D_IPART_NUMBERP[13:0]	Input	Part number in Device Identification Register
D_IDEVICE_REVP[1:0]	Input	Device Revision code in Device Identification Register
D_ILOCATIONP[3:0]	Input	LSI Geographical Location Code in Device Identification Register
Timer Signals		
T_0OUTN	Output	Timer 0 output
T_1OUTN	Output	Timer 1 output

(Sheet 2 of 2)

Table 8 Debug Interface

Signal	I/O	Description
Scan Test Signals		
D_DX2EMP[43:0]	Input	Debug concatenated input bus
D_EM2DXP[221:0]	Output	Debug concatenated output bus
Processor Probe (or JTAG Tester) Signals		
D_TCK	Input	JTAG clock
D_TDI_DINT	Input	JTAG data in
D_TDO_DRIVEN	Output	JTAG drive indication for TDO
D_TDO_TPC	Output	JTAG data out
D_TMS	Input	JTAG mode select
D_TRST	Input	Active-LOW JTAG reset
EJTAG Tester Signals		
D_JTAGALSOP	Input	Normal JTAG interface attached
D_JTAGIRBITSP[1:0]	Input	Number of bits in JTAG instruction register
D_JTAGTDOP	Input	Test Data Output from normal JTAG module
Implementation Register Signals		
D_IASIDSIZEP[1:0]	Input	ASID size in Implementation Register
D_ICHP[3:0]	Input	Obsolete Ch field in Implementation Register
D_ICPLXBRKP	Input	Complex Break Support in Implementation Register
D_IDCACHECP	Input	Data Cache Coherency in Implementation Register
D_IICACHECP	Input	Instruction Cache Coherency in Implementation Register
D_IIMPL3126P[5:0]	Input	Reserved
D_INODATABRKP	Input	Data Address Break in Implementation Register
D_INODMAP	Input	No JTAG DMA Support in Implementation Register

(Sheet 1 of 2)

Table 8 Debug Interface (Cont.)

Signal	I/O	Description
D_INOINSTBRKP	Input	Instruction Break in Implementation Register
D_INOPCTRACEP	Input	No PC Trace Support in Implementation Register
D_INOPROCBRKP	Input	Processor Bus Break in Implementation Register
D_IPCSTWP[2:0]	Input	PCST Width and DCLK Division Factor in Implementation Register
D_IPROFSUPP[1:0]	Input	Profiling Support in Implementation Register
D_ISDBBPCODEP	Input	SDBBP uses Special2 (or version 1.3) Opcode
D_ITPCWP[2:0]	Input	TPC Width in Implementation Register
Other Debug Signals		
D_CDEBUGMP	Output	Debug Mode Indicator
D_PCLKWAKEUP	Output	Indicates wake-up of the PCLKP clock generator when either a JTAG break or a CPU soft reset occurs
D_PERRSTN	Output	Reset signal for peripheral from the EJTAG Control Register
D_PSLEEPN	Input	Run indication for CPU clock, generated by clock module

(Sheet 2 of 2)

Table 9 FlexLink Interface

Signal	I/O	Description
F_CIR_BOTP[5:0]	Output	Instruction register bottom six bits
F_CIR_TOPP[5:0]	Output	Instruction register top six bits
F_CKILLXP	Output	Kill instruction in X1 stage
F_CPIPE_RUNN	Output	Indicates that next cycle is a CPU run cycle without an X2 stage
F_CRSP[31:0]	Output	Source register (rs) bus
F_CRTP[31:0]	Output	Source register (rt) bus

(Sheet 1 of 2)

Table 9 FlexLink Interface (Cont.)

Signal	I/O	Description
F_CRUN_INN	Output	CPU run enable
F_CRX_VALIDN	Output	Register buses valid
F_MODE16P	Output	FlexLink MIPS16 mode indication
F_SELP	Input	FlexLink bolt-on select
F_STALLP	Input	FlexLink bolt-on stall request
F_XBUSP[31:0]	Input	FlexLink bolt-on result bus
(Sheet 2 of 2)		

Table 10 MMU Interface

Signal	I/O	Description
M_CAMINP[25:0]	Input	TLB CAM array data
M_CAMOUTP[25:0]	Output	TLB CAM array data
M_GBITOUTP	Output	TLB group mask (global) bit
M_MATCHINP[5:0]	Input	TLB encoded match address
M_RAMINP[23:0]	Input	TLB RAM array data
M_RAMOUTP[23:0]	Output	TLB RAM array data
M_TLBCLKP	Output	TLB gated CLK (runs only during MMU stall cycles)
M_TLBINDP[5:0]	Output	TLB Address
M_TLBMISSP	Input	TLB miss indicator
M_TLBMTCHP	Output	TLB match enable
M_TLBRDP	Output	TLB read enable
M_TLBWRTP	Output	TLB write enable

Table 11 CBus Interface[1]

Signal	I/O	Description
C_ADDR_ERRORP	Output	Memory address error
C_BBEP	Input	BIU Bus error
C_BBEP_ACKP	Output	CPU BIU Bus error acknowledge
C_BYTEP[3:0]	Output	Byte enable signals
C_CBUS_STEALN	Output	Indicates a CBus steal from the BBCC
C_COPCONDP[3:0]	Input	CPU coprocessor condition bits
C_COP_DRIVEP	Output	Indicates that the coprocessor is driving the data bus
C_COPEXISTP[3:1]	Input	Indicates coprocessor existence
C_COPP[1:0]	Output	Coprocessor number
C_DATAP[31:0]	Output	CBus data bus
C_DRDYP	Output	CBus data ready on data bus
C_EXT_CDATAP[31:0]	input	CBus input from external modules
C_EXT_DRDYP	Input	External CBus data ready on data bus
C_EXT_IRDYP	Input	External CBus instruction ready
C_EXT_RUN_ENABLEP	Input	CBus run enable signal, deasserting C_EXT_RUN_ENABLEP causes the CPU to stall
C_EXT_OEP	output	External CBus output enable
C_EXT_SELP	Input	External CBus select signal
C_INTGRP	Output	CPU interrupt grant
C_INTP[5:0]	Input	CPU interrupt direct
C_IP_DN	Output	Indicates that instruction/data is available on the CBus
C_IRDYP	Output	CBus instruction ready
C_KILLMEMP	Output	CPU kill memory transaction
C_KILLWP	Output	CBus kill instruction in WB stage

(Sheet 1 of 2)

Table 11 CBus Interface[1] (Cont.)

Signal	I/O	Description
C_KILLXP	Output	CBus kill instruction in X1 stage
C_MEM_FETCHP	Output	CPU memory fetch request
C_MNOCACHEP	Output	MMU prevents current page data from storage in cache
C_MODE16P	Output	CPU in MIPS16 mode
C_RUNN	Output	Indicates that the next cycle is a run cycle
C_STOREP	Output	CPU store to memory request
(Sheet 2 of 2)		

1. Note that ADDRP[31:0] and BBUS_STEALN are intentionally left out of the interface.

Table 12 BBCC Interface

Signal	I/O	Description
OCM Related Signals		
C_MADDR_OUTP[31:2]	Output	Physical address output from MMU
C_MADDR_VALIDP	Output	Indicates that physical address is valid
C_OCMCLKP	Output	On-chip memory clock
C_OCMEXISTP	Input	On-chip memory exists
C_OCMOEP	Output	On-chip memory output enable
C_OCMSELP	Input	On-chip memory select signal
C_OCMWEP	Output	On-chip memory write enable
Cache and Tag Signals		
R_I1DCDATAP[31:0]	Input	Data from I-Cache Set 1 Data RAM
R_I1DCLKP	Output	Clock for I-Cache Set 1 Data RAM
R_I1DWEP	Output	Write enable for I-Cache Set 1 Data RAM
R_I1TCDATAP[25:0]	Input	Data from I-Cache Set 1 Tag RAM
(Sheet 1 of 4)		

Table 12 BBCC Interface (Cont.)

Signal	I/O	Description
R_I1TCLKP	Output	Clock for I-Cache Set 1 Tag RAM
R_I1TWEP[4:0]	Output	Write enable for I-Cache Set 1 Tag RAM
R_IDDCDATAP[31:0]	Input	Data from I-Cache Set 0/D-Cache Data RAM
R_IDDCLKP	Output	Clock for I-Cache Set 0/D-Cache Data RAM
R_IDDWEP[3:0]	Output	Write enable for I-Cache Set 0/D-Cache Data RAM
R_IDTCDATAP[26:0]	Input	Data from I-Cache Set 0/D-Cache Tag RAM
R_IDTCLKP	Output	Clock for I-Cache Set 0/D-Cache Tag RAM
R_IDTWEP[5:0]	Output	Write enable for I-Cache Set 0/D-Cache Tag RAM
R_INDEXP[14:2]	Output	Address for I-Cache Set 0/D-Cache and I-Cache Set 1 Data RAMs
R_IP_DN	Output	MSB address bit for I-Cache Set 0/D-Cache Data and Tag RAM
R_LOCKP	Output	Lock bits for I-Cache Set 0/D-Cache Tag RAM
R_TAGP[21:0]	Output	Address Tag for I-Cache Set 0/D-Cache and I-Cache Set 1 Tag RAM
R_VALIDP[3:0]	Output	Valid bits for I-Cache Set 0/D-Cache and I-Cache Set 1 Tag RAM
BBus Signals		
B_CONTADDRN	Output	BBus continuous address indicator
B_FBREQN	Input	BBus request to master from FBus module (7)
B_WRAPP	Output	BBus address wrap-around indicator
B_XBADDRP[31:2]	Output	Output address bus to all BBus devices
B_XBBLKREQN	Output	Block fetch request to external BBus device (only from BBCC)
B_XBBYTEN[3:0]	Output	Byte enable bits to all BBus devices
B_XBDATAP[31:0]	Output	Output data bus to all BBus devices

(Sheet 2 of 4)

Table 12 BBCC Interface (Cont.)

Signal	I/O	Description
B_XBERRORN	Output	BBus error signal to all BBus devices (bundled)
B_XBIP_DN	Output	Instruction/data indicator to all BBus devices
B_XBNOSELN	Output	Indicates hardware test mode (B_ZCACHE_SELP) and no address selected to all BBus devices
B_XBRDYN	Output	Ready signal (transaction complete) to all BBus devices
B_XBSNOOPWAITP	Output	Wait for snoop to finish signal to all BBus devices
B_XBSTARTN	Output	Transaction start signal to all BBus devices
B_XBTXN	Output	Transaction active signal to all BBus devices
B_XBWBURST_GNTN	Output	Write burst grant to external BBus device (only from BBCC)
B_XBWRN	Output	Read/write indicator to all BBus devices
B_XFBGNTN	Output	BBus grant to FBus module (FBM)
B_XZBGNTN	Output	BBus grant to external BBus device
B_ZBADDRP[31:2]	Input	Input address bus from external BBus device
B_ZBBLKGNTN	Input	Block fetch grant from external BBus device (only to BBCC)
B_ZBBYTEN[3:0]	Input	Byte enable bits from external BBus device
B_ZBDATAP[31:0]	Input	Input data bus from external BBus device
B_ZBDSNOOPP	Input	BBus data snoop signal
B_ZBERRORN	Input	BBus error signal from external BBus device
B_ZBIP_DN	Input	Indicates arriving instruction/data from external BBus device
B_ZBISNOOPP	Input	BBus instruction snoop signal
B_ZBRDYN	Input	Ready signal (transaction complete) from external BBus device
B_ZBREQN	Input	BBus request from external BBus device

(Sheet 3 of 4)

Table 12 BBCC Interface (Cont.)

Signal	I/O	Description
B_ZBSTARTN	Input	Transaction start signal from external BBus device
B_ZBTXN	Input	Transaction active signal from external BBus device
B_ZBWBURST_REQN	Input	Write burst request from external BBus device (only to BBCC)
B_ZBWRN	Input	Indicates a read/write from external BBus device
B_ZCACHE_SELP	Input	Indicates hardware test mode. Signal is supplied by hardware test master (from external BBus device).
B_ZISETP	Input	Hardware cache test select between I-Cache Set 0 and Set 1. B_ZISETP is supplied by hardware test master (from external BBus device).
B_ZTAGTESTN	Input	Hardware cache test select between Tag and Data cache. B_ZTAGTESTN is supplied by hardware test master (from external BBus device).
ICEport Signals		
I_ICECLKP	Input	External clock, must run at 16x the serial bit rate
I_ICERXP	Input	Serial receive data
I_ICETXP	Output	Serial transmit data
I_RXRDYP	Output	Asserts when a byte is received

(Sheet 4 of 4)

EZ4102 Nomenclature

As with any new product, the EZ4102 nomenclature has changed since the previous TR4101 design. Table 13 lists the supporting products for the TR4101 and EZ4102 designs.

Table 13 TinyRISC Family Nomenclature

TinyRISC Design	Core	EasyMACRO	Evaluation Chip	Reference Chip	Evaluation Board
4101	TR4101 (CW001000)	—	EV4101 (L9C0099)	—	BDMR4101
4102	—	EZ4102 (CW001005)	—	LR4102 (L9A0212)	BDMR4102

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