

10/100 LAN Interface Module with Enhanced Common Mode Attenuation

EPF8037



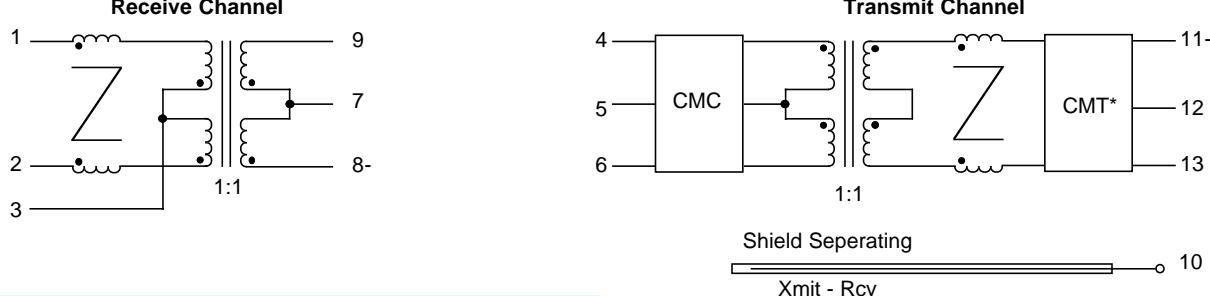
- Optimized for DP83840A/DP83223 Chip Set •
- Recommended for use with ICS 1890 Series and SS578Q2120 • when connected per appropriate schematic
- Guaranteed to operate with 8 mA DC bias at 70°C •
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

Electrical Parameters @ 25° C

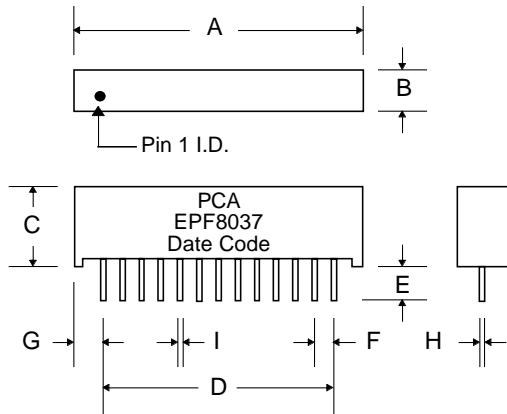
OCL @ 70°C	Insertion Loss (dB Max.)			Return Loss (dB Min.)			Common Mode Rejection (dB Min.)			Crosstalk (dB Min.) [Between Channels]										
100 KHz, 0.1 Vrms 8 mA DC Bias	1-80 MHz	80-100 MHz	100-150 MHz	1-30 MHz	30-60 MHz	60-100 MHz	1-30 MHz	30-100 MHz	100-500 MHz	5-10 MHz	10-100 MHz									
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit									
350µH	-1	-1	-1	-1	-3.5	-3	-18	-18	-12	-12	-10	-10	-40	-40	-35	-30	-10	-10	-35	-35

- **Isolation** : 1500 Vrms
- **Impedance** : 100 Ω
- **Rise Time** : 3.0 nS Max.
- * **CMT** : Optional

Schematic



Package



Dimensions

Dim.	(Inches)			(Millimeters)		
	Min.	Max.	Nom.	Min.	Max.	Nom.
A	1.340	1.360		34.04	34.54	
B	.190	.210		4.83	5.33	
C	.480	.500		12.19	12.7	
D	1.200	Typ.		30.48	Typ.	
E	.125	.150		3.18	3.81	
F	.100	Typ.		2.54	Typ.	
G				.075	12.7	13.20
H	.008	.012		.203	.304	1.91
I	.018	.021		.381	.533	

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The circuit below is a guideline for interconnecting PCA's EPF8037 with National DP83840A and DP83223 twister chip set for 10/100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes. Please consult PCA for applications help regarding the SSI78Q2120 or ICS1890 series parts or consult with the respective application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the TXREF resistor of the twister chip to get at least 2.12V pk-pk across pins 16-15.

Note that significant low frequency response improvement can be obtained in the system (improving equalization effects) if the DC blocking capacitors were not used; this can only be done by choosing a different pinout for the 10 Base-T receiver side. This is accomplished without impacting any other behavior. If any user has a need to improve this feature, please consult with the PCA Technical support group. This solution is similar to approaches used in EPF8013GM, EPF8022G and EPF8038S (a repeater interface module).

It is recommended that system designers do not ground the receiver side center tap, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8037. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω , balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP (Excerpts from NSC DP83840A application notes)

