Eureka Technology

EC220 32-bit PCI Master/Target

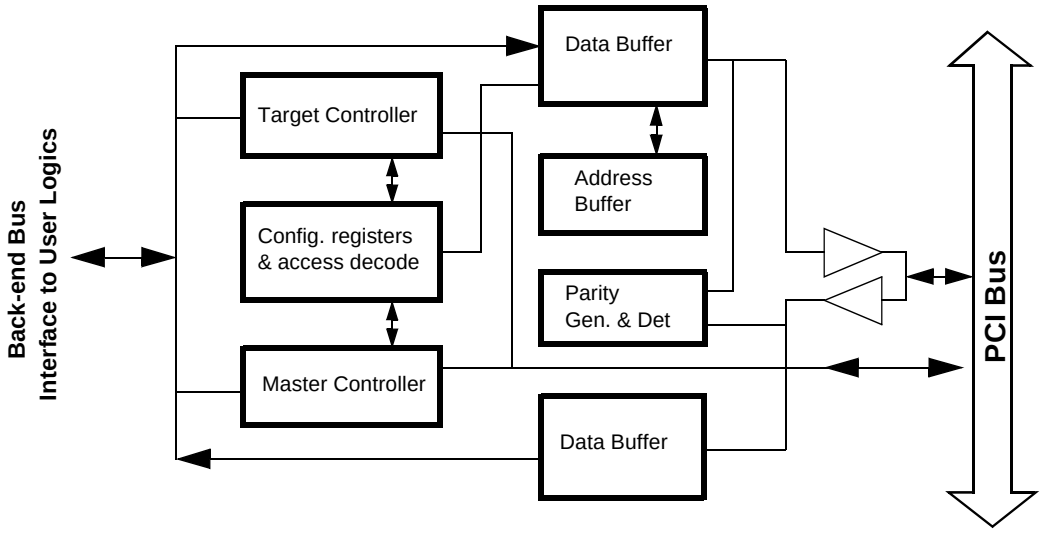
Product Summary

FEATURES

- Fully supports PCI specification 2.1 and 2.2 protocol.
- Designed for ASIC and PLD implementations.
- Fully static design with edge triggered flip-flops.
- Efficient back-end interface for different types of user devices.
- Supports compact PCI, Cardbus, Mini-PCI and Power Management.
- Combined bus master and target functions.
  Master function
  - Initiate PCI memory and IO read/write.
  - Automatic transfer restart on target retry and disconnect
  Target function
  - Memory or IO read/write
  - Configuration read/write
  - Support for back-end initiated target retry, disconnect and abort.
- Supports Zero wait state and user inserted wait state burst data transfer.
- Dual write buffer supports write data posting.
- User controlled burst and non-burst data transfer.
- Automatic handling of configuration register read/write access.
- Supports user initiated target retry, disconnect, abort and delayed transaction.
- Parity generation and parity error detection.
- Includes all PCI specific configuration registers.
- Supports high speed bus request and bus parking.

DESCRIPTIONS

The 32-bit PCI bus master/target core is optimized for different applications. The back-end interface is a highly efficient and flexible back-end bus which provides for easy integration with other user logic. The core utilizes double data buffer design approach which minimizes design gate count and achieves highest possible



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data bandwidth at the same time.

The PCI bus master controller is capable of initiating memory or IO read and write upon back-end requests. The type of command and the burst size are specified by the user for each data transaction. Burst size can be pre-determined by the user for each transaction or changed as the transaction progresses.

Once a master transfer begins, the core monitors the target device's signals on the PCI bus and transfer data to the user logic. All different types of transfer termination are handled by the core. If a transfer is retry or disconnected by the target, the master core re-starts the transfer automatically without the assistance of the user logic. Bus request, bus parking, parity detection and generation all are handled by the core.

The PCI target is capable of handling memory and IO accesses on the PCI bus. All seven types of PCI memory/IO accesses are supported. Configuration register read and write transactions are supported locally by the bus target without assistance from the user logic. The user interface allows the user to control the characteristics of the access. For example, the user can insert a wait state or transfer data without wait state according to its data bandwidth. Single or burst transfer, retry, disconnect, delay transaction and target abort can all be controlled by user logic.

OPTIONAL FEATURES

The following table summarizes the optional features which are provided with the core as required by user application.

Options	Description
Mini-PCI and Power Management	Specific supports for Mini-PCI and Power Management for mobile applications.
Base address registers	Supports multiple base address registers, memory or IO mapped, and expansion ROM base address register.
Address and data multiplexing	Separate or combined back-end address and data buses.
DAC	Dual Address cycle to support 64-bit address space.
Direct FIFO interface	The back-end bus can be made to directly interface a FIFO.
Burst length	Automatically limits the burst size beyond user specific boundaries.
Target burst	Single transfer support to minimize core size.
Asynchronous clock domains	Separate and asynchronous user and PCI clock domains. The core provides re-synchronization and data FIFO.

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CPLD SPECIFICATIONS

Supported Family	Cypress Delta39K CPLD, 0.18um SRAM process
Device Tested	CY39100V676-200MBC
Data Bus Width	32 bits
Post Layout Performance	33 MHz
Tsu on PCI Bus	6.933ns
Tco on PCI Bus	7.530ns
Tpd	3.683ns
Macrocells Used	714/1536
Cluster Memories Used	0/24
Channel Memories Used	0/12
IO Cells Used	220/294
Global Clocks Used	1/4
Global Controls Used	0/4

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