Eureka Technology

EC125 32-bit PCI Target

Product Summary

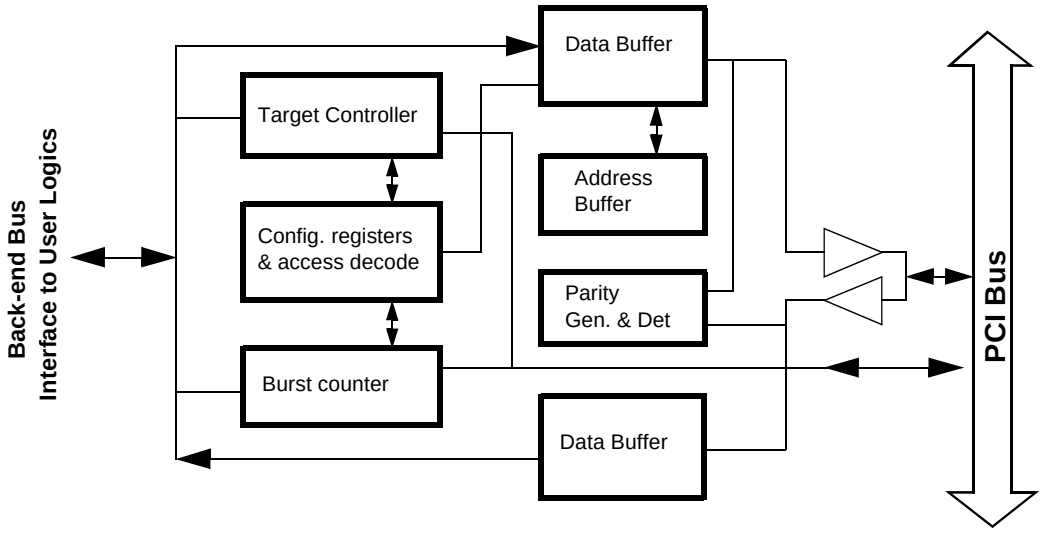
FEATURES

- Fully supports PCI specification 2.1 and 2.2 protocol.
- Designed for ASIC and PLD implementations.
- Fully static design with edge triggered flip-flops.
- Efficient back-end interface for different types of user devices.
- Supports compact PCI, Cardbus, Mini-PCI and Power Management.
- Supports zero wait state data burst transfer to maximize memory bandwidth.
- Zero wait state and user inserted wait state burst data transfer.
- Dual write buffer supports write data posting.
- User controlled burst and non-burst data transfer.
- Multiple address mapping to memory and IO address spaces.
- Automatic handling of configuration register read/write access.
- Supports back-end initiated target retry, disconnect and abort.
- Supports delayed data transaction initiated by user logic.
- Parity generation and parity error detection.
- Includes all PCI specific configuration registers.

DESCRIPTIONS

The 32-bit PCI bus target core is optimized for different applications. The back-end interface is a highly efficient and flexible back-end bus which provides for easy integration with other user logic. The core utilizes double data buffer design approach which minimizes design gate count and achieves highest possible data bandwidth at the same time.

The PCI target controller is capable of handling memory and IO accesses on the PCI. All seven types of PCI memory/IO accesses are supported. Configuration register read and write transactions are supported locally by the bus target without



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assistance from the user logic. Data parity detection and generation are also handled by the core locally.

When a bus master on the PCI bus initiates a PCI transaction, the core decodes the address and the command and claims the transaction if the address is decoded to be within the address space of one of the target devices at the back-end. The PCI transaction is propagated to the proper target device in simple protocol through the back-end bus.

The user interface allows the user to control the characteristics of the access. For example, the user can insert a wait state or transfer data without wait state according to its data bandwidth. Single or burst transfer, retry, disconnect, delay transaction and target abort can all be controlled by user logic.

OPTIONAL FEATURES

The following table summarizes the optional features which can be provided with the core as required by user application.

Options	Description
Mini-PCI and Power Management	Specific supports for Mini-PCI and Power Management for mobile applications.
Base address registers	Supports multiple base address registers, memory or IO mapped, and expansion ROM base address register.
Address and data multiplexing	Separate or combined back-end address and data buses.
DAC	Dual Address cycle to support 64-bit address space.
Direct FIFO interface	The back-end bus can be made to directly interface a FIFO.
Burst length	Automatically limits the burst size beyond user specific boundaries.
Target burst	Single transfer support to minimize core size.
Asynchronous clock domains	Separate and asynchronous user and PCI clock domains. The core provides re-synchronization and data FIFO.

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CPLD SPECIFICATIONS

Supported Family	Cypress Delta39K CPLD, 0.18um SRAM process
Device Tested	CY39100V676-200MBC
Data Bus Width	32 bits
Post Layout Performance	33 MHz
Tsu on PCI Bus	5.957ns
Tco on PCI Bus	7.745ns
Macrocells Used	376/1536
Cluster Memories Used	0/24
Channel Memories Used	0/12
IO Cells Used	196/294
Global Clocks Used	1/4
Global Controls Used	0/4

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