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EM127C08

Low Power 128Kx8 SRAM with ROM Type Pinout

Overview

The EM127C08 is an integrated memory device containing a low power 1 Mbit Static Random Access Memory organized as 131,072 words by 8 bits. The device is fabricated using an advanced CMOS process and NanoAmp's high-speed/low-power circuit technology. This device is designed to be quite effective in battery powered products with it's very low operating and standby currents. It is also capable of full operation at voltages as low as 1.5 volts. The device pinout is fully compatible with NanoAmp's EM02R2XX/EM11R2XX family of Combination RAM and ROM products making it very easy to substitute an SRAM only device where the ROM is unneccessary in the application. This device is extremely stable over broad temperature and voltage ranges.

Features

- **Extended Operating Voltage Range**
  1.5 to 3.6 V
- **Very Low Standby Voltage**
  1.2 V
- **Extended Temperature Range**
  -20^{o} to $+80^{o}$C
- **Fast Cycle Time**
  100 ns (@ 2.7V)
- **Very Low Operating Current**
  I_{CC} < 1 mA typical at 3V, 1 Mhz
- **Very Low Standby Current**
  I_{SB} = 200 nA typical
- **Available in 32-pin STSOP package**

FIGURE 1: Pin Configuration

TABLE 1: Pin Descriptions

Pin Name	Pin Function
A0-A16	Address Inputs
D0-D7	Data Inputs/Outputs
CE1	Chip Enable (Active Low)
CE2	Chip Enable (Active High)
OE	Output Enable (Active Low)
WE	Write Enable (Active Low)
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected (Floating)

FIGURE 2: Operating Envelope

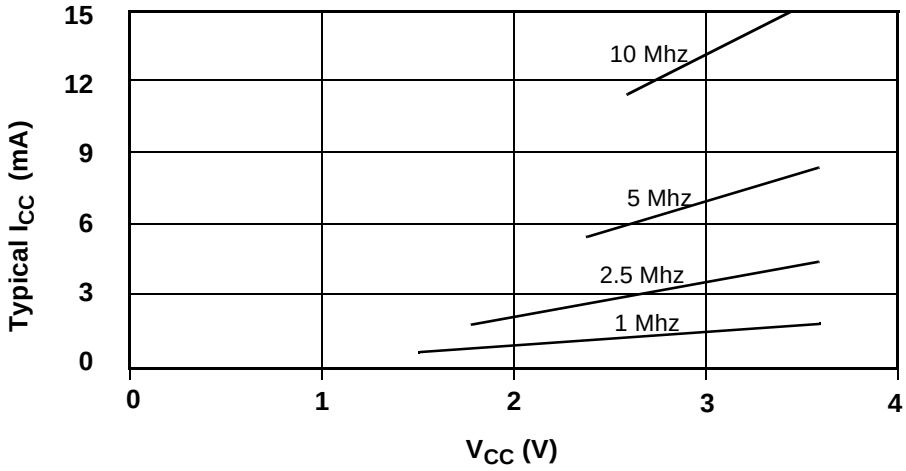

FIGURE 3: Functional Block Diagram

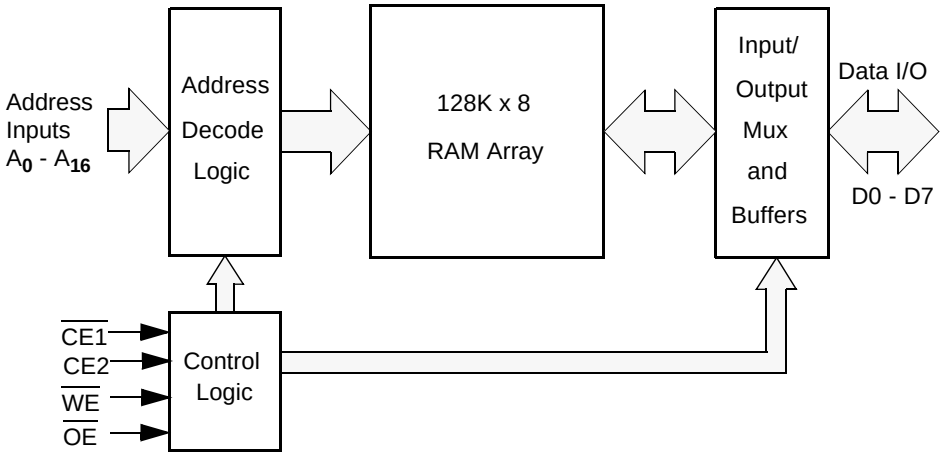

FIGURE 4: Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	D0-D7	MODE	POWER
H	X	X	X	High Z	Standby	Standby
X	L	X	X	High Z	Standby	Standby
L	H	H	H	High Z	Standby	Standby*
L	H	H	L	Data Out	READ	Active -> Standby*
L	H	L	X	Data In	WRITE	Active -> Standby*

*The device will consume active power in this mode whenever addresses are changed

TABLE 2: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.6	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to +125	^oC
Operating Temperature - Extended Commercial	T_A	-20 to +80	^oC

*Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 3: Operating Characteristics (Over specified temperature range)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Supply Voltage	V_{CC}		1.5	3.6	V
Data Retention Voltage	V_{DR}	$\overline{CE} = V_{CC}$	1.2	3.6	V
Input High Voltage	V_{IH}		$0.7V_{CC}$	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}		–0.3	$0.3V_{CC}$	V
Output High Voltage	V_{OH}	I_{OH} = 200 µA	V_{CC}–0.2		V
Output Low Voltage	V_{OL}	I_{OL} = –200 µA		0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		1	µA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ or $\overline{CE} = 1$		1	µA
Operating Supply Current (Note 1)	I_{CC}	$V_{IN} = V_{CC}$ or 0V, $\overline{CE} = 0$		0.5 * f * V	mA
Standby Current (Note 2)	I_{SB}	$V_{IN} = V_{CC}$ or 0V		10	µA

Note 1. Operating current is a linear function of frequency and voltage. You may calculate operating current using the formula shown with operating frequency (f) expressed in Mhz and operating voltage (V) in volts. Example: Operating at 2 Mhz and 2.0 volts will draw a maximum current of 0.5*2*2 = 2.0 mA.

Note 2. This device assumes a standby mode if either $\overline{CE1}$ is disabled (high) or CE2 is disabled (low). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) regardless of the state of $\overline{CE1}$ or CE2. In order to achieve low standby current in the enabled mode ($\overline{CE1}$ low and CE2 high), all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

TABLE 4: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 Mhz, $T_A = 25^oC$		5	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 Mhz, $T_A = 25^oC$		5	pF

Note: These parameters are verified in device characterization and are not 100% tested

TABLE 5: Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5V_{CC}$
Output Load	CL = 30pF
Operating Temperature (Unless otherwise stated)	-20 to +80 ^oC

TABLE 6: Timing

Item	Symbol	Min/Max	1.5V	1.8V	2.4V	2.7-3.6V	Units
Read Cycle Time	t_{RC}	Min	750	250	150	100	ns
Address Access Time	t_{AA}	Max	750	250	150	100	ns
Chip Enable Access Time	t_{CE}	Max	750	250	150	100	ns
Output Enable to Valid Output	t_{OE}	Max	250	70	50	30	ns
Chip Enable to Low-Z output	t_{LZ}	Min	0	0	0	0	ns
Output Enable to Low-Z Output	t_{OLZ}	Min	0	0	0	0	ns
Chip Enable to High-Z Output	t_{HZ}	Min	0	0	0	0	ns
		Max	100	50	40	25	
Output Disable to High-Z Output	t_{OHZ}	Min	0	0	0	0	ns
		Max	100	50	40	25	
Output Hold from Address Change	t_{OH}	Min	40	20	15	10	ns
Write Cycle Time	t_{WC}	Min	750	250	150	100	ns
Chip Enable to End of Write	t_{CW}	Min	750	250	150	100	ns
Address Valid to End of Write	t_{AW}	Min	750	250	150	100	ns
Address Set-Up Time	t_{AS}	Min	0	0	0	0	ns
Write Pulse Width	t_{WP}	Min	400	150	75	50	ns
Write Recovery Time	t_{WR}	Min	0	0	0	0	ns
Write to High-Z Output	t_{WHZ}	Min	0	0	0	0	ns
		Max	150	70	50	30	
Data to Write Time Overlap	t_{DW}	Min	400	150	75	50	ns
Data Hold from Write Time	t_{DH}	Min	75	35	20	15	ns
End Write to Low-Z Output	t_{OW}	Min	40	20	15	10	ns

FIGURE 5: Read Cycle Timing ($\overline{WE}$ = V_{IH})

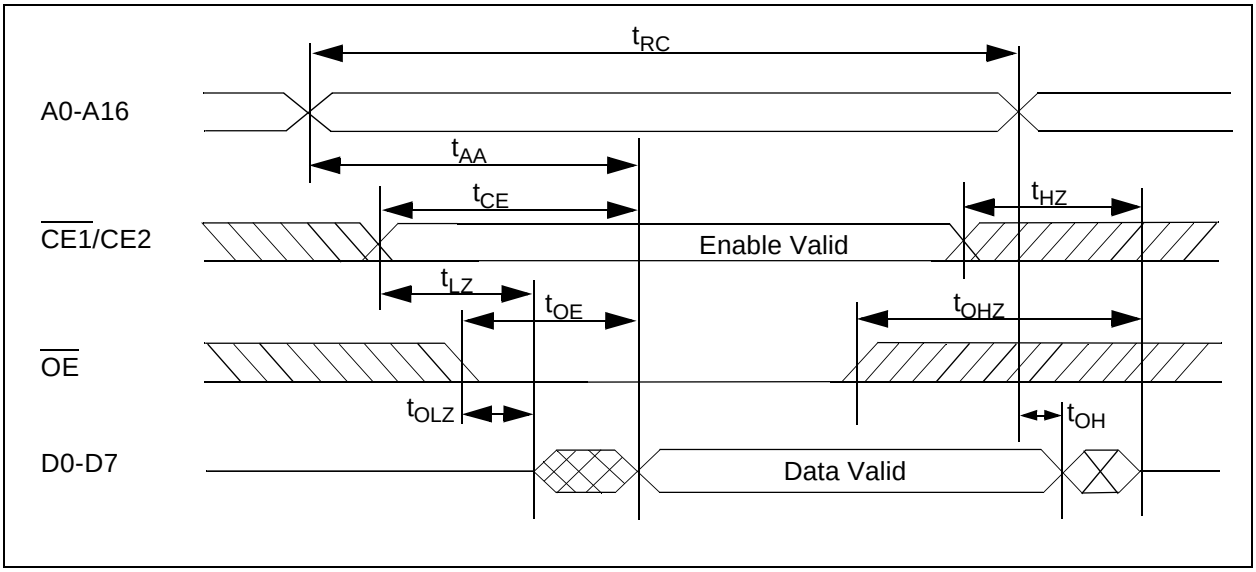

FIGURE 6: Write Cycle Timing ($\overline{OE}$ clock)

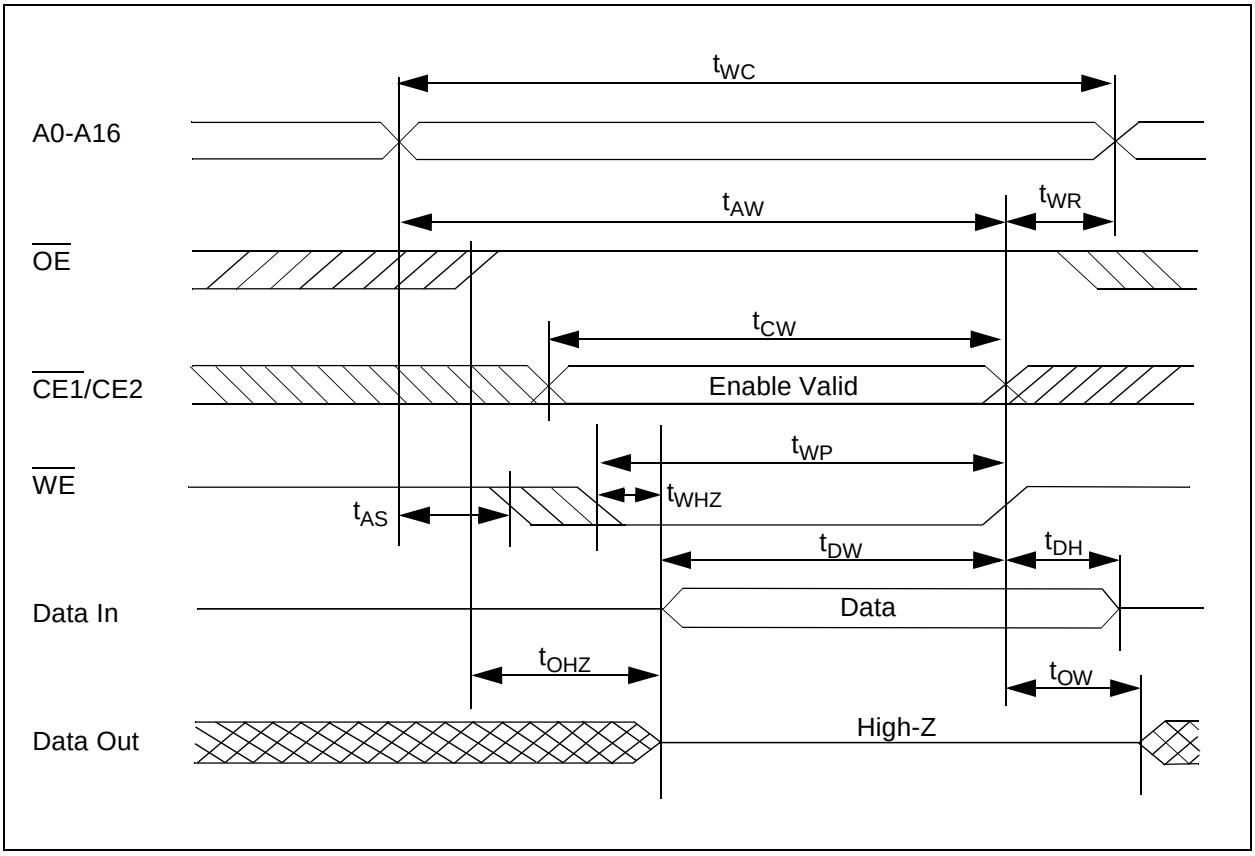

FIGURE 7: Write Cycle Timing ($\overline{OE}$ fixed)

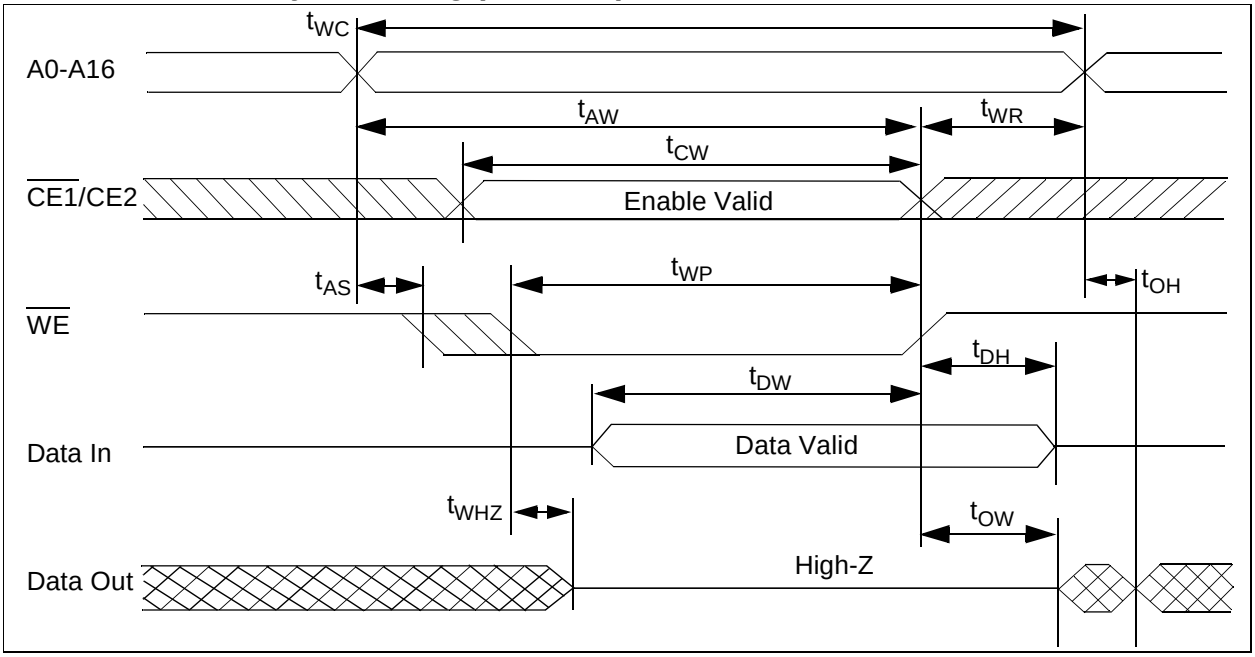

TABLE 7: Ordering Information

Part Number*	Package	Temperature Range	Voltage Range	Speed (@ 2.7V+)
EM127C08N	32 pin STSOP	-20 to +80^{O}C	1.5 to 3.6 V	100 ns

* Please use this part number when ordering this product. This number will be marked on the device package.

TABLE 8: Revision History

Revision #	Date	Change Description
01	Nov. 1, 1998	Initial Production Release