NanoAmp Solutions, Inc.
1982 Zanker Road, San Jose, CA 95112
ph: 408-573-8878, FAX: 408-573-8877
www.nanoamp.com

EM064C16 Family

64Kx16bit Ultra-Low Power Asynchronous Static RAM

Overview

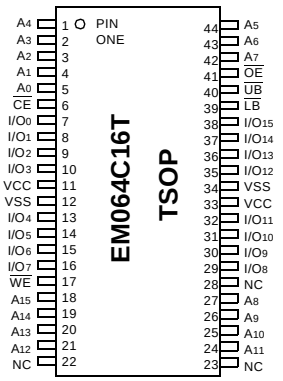
The EM064C16 is an integrated memory device containing a low power 1 Mbit Static Random Access Memory organized as 65,536 words by 16 bits. The device is fabricated using NanoAmp's advanced CMOS process and high-speed/ultra low-power/low-voltage circuit technology. The device pinout is compatible with other standard 64K x 16 SRAMs and is also pin compatible with NanoAmp's 2 and 4 Mbit devices in this family.

These designs are unique in their combination of fast access time and very low power making them very suitable for high performance battery powered applications such as Cellular Phones and hand held GPS navigation devices.

Features

- **Wide Voltage Range:**
  1.5 to 3.6 V
- **Extended Temperature Range**
  -40 to +85 ^{o}C
- **Fast Cycle Time:**
  Standard: T_{ACC} < 100 ns @ 1.8V
  T_{ACC} < 45 ns @ 2.7V
  -35 Version T_{ACC} < 70 ns @ 1.8V
  T_{ACC} < 35 ns @ 2.7V
- **Very Low Operating Current:**
  I_{CC} < 1.0 mA typical at 2V, 1 MHz
- **Very Low Standby Current:**
  I_{SB} < 1 µA @ 55 ^{o}C
- **44-Pin TSOP and BGA Packages**

FIGURE 1: Pin Configurations



	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_2	I/O_1
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	NC	NC	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

48 Pin BGA (top)
7 x 9 mm

TABLE 1: Pin Descriptions

Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
NC	Not Connected
V_{CC}	Power
V_{SS}	Ground

FIGURE 1: Operating Envelope

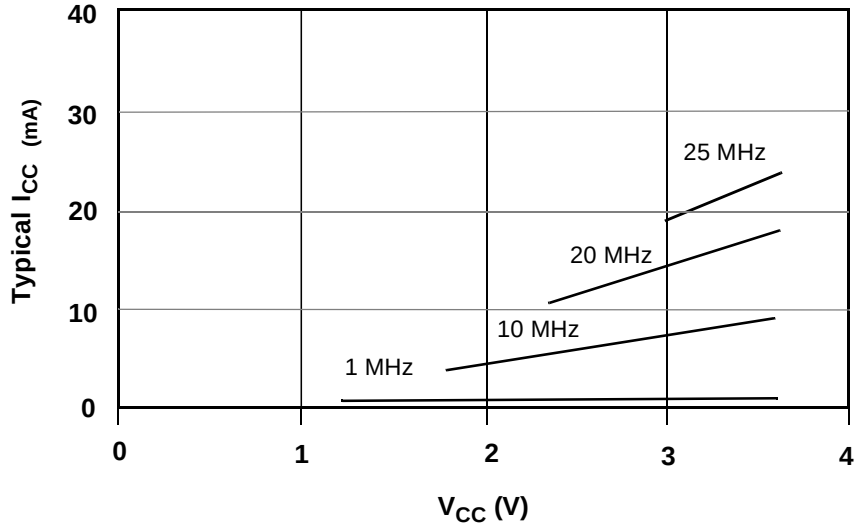


FIGURE 2: Functional Block Diagram

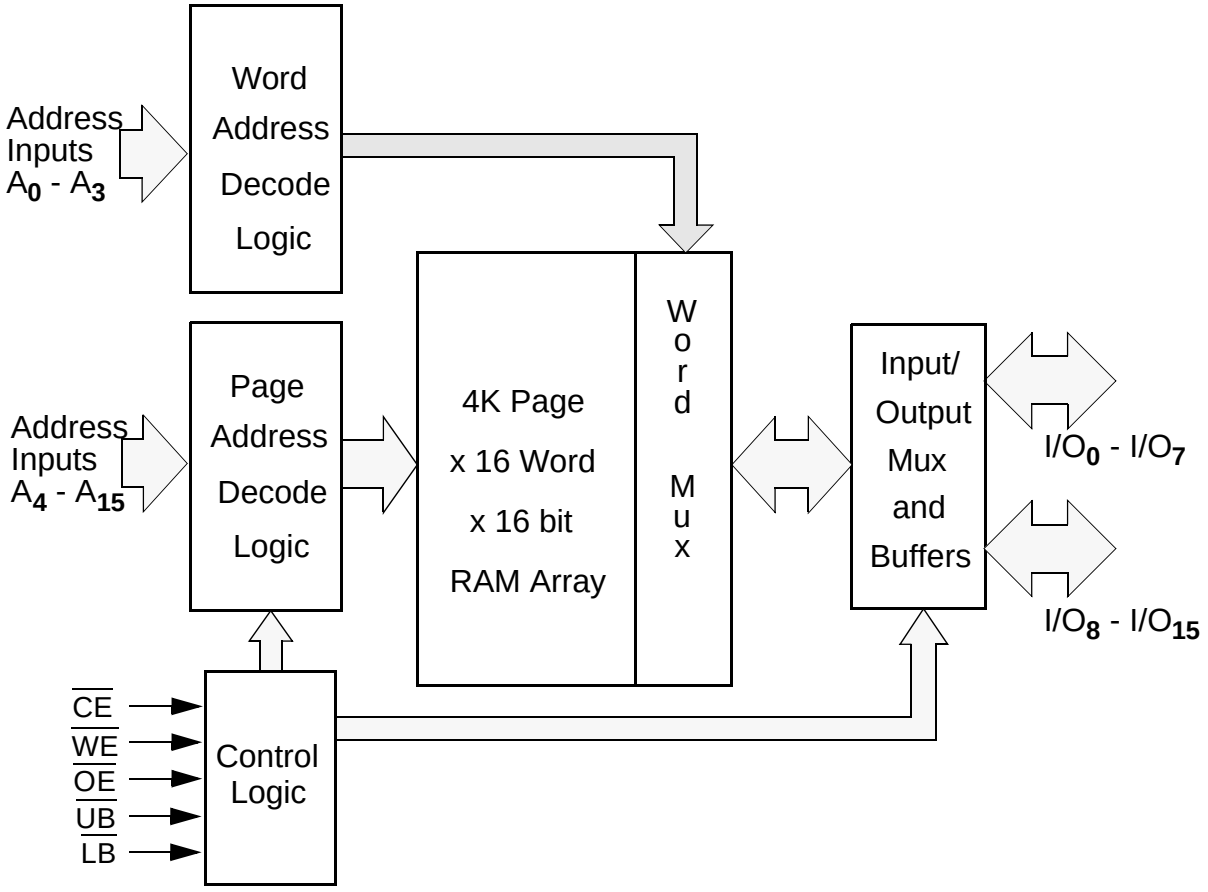


TABLE 2: Functional Description

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O_0 - I/O_{15}[1]	MODE	POWER
H	X	X	High Z	Standby[2]	Standby
L	L	X	Data In	Write[3]	Active -> Standby[4]
L	H	L	Data Out	Read	Active -> Standby[4]
L	H	H	High Z	Active	Standby[4]

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - I/O_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown. If both $\overline{UB}$ and $\overline{LB}$ are in the deselect mode (high), the chip is active but unaffected by $\overline{WE}$ and $\overline{OE}$ commands.
2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.
4. The device will consume active power in this mode whenever addresses are changed. Data inputs are internally isolated from any external influence.

TABLE 3: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

These parameters are verified in device characterization and are not 100% tested

TABLE 4: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	^oC
Operating Temperature	T_A	-40 to +85	^oC
Soldering Temperature and Time	T_{SOLDER}	260 ^oC, 10sec(Lead only)	^oC

* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: Operating Characteristics (Over specified Temperature Range)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		1.5		3.6	V
Data Retention Voltage	V_{DR}	$\overline{CE} = V_{CC}$	1.2			V
Input High Voltage	V_{IH}		$0.7V_{CC}$		V_{CC}+0.5	V
Input Low Voltage	V_{IL}		–0.5		$0.3V_{CC}$	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	V_{CC}–0.3			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.3	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ or $\overline{CE}$ =1 or $\overline{OE}$ =1			0.5	µA
Read/Write Operating Supply Current - Page Access Mode (Note 1)	I_{CC1}	$V_{IN} = V_{CC}$ or 0V $\overline{CE}$ = 0, $\overline{OE}$ = 1		0.8 * f * V	1.0 * f * V	mA
Read/Write Operating Supply Current - Word Access Mode (Note 1)	I_{CC2}	$V_{IN} = V_{CC}$ or 0V $\overline{CE}$ = 0, $\overline{OE}$ = 1		0.15 * f * V	0.2 * f * V	mA
Read/Write Quiescent Operating Supply Current (Note 2)	I_{CC3}	$V_{IN} = V_{CC}$ or 0V $\overline{CE}$ = 0, f = 0, t_A= 55 ^oC			1	µA
Max Standby Current (Note 2)	I_{SB}	$V_{IN} = V_{CC}$ or 0V t_A = 55 ^oC			1	µA
Max Standby Current (Note 2)	I_{SB}	$V_{IN} = V_{CC}$ or 0V t_A = 85^oC			10	µA
Typical Standby Current (Note 2)	I_{SB}	$V_{IN} = V_{CC}$ or 0V t_A = 25 ^oC			0.2	µA

1. Operating current is a linear function of operating frequency and voltage. You may calculate operating current using the formula shown with operating frequency (f) expressed in MHz and operating voltage (V) in volts. Example: When operating at 2 MHz at 2.0 volts the device will draw a typical active current of 0.8*2*2 = 3.2 mA in the page access mode. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
2. This device assumes a standby mode if $\overline{CE}$ is disabled (low). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) regardless of the state of CE. In order to achieve low standby current all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

TABLE 6: Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 30pF
Operating Temperature	-40 to +85 ^{o}C

TABLE 7: Read Cycle Timing

Item	Symbol	Min/ Max	EM064C16			EM064C16-35			Units
			1.5 V	1.8 V	2.7 V - 3.6V	1.5 V	1.8 V	2.7 V - 3.6V	
Read Cycle Time	t_{RC}	Min	200	100	45	120	70	35	ns
Address Access Time	t_{AA}	Max	200	100	45	120	70	35	ns
Chip Enable to Valid Output	t_{CO}	Max	200	100	45	120	70	35	ns
Output Enable to Valid Output	t_{OE}	Max	80	40	20	50	30	20	ns
Byte Select to Valid Output	t_{LB}, t_{UB}	Max	80	40	20	50	30	20	ns
Chip Enable to Low-Z output	t_{LZ}	Min	0	0	0	0	0	0	ns
Output Enable to Low-Z Output	t_{OLZ}	Min	0	0	0	0	0	0	ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	Min	0	0	0	0	0	0	ns
Chip Enable to High-Z Output	t_{HZ}	Min	0	0	0	0	0	0	ns
		Max	60	30	15	40	20	10	
Output Disable to High-Z Output	t_{OHZ}	Min	0	0	0	0	0	0	ns
		Max	60	30	15	40	20	10	
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	Min	0	0	0	0	0	0	ns
		Max	60	30	15	40	20	10	
Output Hold from Address Change	t_{OH}	Min	20	10	5	20	10	5	ns

FIGURE 3: Timing of Read Cycle (1) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

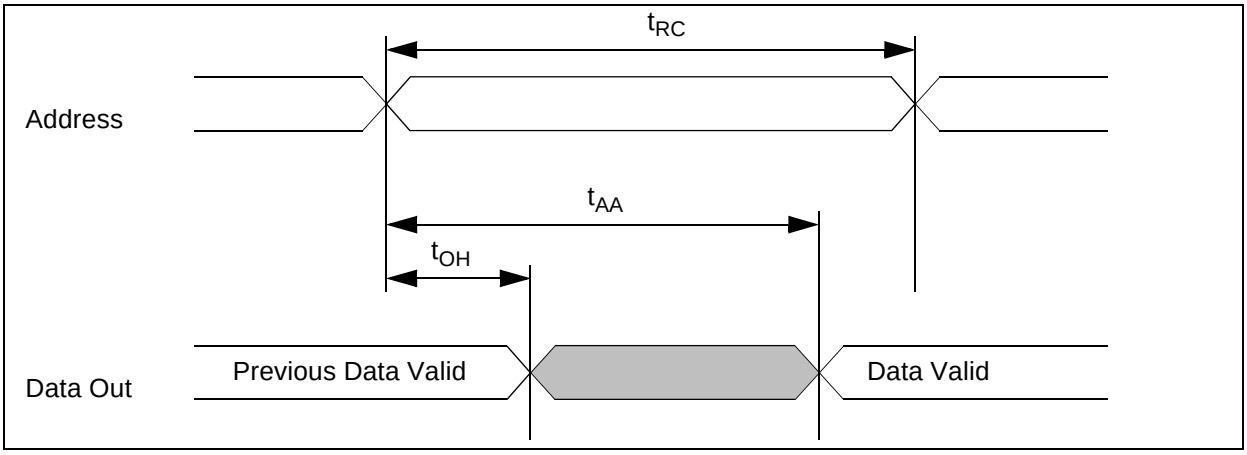


FIGURE 4: Timing Waveform of Read Cycle (2) ($\overline{WE}$ = V_{IH})

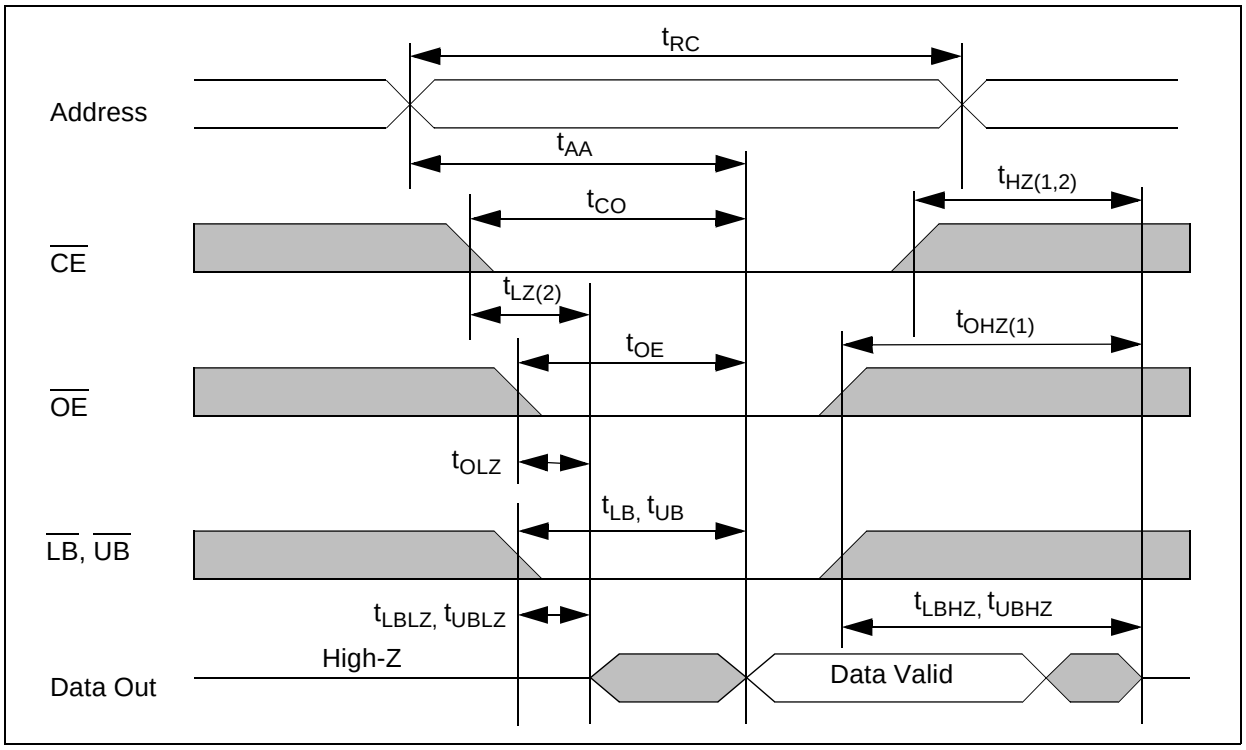


TABLE 8: Write Cycle Timing

Item	Symbol	Min/ Max	EM064C16			EM064C16-35			Units
			1.5 V	1.8 V	2.7 V to 3.6V	1.5 V	1.8 V	2.7 V to 3.6V	
Write Cycle Time	t_{WC}	Min	200	100	45	120	70	35	ns
Chip Enable to End of Write	t_{CW}	Min	200	100	45	120	70	35	ns
Address Valid to End of Write	t_{AW}	Min	100	50	25	60	35	20	ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	Min	200	100	45	120	70	35	ns
Address Set-Up Time	t_{AS}	Min	0	0	0	0	0	0	ns
Write Pulse Width	t_{WP}	Min	100	50	25	60	35	20	ns
Write Recovery Time	t_{WR}	Min	0	0	0	0	0	0	ns
Write to High-Z Output	t_{WHZ}	Min	0	0	0	0	0	0	ns
		Max	30	15	10	20	10	5	ns
Data to Write Time Overlap	t_{DW}	Min	100	50	25	60	35	20	
Data Hold from Write Time	t_{DH}	Min	0	0	0	0	0	0	ns
End Write to Low-Z Output	t_{OW}	Min	60	30	15	40	20	10	
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	Min	0	0	0	0	0	0	ns
		Max	60	30	15	40	20	10	
Output Hold from Address Change	t_{OH}	Min	0	0	0	0	0	0	ns

FIGURE 5: Timing Waveform of Write Cycle (1) ($\overline{WE}$ control)

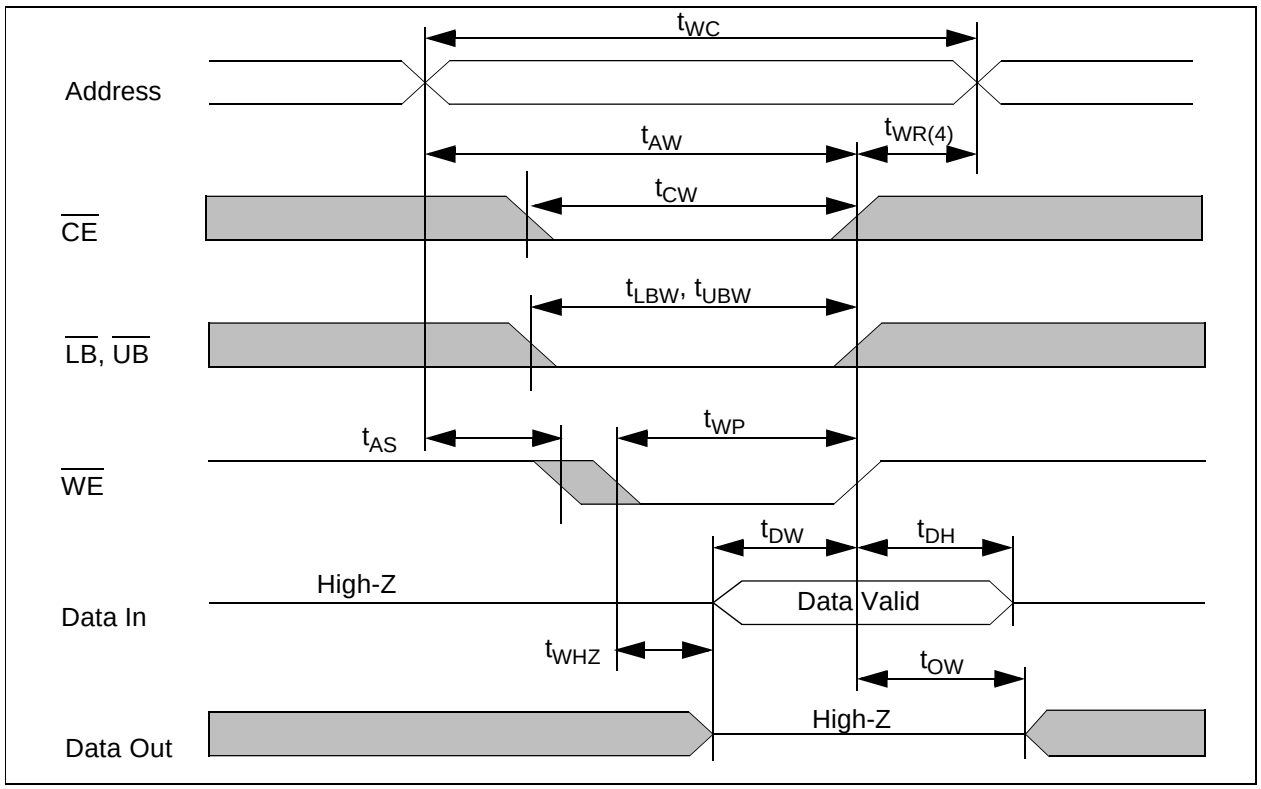


FIGURE 6: Timing Waveform of Write Cycle (2) ($\overline{CE}$ Control)

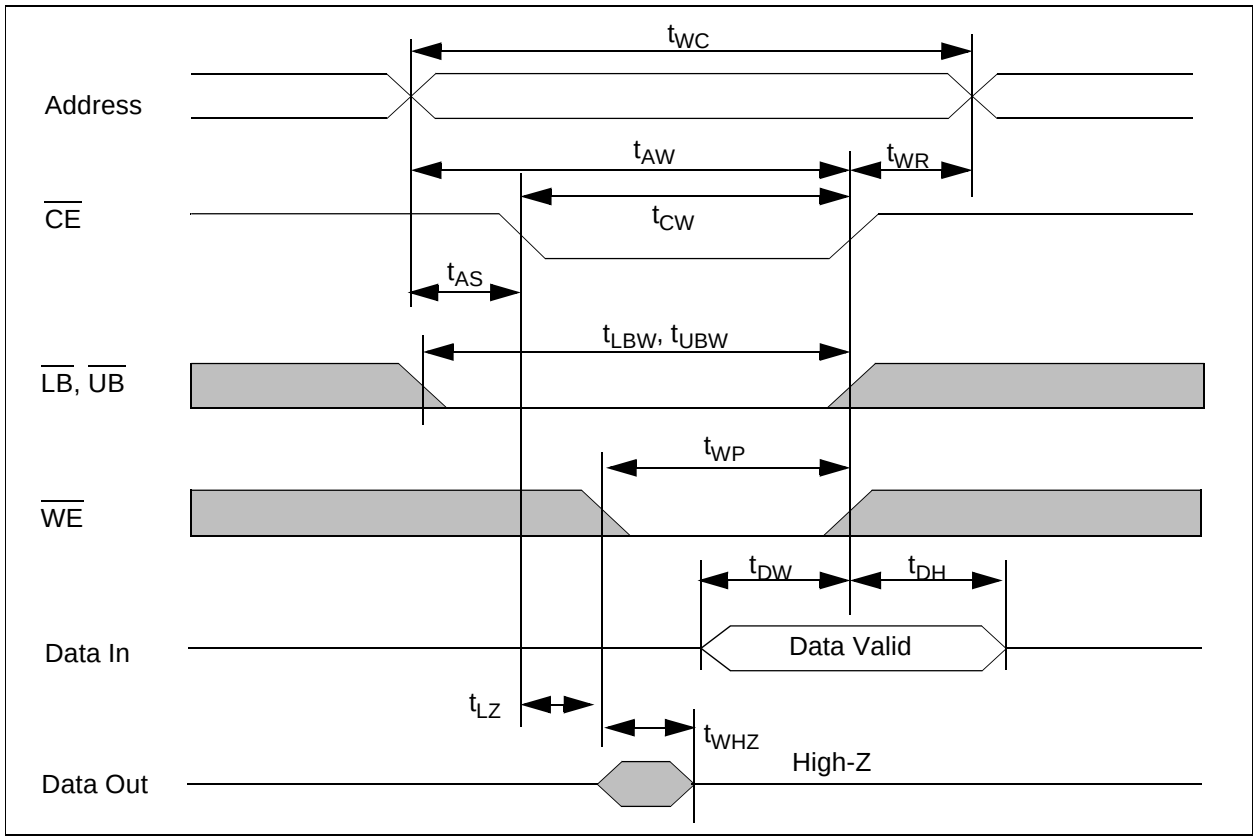


TABLE 9: Ordering Information

Part Number*	Package	Temperature Range	Voltage Range	Speed
EM064C16T	44 pin TSOP	-40 to +85^{o}C	1.5 to 3.6 V	45 ns
EM064C16B	48 pin BGA	-40 to +85^{o}C	1.5 to 3.6 V	45 ns
EM064C16T-35	44 pin TSOP	-40 to +85^{o}C	1.5 to 3.6 V	35 ns
EM064C16B-35	48 pin BGA	-40 to +85^{o}C	1.5 to 3.6 V	35 ns

* This part number must appear on your order.

TABLE 10: Revision History

Revision #	Date	Change Description
01	Oct.10, 1998	Preliminary Release
02	Nov. 2, 1998	Increased “Standard” temperature range to -40 to +85^{o}C Increased “Standard” access times to 45 ns
03	Mar. 22, 1999	Increased 1.8 volt access times to 100 ns
04	May 6, 1999	Eliminated C version, Added -55 part instead. Changed Operating temperature to -20 to +80^{o}C
05	June 9, 1999	Revised Standby and Operating Currents per Characterization
06	August 1, 1999	Corrected Speed Grades: Standard = 45 ns, Speed selected “-35” Changed Temp Range to -40 to +85^{o}C (industrial standard)