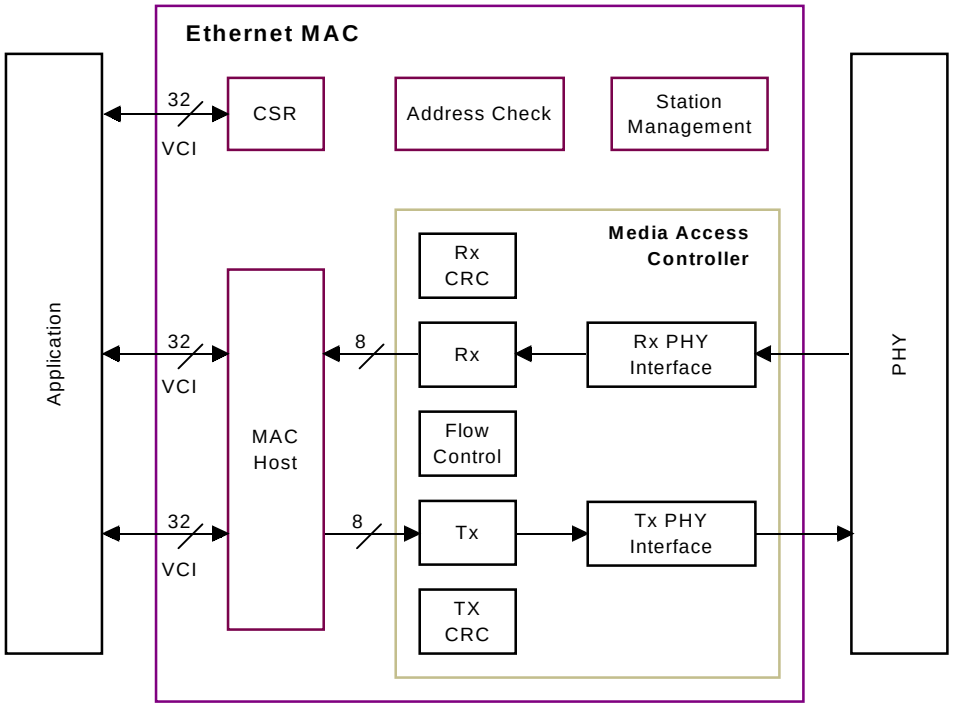
Ethernet MAC
with 10- and 100-Mbps Operation

Highlights

- Optimized for switching, routing, network interface card and system-on-chip applications
- Compliant with IEEE 802.3 and 802.3u specifications
- Supports 10/100 Mbps data transfer rates
- IEEE 802.3 Media Independent Interface (MII), Reduced Media Independent Interface (RMII) and General Purpose Serial Interface (GPSI)
- Supports Full- and Half-Duplex operations
- Virtual LAN (VLAN) support
- Power management: supports remote monitoring (RMON), LAN and magic packets
- RapidScript® utility for fast RMON customization
- Virtual Component Interface (VCI)
- Available in Verilog
- Application integration support
- Approximately 12K gates



Ethernet MAC Block Diagram

Overview

The inSilicon Media Access Controller (MAC) includes the MAC and the MAC test environment. The Ethernet MAC is in a synthesizable Verilog RTL code that provides all the necessary features to implement the layer 2 protocol of the Ethernet standard. It is designed to run according to the IEEE 802.3 and 802.3u specifications that define the 10 Mbps and 100 Mbps Ethernet standards, respectively. The Ethernet MAC also includes:

- Collision detection in Half-Duplex mode (CSMA/CD protocol)
- Support for control frames in Full-Duplex mode (IEEE 802.3x)
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Configurable counters for remote monitoring (RMON)
- Complete status for transmission and reception packets

inSilicon's Ethernet MAC provides Ethernet functionality for switch, NIC and system-on-chip applications. Ethernet MAC implements more than the traditional functionality of standard MACs, including a MAC Host, Station Management, Address Check, and Control/Status Register (CSR) blocks. These additional blocks provide the higher-level system functionality that is traditionally implemented in firmware or using separate products. With these additional capabilities, the Ethernet MAC simplifies the system implementation effort. The Ethernet MAC implements the standard IEEE 802.3 Media Independent Interface (MII) that defines the connection between the PHY and Link layers. It also contains a General Purpose Serial Interface (GPSI) and an optional RMII interface. This is very useful for switch applications that integrate multiple PHYs, as it lowers the pin count required to implement the Link and PHY interface.

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In Half-Duplex mode, the Ethernet MAC supports backpressure. In Full-Duplex mode (IEEE 802.3x), it supports reception and generation of flow control frames.

The Ethernet MAC also supports HomePNA (1.1) and is interoperable with HomePNA (2.0) PHYs such as Lucent's Intrepid™ PHY. Example drivers are also available for HPNA systems.

Packet Handling

Ethernet MAC handles preamble generation and removal. 32-bit CRC generation and checking is performed automatically to verify data integrity. Insertion and stripping of padding bytes on transmission and reception are also available. To minimize system overhead, the Ethernet MAC's flexible address scheme enables data filtering in the network that is not addressed to the node in which it resides. This feature is handled in the Address Check block.

System Management Support

The RMON module contains configurable counters for remote monitoring. These counters track events such as the number of CRC errors, the number of network collisions, and the number of runt frames. The configuration of these counters is done using inSilicon's RapidScript utility.

The optional Station Management block implements the functionality needed to control MII-compatible PHYs. For example, this feature can force PHYs to run at 10 Mbps versus 100 Mbps or configure them to run at Full-Duplex versus Half-Duplex mode. Useful in switch applications, the Station Management function can shut down individual PHY ports.

Application Interface

Ethernet MAC includes the Virtual Component Interface (VCI) as defined by the Virtual Socket Interface (VSI) Alliance. The VCI contains transaction layer logic and FIFOs to handle data transfers between the application and the MAC. The VCI comes with clear documentation, synthesis scripts and testbenches as defined by the VSIA. Using the MAC with a VCI simplifies the task of integrating IP into system designs.

Test Environment

Before the Ethernet MAC is delivered, inSilicon's thorough test methodology verifies functional compliance using random vector testing and implementation in silicon. To facilitate system verification, the MAC is delivered with a test environment that can be used to verify functional compliance to the Ethernet specification.

inSilicon's Support and Maintenance Services

inSilicon's support and maintenance services provide customers with product training classes, product updates, application notes, automated support request and defect tracking, and a staff of dedicated Application Engineers to help you implement inSilicon products in your application. We offer this array of services via our web site, email, and our Customer Support Hot Line.

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