Edge720
500 MHz Pin Electronics Driver, Window Comparator, and Load

Description

The Edge720 is a totally monolithic ATE pin electronics solution manufactured in a high-performance complementary bipolar process.

The three-statable driver is capable of generating 9V swings over a +12V range. In addition, 13V super voltage may be obtained under certain operating conditions. An input power down mode allows extremely low leakage current in HiZ. Thus, the Edge720 can help to eliminate relays that are typically used to isolate devices such as per pin measurement units from the driver/comparator/load.

The load supports programmable source and sink currents of ± 35 mA over a 12V range, or it can be completely disabled. In addition, the load is configurable and may be used as a programmable voltage clamp.

The window comparator spans a 12V common mode range, tracks input signals with edge rates greater than 6 V/ns and passes sub-ns pulses. An input power down mode allows for extremely low leakage measurements.

The inclusion of all pin electronics building blocks into a 52 lead QFP (10 mm body w/ exposed heat sink) offers a highly integrated solution that is traditionally implemented with multiple integrated circuits or discretes.

The Edge720 is an upgrade to the Edge710, with the following improvements:

Load

- Additional VCM_IN Buffer

Comparator

- IPD_C / SUPERV completely power down comparator and load for lowest possible leakage current, and allow safe operation for supervoltage levels.

Package

- Exposed heat slug on the bottom.

Features

- Fully Integrated Three-Statable Driver, Window Comparator, and Dynamic Active Load
- 8.75V Driver, Load, Compare Range
- +13V Super Voltage Capable
- ± 35 mA Programmable Load
- Comparator Input Tracking >6V/ns
- Leakage (L+D+C) < 2 µA (normal mode, typical)
- Leakage (L+D+C) < 30 nA (power-down mode, guaranteed)
- Small footprint (52 lead Exposed Pad QFP)

Applications

- Flash Memory Test
- VLSI Test Equipment
- Mixed-Signal Test Equipment
- Memory Testers (Bidirectional Channels)
- ASIC Verifiers

Functional Block Diagram