APEX Devices

High-Density Embedded Programmable Logic Devices for System-Level Integration

January 2001

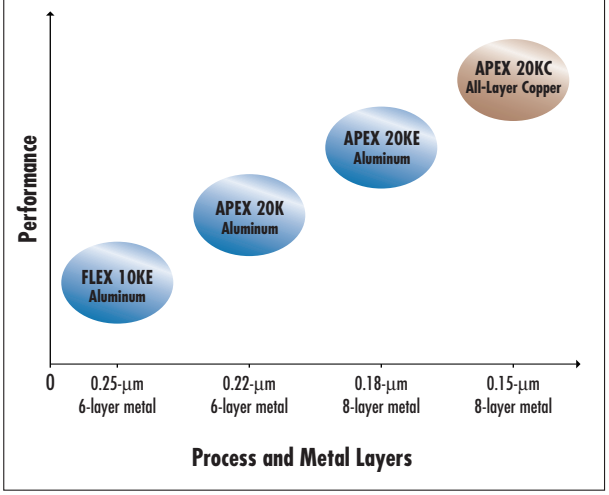
APEX™ programmable logic devices provide the flexibility and high density needed for system-on-a-programmable-chip (SOPC) applications. Its MultiCore™ architecture combines the benefits of look-up table logic with embedded memory, saving board space and simplifying complex system design. APEX devices also offer True-LVDS™ dedicated circuitry for 840-Mbps data transfer rates, the fastest in the industry. APEX 20KC devices, manufactured using all-layer copper interconnect technology, feature increased performance to address the high-bandwidth needs of communications applications.

APEX: A Revolutionary Embedded Architecture

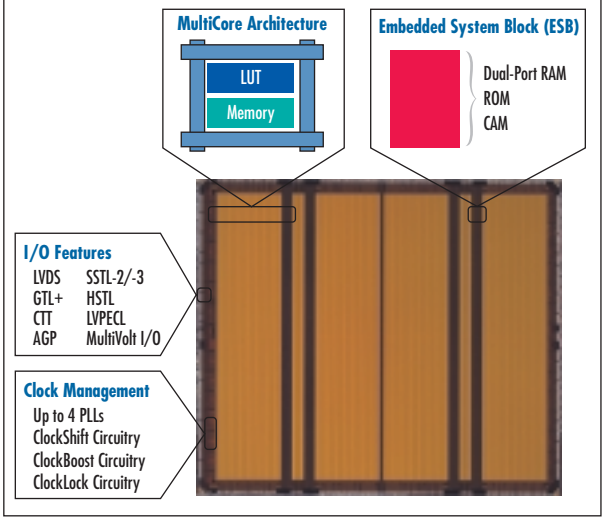
The Altera® APEX™ device family offers complete system-level integration on a single device. With the innovative MultiCore™ architecture, the APEX family combines and enhances the strengths of previous programmable logic device (PLD) architectures and delivers the ultimate in design flexibility and efficiency for high-performance, system-on-a-programmable-chip (SOPC) applications. The new APEX 20KC devices are manufactured on a 0.15 µm all-layer copper interconnect technology to address the high-density, high-performance needs of communication applications.

With densities ranging from 30,000 to over 1.5 million gates (113,000 to over 2.4 million maximum system gates) and performance enhancements from copper interconnect technology, multiple phase-locked loops (PLLs), this family is designed to be 64-bit, 66-MHz PCI and PCI-X compliant. With the APEX True-LVDS circuitry, this family can achieve data transfer rates up to 840 Mbps. The 2.5-V APEX 20K devices are fabricated on an advanced 0.22-µm, six-layer-metal SRAM process. The 1.8-V APEX 20KE devices, which are a functional superset of the APEX 20K devices, utilize a 0.18-µm, eight-layer-metal process. The 1.8-V all-layer copper APEX 20KC devices are fabricated on a 0.15-µm, eight-layer-metal process.

Improved Performance with APEX 20KC Devices



APEX Device Features



Breakthrough MultiCore Architecture

The innovative APEX MultiCore architecture contains two types of PLD structures: the look-up-table (LUT) logic of FLEX® 10K and FLEX 6000 devices and the enhanced embedded memory blocks of FLEX 10KE devices. Both structures are combined into a single integrated architecture, eliminating the need for multiple devices, saving board space, and simplifying the implementation of complex designs.

The MultiCore architecture introduces a new level of hierarchy called the MegaLAB™ structure. Each MegaLAB structure contains 16 logic array blocks (LABs) that consist of 10 logic elements, each of which are used to implement LUT logic, and an advanced embedded structure called embedded system block (ESBs). The MegaLAB local interconnect ties the 16 LABs and the ESBs together without using valuable global routing resources. The MegaLAB structures are connected by the FastTrack® Interconnect continuous routing structure for fast, predictable delays.

APEX Highlights

Feature	Benefit
840-MHz data rates	High-speed I/O interface to provide a true system-level programmable solution
All-layer copper interconnect	Improves performance by 25% to 35% over 0.18 µm aluminum-based devices
MultiCore architecture	Integrates LUT logic and memory into a single architecture
Embedded system block (ESB)	Implements dual-port RAM, first-in first-out (FIFO), ROM, and CAM
PCI compliance	Meets all specifications for 64-bit, 66-MHz PCI compliance and PCI-X support
Support for emerging I/O standards	Supports LVDS, LVTTL, LVCMOS, GTL+, CTT, AGP, HSTL, LVPECL, and SSTL-2/-3 I/O standards
SignalTap® logic analysis	Improves verification of chip functionality
Density up to 1.5 million gates (2.4 million system gates)	Addresses system-level density needs
1.8-V and 2.5-V operation	Reduces power consumption
Up to four phase-locked loops (PLLs)	Supports ClockLock™, ClockBoost™, and ClockShift™ circuitry, and 1x to 160x clock multiplication, and 1 to 256 clock division with an extended frequency range
MultiVolt I/O operation	Ideal for mixed-voltage systems
FineLine BGA™ packaging	Area-optimized, better thermal characteristics, high-pin-count BGA offerings and packaging migration flexibility
Vertical migration	Addresses changing density without the need to re-spin the board

APEX 20KC Device Features (1.8 V)

Device	EP20K100C	EP20K200C	EP20K400C	EP20K600C	EP20K1000C	EP20K1500C
Maximum system gates	263,000	526,000	1,052,000	1,537,000	1,772,000	2,392,000
Logic elements	4,160	8,320	16,640	24,320	38,400	51,840
Maximum RAM bits	53,248	106,496	212,992	311,296	327,680	442,368
Phase-locked loops (PLLs)	2	2	4	4	4	4
Speed grades[1]	-7, -8, -9	-7, -8, -9	-7, -8, -9	-7, -8, -9	-7, -8, -9	-7, -8, -9

Notes: [1] -7 is the fastest speed grade in the APEX 20KC family.

APEX 20KE Device Features (1.8 V)

Device	EP20K30E	EP20K60E	EP20K100E	EP20K160E	EP20K200E	EP20K300E	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	113,000	162,000	263,000	404,000	526,000	728,000	1,052,000	1,537,000	1,772,000	2,392,000
Logic elements	1,200	2,560	4,160	6,400	8,320	11,520	16,640	24,320	38,400	51,840
Maximum RAM bits	24,576	32,768	53,248	81,920	106,496	147,456	212,9924	311,296	327,680	442,368
Phase-locked loops (PLLs)	2	2	2	2	2	4	4	4	4	4
Speed grades[1]	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3
Maximum user I/O pins	128	196	246	316	376	408	488	588	708	808
Package	Maximum User I/O Pins									
144-Pin TQFP[2]	92	92	92	88						
144-Pin FineLine BGA[3]	93	93	93							
208-Pin PQFP[4]	125	148	151	143	136					
240-Pin PQFP		151	151	175	168	152				
324-Pin FineLine BGA	128	196	246							
356-Pin BGA			246	271	271					
484-Pin FineLine BGA				316	376					
652-Pin BGA					376	408	488	488	488	488
672-Pin FineLine BGA					376	408	488	508	508	
1,020-Pin FineLine BGA "F33"								588	708	808

Notes: [1] -1 is the fastest speed grade in the APEX 20K and APEX 20KE families
[2] TQFP: thin quad flat pack
[3] BGA: ball-grid array
[4] PQFP: plastic quad flat pack

APEX 20K Device Features (2.5 V)			
Device	**EP20K100**	**EP20K200**	**EP20K400**
Maximum system gates	263,000	526,000	1,052,000
Logic elements	4,160	8,320	16,640
Maximum RAM bits	53,248	106,496	212,992
Phase-locked loops (PLLs)	1	1	1
Speed grade	-1, -2, -3	-1, -2, -3	-1, -2, -3
Maximum user I/O pins	252	382	502
Package	**Maximum User I/O Pins**		
144-Pin TQFP	101		
144-Pin FineLine BGA	106		
208-Pin PQFP	159	144	
240-Pin PQFP	189	174	
324-Pin FineLine BGA	252		
356-Pin BGA	252	277	
484-Pin FineLine BGA		382	
652-Pin BGA			502
672-Pin FineLine BGA			502

CAM Applications	
Address translation	Packet header identification
Cache tagging	Pattern recognition
IP filtering	Switch address mapping
MAC address look-up	VPI/VCI translation in ATM switches

Embedded System Block Configuration

Embedded system blocks are the heart of the MultiCore architecture. The 2,048 programmable bits of each APEX ESB can be configured as dual-port RAM, ROM, or content-addressable memory (CAM).

Embedded Dual-Port RAM

APEX ESBs support dual-port RAM with independent read/write ports, synchronous or asynchronous RAM operation, and high-speed first-in first-out (FIFO) performance in a wide range of RAM widths and depths (128 × 16, 256 × 8, 512 × 4, 1,024 × 2, and 2,048 × 1). APEX ESBs also support 225-MHz cache RAM performance and ROM performance over 230 MHz. Multiple ESBs can be combined to build wider and deeper memories.

High-Performance CAM

Within APEX 20KE and APEX 20KC devices, ESBs can be configured as CAM, a parallel processing memory that facilitates fast address search functions. CAM operates like reverse RAM: while RAM receives an address input and supplies data output, CAM receives data input and supplies the address that contains the input data.

CAM is commonly used in data communication applications. Because the APEX 20KE and APEX 20KC CAM functions as a high-speed parallel comparator, it opens up many new applications for PLD designs. APEX CAM supports single match, multiple match, fast multiple match, and ternary CAM.

Each ESB can be configured as a 32-word × 32-bit CAM, and ESBs can be cascaded to build larger CAMs. The integrated CAM in APEX 20KE and APEX 20KC devices offers considerable gains in system performance and configuration flexibility relative to discrete CAM solutions.

High-Bandwidth, Low-Voltage I/O

The demand for higher system performance and lower supply voltages is growing. APEX 20KE and APEX 20KC devices support multiple I/O interfacing standards, including LVTTL, LVCMOS, GTL+, SSTL-3/2, HSTL, AGP, CTT, LVPECL, and LVDS with performance up to 840 Mbps. All APEX devices support the Altera MultiVolt™ I/O interface, which is ideal for mixed-voltage systems.

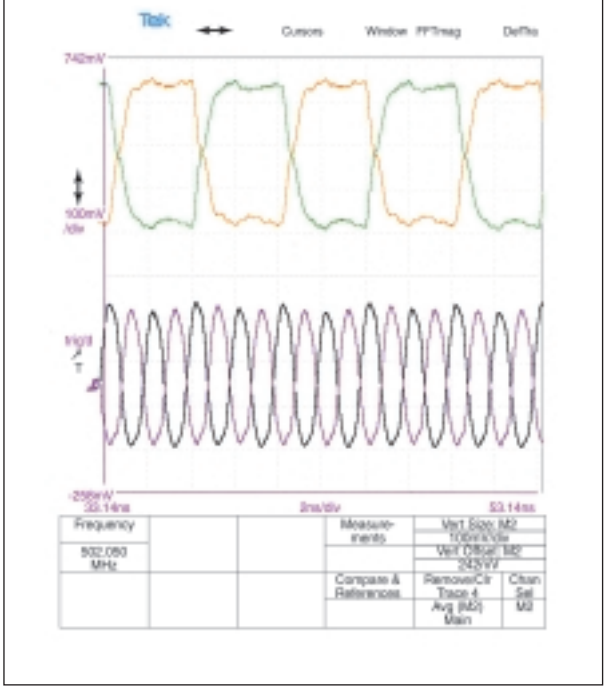
Enhanced Phase-Locked Loop

To increase system-clock rates, APEX 20KE and APEX 20KC devices feature up to four PLLs with enhanced ClockLock™, ClockBoost™, and ClockShift™ circuitry. The ClockLock circuitry uses a synchronizing PLL with an extended frequency range that reduces clock delay and skew within the device. The ClockBoost circuitry provides a clock multiplier that allows the designer to distribute a low-speed clock and to multiply that clock on the device. It also allows for resource-sharing within the device and enhances device area efficiency. The ClockShift circuitry provides a programmable clock delay and phase-shift capability.

High-Bandwidth True-LVDS Support

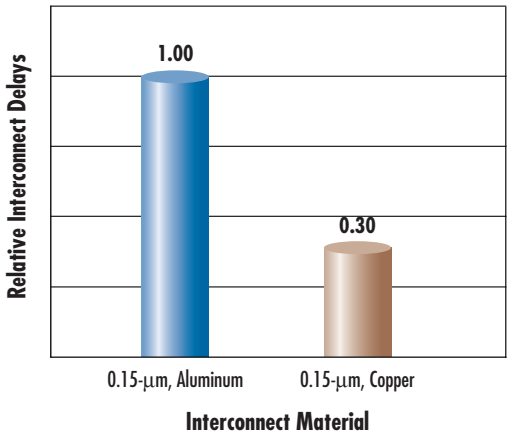
The APEX 20KE and APEX 20KC I/O interface meets 840 Mbps data transfer rate specifications and supports data transfer rates up to 1 Gbps under laboratory conditions. With dedicated built-in True-LVDS circuitry, the APEX 20KE and APEX 20KC LVDS supports programmable bandwidths up to 26 Gbps. APEX devices offer the highest performance, highest bandwidth SOPC solution for high-speed data transmission designs.

APEX 20KE LVDS Running at 1 Gbps Data Transfer Rate*



*Data taken under laboratory conditions.

Aluminum vs. Copper Delays



Greater Performance with All-Layer Copper Interconnect

APEX 20KC devices offer improved internal and I/O performance to address the high-density, high-performance needs of communication applications. With internal performance improvements of 25% to 35% and I/O transmission speeds up to 840 Mbps, these devices are ideal for applications such as OC-192 and SONET SDH protocol, as well as WAN and gigabit Ethernet applications.

APEX 20KC devices build on the state-of-the-art features offered in the industry-leading APEX 20KE devices. Combined with the revolutionary MultiCore architecture, a wide density range, and advanced FineLine BGA package offering up to four PLLs and multiple user-selectable I/Os, the APEX 20KC devices provide even greater system-level integration.

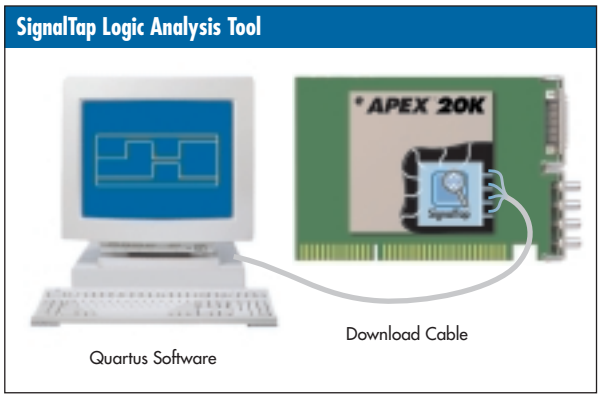
Copper technology replaces aluminum in the APEX 20KC devices for routing structure performance enhancements. Copper has low resistivity and better electro-migration characteristics, making it one of the best-known electrical conductors. Interconnect delays are 70% lower than aluminum delays, which translates to significant core performance improvements. Copper is also more scalable than aluminum, resulting in smaller die size, enhanced internal performance and speed.

The six APEX 20KC devices range in density from 100,000 to 1.5 million system gates (263,000 to 2.4 milliion maximum system gates) with embedded memory ranging from 53,248 to 442,368 RAM bits. Three new speed grades (-7, -8, -9) represent the faster performance of these devices.

Intellectual Property & Quartus Development Tool Simplify Design

Altera's Quartus™ development tool allows designers to process multi-million gate designs using advanced features in PLD development tools. To streamline the development flow and increase productivity, the Quartus software supports system-level solutions, schematic block-level editing, and integrates with standard revision control software. The Quartus software allows designers to implement advanced device features such as CAM, PLL, and LVDS, or to integrate intellectual property (IP) megafunctions easily.

The SignalTap logic analysis tool reduces verification time by enabling engineers to see internal chip signal values while the system is running at speed. Enhanced timing analysis tools support designs with single and multiple clocks as well as designs with multicycle paths. PowerFit™ fitting technology optimizes designs based on the user's timing specifications and meets design requirements with only minimal user effort. The Quartus software uses



NativeLink™ integration to seamlessly interface with third-party EDA software tools, and is "Internet-aware," providing up-to-the-minute information and file exchanges, software updates, and support services through the Internet. Together these features make the Quartus software the ideal platform for multi-million gate designs.

Contact Altera Today

The APEX device family provides a new level of capability and offers a platform for system-on-a-programmable-chip applications. The revolutionary MultiCore architecture brings together the power of LUT logic and embedded memory for system-level integration. Call Altera today to learn more about this multi-million-gate programmable logic family or visit the Altera world-wide web site at **http://www.altera.com**.

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