ACEX Devices

Low-Cost Solutions for High Volume Applications

December 2000

The look-up table (LUT)-based ACEX™ programmable logic device (PLD) family provides value and performance for cost-sensitive, volume-driven applications. These devices are ideal for the communications and consumer marketplaces in applications such as cable modems, xDSL modems, low-cost switches, and routers.

ACEX devices have the low-cost advantages of application-specific integrated circuits (ASICs) and application-specific specialized products (ASSPs), with the added benefits of fast time-to-market and programmable flexibility. ACEX devices offer in-circuit reconfigurability (ICR), eliminating costly delays by allowing designers to quickly implement complete design revisions. These devices are supported by Altera's powerful development software and pre-optimized, drop-in intellectual property megafunctions, further reducing time-to-market. Products can be designed, revised, released, and updated with minimal complications or delays.

Cutting-Edge ACEX Family

The ACEX 1K family, which is based on an advanced cost-optimized 2.5-V SRAM process, ranges from 10,000 to 100,000 gates. The next-generation ACEX family, the ACEX 2K family, will offer densities ranging from 30,000 to 160,000 gates. Additionally, the ACEX 2K family will support a wide range of specialized I/O standards, enabling effective high-speed, board-level communications. Operating at 2.5 V, the ACEX 1K devices are fully 64-bit, 66-MHz compliant and feature embedded dual-port RAM and advanced packaging technologies. ACEX devices support phase-locked loop (PLL) circuitry and can drive two separate ClockLock™- and ClockBoost™-generated signals for extensive clock management capability.

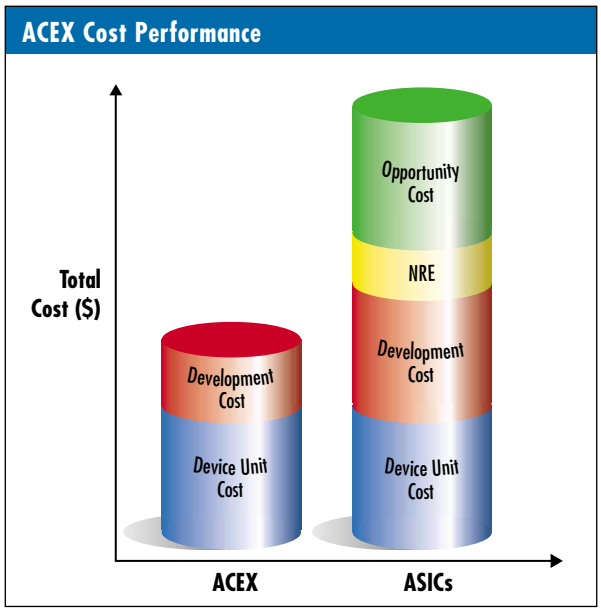
High Performance, Low Cost

High performance, integral to volume-driven telecommunications products, requires a delicate balance between performance and price. ACEX devices meet these requirements. Despite their low price points, system performance in ACEX devices can reach speeds over 100 MHz with minimal intervention. Advanced software fitting techniques place and route designs, achieving accelerated design performance within the ACEX interconnect architecture.

ACEX 1K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	SPEED GRADES
EP1K10	10,000	100-Pin TQFP[1], 144-Pin TQFP[1], 208-Pin PQFP[2], 256-Pin BGA[3]	60, 102, 130, 130	2.5 V	576	12,288	-1, -2, -3
EP1K30	30,000	144-Pin TQFP[1], 208-Pin PQFP[2], 256-Pin BGA[3]	102, 147, 171	2.5 V	1,728	24,576	-1, -2, -3
EP1K50	50,000	144-Pin TQFP[1], 208-Pin TQFP[1], 256-Pin BGA[3], 484-Pin BGA[3]	102, 147, 186, 249	2.5 V	2,880	40,960	-1, -2, -3
EP1K100	100,000	208-Pin TQFP[1], 256-Pin BGA[3], 484 Pin BGA[3]	147, 186, 333	2.5 V	4,992	49,152	-1, -2, -3

Notes: [1] Plastic thin quad flat pack.
[2] Plastic quad flat pack.
[3] Space-saving FineLine BGA™ package.



Total Cost: PLDs vs. ASICs

The ACEX family—as well as all PLDs—offers cost leadership over traditional ASICs. Design costs, development costs, non-recurring engineering (NRE) charges, and lost opportunity costs combine to make the total cost of an ASIC design higher than the cost of Altera's ACEX solution.

ASIC development costs, including the costs of engineering resources and development tools, are significant. Traditional ASIC development requires increased engineering resources to perform software verification and silicon verification, both time- and resource-intensive tasks. With pre-verified silicon, PLDs offer lower engineering resource requirements and faster-time-to-market for customer designs.

Altera ACEX PLDs do not require the NRE charges associated with ASICs. ASIC development also introduces unforeseeable opportunity costs and risks, including respins that result in additional expenses and a protracted development effort, leading to lost revenue and smaller market opportunity.

Versatile Memory Blocks for Embedded Functions

The embedded array blocks (EABs) in ACEX devices are flexible blocks of memory that support a variety of functions, including dual-port RAM with independent read/write ports, synchronous/asynchronous RAM operation, and high performance first-in first-out (FIFO) buffers. Complex memory-intensive designs can be implemented in a single ACEX device without routing and timing performance degradation, as is often the case with devices that feature smaller, segmented RAM structures. For resource optimization, the size of individual EABs can be tailored to suit design requirements, covering a range of widths and depths. Larger aggregate structures can be implemented for memory-intensive functions that require larger blocks of RAM by transparently cascading adjacent EABs. EABs in ACEX devices can also be used for more than just on-chip memory—they can implement specialized arithmetic functions such as multipliers, arithmetic logic units, and sequencers more efficiently than a traditional logic array, making microprocessors, microcontrollers, and complex digital signal processing functions a reality.

ACEX 1K Performance

APPLICATION	RESOURCES USED		PERFORMANCE			UNITS
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	0	200	188	128	MHz
256 x 16-bit RAM read cycle speed[1]	0	1	212	181	131	MHz
16-bit, 8-tap parallel finite impulse response (FIR) filter	420	0	185	175	122	MSPS[2]

Note: [1] This application uses registered inputs and outputs.
[2] Million samples per second.

PLD Value Proposition			
Criteria	ASIC	ASSP	ACEX
No NRE Costs		✓	✓
Fast Development Time		✓	✓
Fast Time-to-Market		✓	✓
Easy Customization	✓		✓
High Flexibility	✓		✓
Product Upgrades			✓

Phase-Locked Loop for Clock Management

Phase-locked loop (PLL) circuitry for clock management is available in ACEX devices for increased clock performance and flexibility. The ClockLock and ClockBoost features permit advanced clock manipulation, efficiently reducing the effects of external board delay and internal device skew while improving input/output timing performance. PLLs provide significant improvements in overall system performance and design versatility, resulting in optimized resource usage and enhanced clock functionality.

Intellectual Property Support for Complex Functions

To further reduce design times, Altera offers a variety of pre-built functional blocks, called megafunctions, that are optimized for the ACEX architecture. These off-the-shelf megafunctions simplify complex design tasks and dramatically shorten design cycles.

Altera offers both Altera-developed MegaCore functions and functions developed through the Altera Megafunction Partners Program (AMPP℠), an alliance between Altera and third-party megafunction developers. Together, Altera's MegaCore and AMPP functions cover a wide range of applications to simplify complex design tasks, dramatically shorten design cycles, and provide results that extend the performance of programmable logic solutions.

Advanced Development Software Support

Altera's design flow equips ACEX developers with a powerful, easy-to-use tool, the MAX+PLUS® II development tool, that contributes to the overall reduction in design cycle times. Advanced fitting techniques ensure optimal placement and routing, culminating in maximized system performance. Seamless integration with synthesis and simulation software from leading EDA vendors as well as state-of-the-art intellectual property cores allow you to take advantage of the full potential of ACEX devices at a minimal cost.

Contact Altera Today

ACEX devices are the ultimate combination of high-performance programmable logic technology with industry-leading, cost-effective price points. An advanced process technology and extensive feature set, coupled with significant pricing advantages and a commitment to technological excellence, has resulted in unprecedented value for the high-volume marketplace. Call Altera today to learn more about the revolutionary ACEX device family or visit the Altera web site at **http://www.altera.com**.

Altera Offices

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
Telephone: (408) 544-7000
http://www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan Ltd.
Shinjuku i-Land Tower 32F
5-1, Nishi-Shinjuku, 6-Chome
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
http://www.altera.com/japan

Altera International Ltd.
Suites 908-920, Tower 1
MetroPlaza
223 Hing Fong Road
Kwai Fong, New Territories
Hong Kong
Telephone: (852) 2487 2030

M-GB-ACEX-01