EPSON

E0C624C

4-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Core CPU Architecture
- Dot Matrix LCD Driver
- Serial Interface
- Programmable SVD Circuit

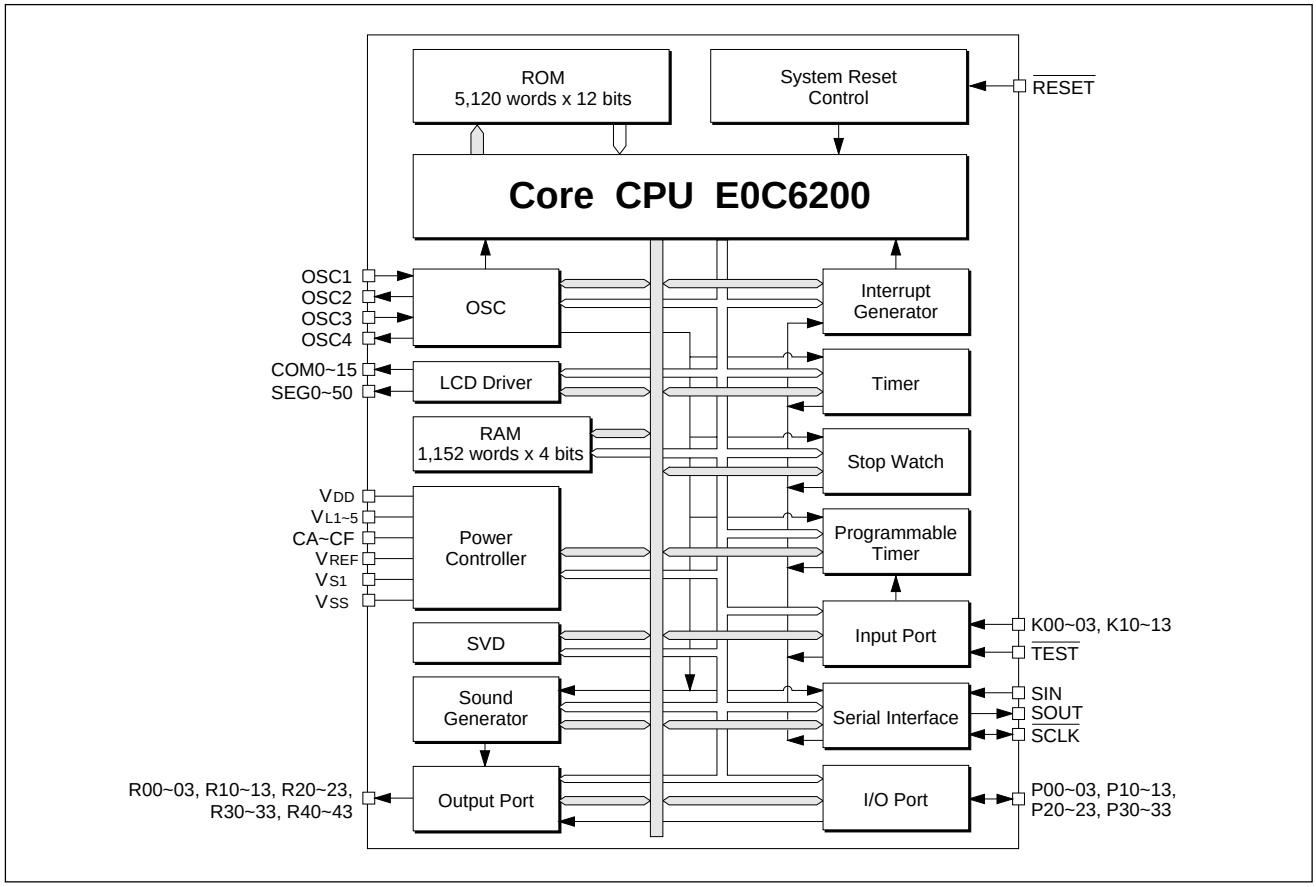
■ DESCRIPTION

The E0C624C is a CMOS 4-bit single chip microcomputer with a Core CPU E0C6200 as main component, ROM, RAM, dot matrix LCD driver, serial interface, time base counter, SVD circuit, and others.
The E0C624C is most suitable for applications with equipment requiring dot matrix display functions.

■ FEATURES

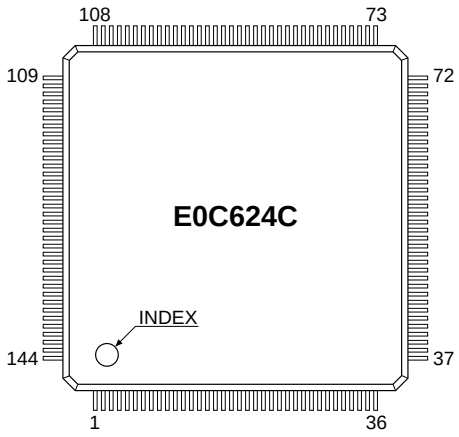
- CMOS LSI 4-bit parallel processing
- Clock ..... OSC1 crystal or CR oscillation circuit : 32.768kHz
  OSC3 ceramic or CR oscillation circuit : 2MHz (Max.)
- Instruction set ..... 108 instructions
- Instruction cycle time ..... Execution at 32.768kHz : 153µsec, 214µsec, 366µsec
  Execution at 2MHz : 2.5µsec, 3.5µsec, 6.0µsec
- ROM capacity ..... 5,120 × 12 bits
- RAM capacity ..... Data : 1,152 × 4 bits
  Segment : 204 × 4 bits
- External memory capacity ..... Read/write (RAM) : 64K × 4 bits (Max.)
  Read only (ROM) : 128K × 4 bits (Max.)
- Input port ..... 8 bits (pull-up resistors are available by mask option)
- Output port ..... 20 bits (can be switched to external memory bus and buzzer output by software)
- I/O port ..... 16 bits (can be switched to external memory bus, special outputs and serial I/O by software)
- Serial interface ..... 8-bit clock synchronous type
- Dot matrix LCD driver ..... 51 segments × 8 commons/16 commons
- Time base counter ..... 3 systems
- Programmable timer ..... 8-bit : 1 system, with event counter function
- Watchdog timer
- Programmable SVD circuit ..... 4 values programmable (2.2V to 4.2V)
- Sound generator ..... With degital envelope function, volume control function (8 levels)
- Interrupt ..... External : Input interrupt 2 systems
  Internal : Clock timer interrupt 3 systems
  Serial interface interrupt 3 systems
- Supply voltage ..... 1.8V to 5.5V
- Current consumption ..... HALT mode (32.768kHz/3.0V) : 2.5µA (Typ.)
  OPERATING mode (2MHz/5.0V) : 1.0mA (Typ.)
- Package ..... QFP8-144pin (plastic)
  Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP8-144pin



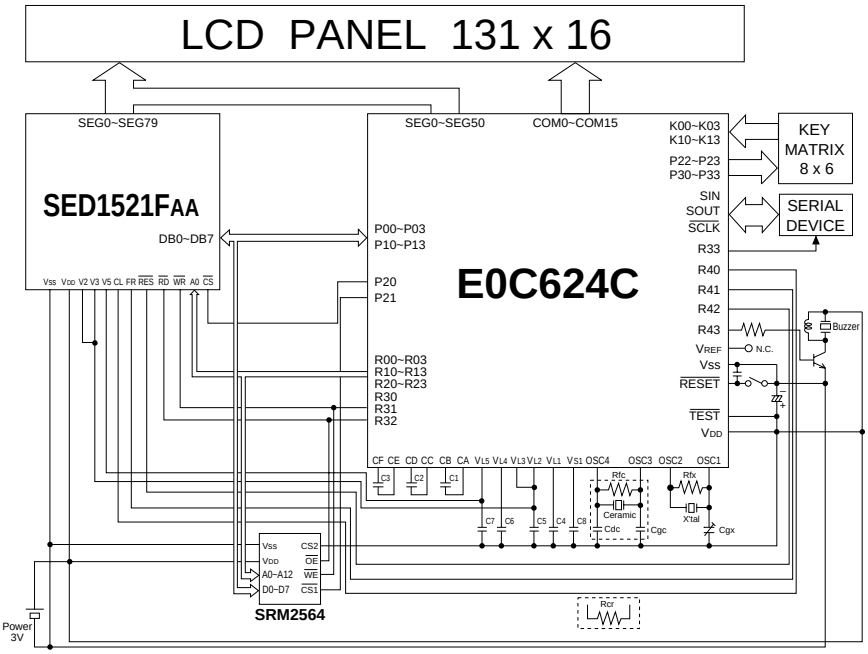
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	CB	30	SEG41	59	SEG15	88	P33	117	R13
2	CA	31	SEG40	60	SEG14	89	P32	118	R12
3	N.C.	32	SEG39	61	SEG13	90	P31	119	R11
4	COM0	33	SEG38	62	SEG12	91	P30	120	R10
5	COM1	34	SEG37	63	SEG11	92	P23	121	R03
6	COM2	35	N.C.	64	SEG10	93	P22	122	R02
7	COM3	36	N.C.	65	SEG9	94	P21	123	R01
8	COM4	37	SEG36	66	SEG8	95	P20	124	R00
9	COM5	38	SEG35	67	SEG7	96	P13	125	V_{SS}
10	COM6	39	SEG34	68	SEG6	97	N.C.	126	$\overline{RESET}$
11	COM7	40	SEG33	69	SEG5	98	P12	127	$\overline{TEST}$
12	COM8	41	SEG32	70	SEG4	99	P11	128	OSC4
13	COM9	42	SEG31	71	SEG3	100	P10	129	OSC3
14	COM10	43	SEG30	72	SEG2	101	P03	130	V_{S1}
15	COM11	44	SEG29	73	SEG1	102	P02	131	OSC2
16	COM12	45	SEG28	74	SEG0	103	P01	132	OSC1
17	COM13	46	SEG27	75	N.C.	104	P00	133	N.C.
18	COM14	47	SEG26	76	$\overline{SCLK}$	105	R43	134	V_{DD}
19	N.C.	48	SEG25	77	SOUT	106	R42	135	V_{REF}
20	COM15	49	SEG24	78	SIN	107	R41	136	V_{L1}
21	SEG50	50	N.C.	79	K13	108	R40	137	V_{L2}
22	SEG49	51	SEG23	80	K12	109	R33	138	V_{L3}
23	SEG48	52	SEG22	81	K11	110	R32	139	V_{L4}
24	SEG47	53	SEG21	82	K10	111	R31	140	V_{L5}
25	SEG46	54	SEG20	83	K03	112	R30	141	CF
26	SEG45	55	SEG19	84	N.C.	113	R23	142	CE
27	SEG44	56	SEG18	85	K02	114	R22	143	CD
28	SEG43	57	SEG17	86	K01	115	R21	144	CC
29	SEG42	58	SEG16	87	K00	116	R20		

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	134	I	Power source (+) terminal
V_{SS}	125	I	Power source (-) terminal
V_{S1}	130	–	Oscillation and internal logic system regulated voltage
V_{L1}–V_{L5}	136–140	–	LCD system power (1/4 or 1/5 bias may be selected by mask option)
V_{REF}	135	O	LCD system power test terminal
CA–CF	2, 1, 144–141	–	Booster capacitor connecting terminal
OSC1	132	I	Crystal or CR oscillation input terminal (selected by mask option)
OSC2	131	O	Crystal or CR oscillation output terminal (selected by mask option)
OSC3	129	I	Ceramic or CR oscillation input terminal (selected by mask option)
OSC4	128	O	Ceramic or CR oscillation output terminal (selected by mask option)
K00–K03, K10–K13	87–85, 83–79	I	Input terminal (Use of pull up resistor is selected by mask option)
P00–P03, P10–P13	104–98, 96	I/O	I/O terminal (Setting for data bus may be selected by mask option)
P20–P23	95–92	I/O	I/O terminal ($\overline{CS}$ output may be selected by mask option)
P30–P33	91–88	I/O	I/O terminal
R00–R03, R10–R13 R20–R23, R30	124–112	O	Output terminal (Setting for address bus may be selected by mask option)
R31	111	O	Output terminal (DC, address or $\overline{WR}$ output may be selected by mask option)
R32	110	O	Output terminal (DC or $\overline{RD}$ output may be selected by mask option)
R33	109	O	Output terminal (DC or $\overline{SRDY}$ output may be selected by mask option)
R40	108	O	Output terminal (DC, CL or $\overline{FOUT}$ output may be selected by mask option)
R41	107	O	Output terminal (DC or FR output may be selected by mask option)
R42	106	O	Output terminal (DC, $\overline{BZ}$ or FOUT output may be selected by mask option)
R43	105	O	Output terminal (DC or BZ output may be selected by mask option)
SIN	78	I	Serial interface input terminal
SOUT	77	O	Serial interface output terminal
$\overline{SCLK}$	76	I/O	Serial interface clock input/output terminal
SEG0–50	74–51, 49–37 34–21	O	LCD segment output terminal
COM0–15	4–18, 20	O	LCD common output terminal
$\overline{RESET}$	126	I	Initial reset input terminal
$\overline{TEST}$	127	I	Test input terminal

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768kHz CI(Max.)=35kΩ
Rfx	Feedback resistor	10MΩ
Cgx	Trimmer capacitor	5~25pF
Ceramic	Ceramic oscillator	500kHz~2MHz
Rfc	Feedback resistor	1MΩ
Cgc	Gate capacitance	100pF
Cdc	Drein capacitance	100pF
Rcr	Resistance for CR oscillation	20kΩ~100kΩ
C1~C3	Voltage booster capacitor (1)~(3)	0.1µF ∗1
C4	Capacitor between V_{DD} and V_{L1}	0.1µF ∗1
C5	Capacitor between V_{DD} and V_{L2}	0.1µF ∗1
C6	Capacitor between V_{DD} and V_{L4}	0.1µF ∗1
C7	Capacitor between V_{DD} and V_{L5}	0.1µF ∗1
C8	Capacitor between V_{DD} and V_{S1}	0.1µF

∗1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C1–C3) and the capacitors between V_{DD} and liquid crystal system power (C4–C7).

Note: The above table is simply an example, and is not guaranteed to work.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *1	P_D	250	mW

*1: In case of plastic package (QFP8-144pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	VSC="0"	-3.8	-3.0	-1.8	V
			VSC="1"	-5.5	-3.0	-2.2	V
			VSC="2"	-5.5	-3.0	-3.5	V
Oscillation frequency (1)	f_{OSC1}			20	32.768	50	kHz
Oscillation frequency (2)	f_{OSC3}	VSC="1"		50	1,000	1,200	kHz
Oscillation frequency (3)	f_{OSC3}	VSC="2"		50	2,000	2,300	kHz
Voltage booster capacitor (1)	C1				0.1		µF
Voltage booster capacitor (2)	C2				0.1		µF
Voltage booster capacitor (3)	C3				0.1		µF
Capacitor between V_{DD} and V_{L1}	C4				0.1		µF
Capacitor between V_{DD} and V_{L2}	C5				0.1		µF
Capacitor between V_{DD} and V_{L4}	C6				0.1		µF
Capacitor between V_{DD} and V_{L5}	C7				0.1		µF
Capacitor between V_{DD} and V_{S1}	C8				0.1		µF

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V,V_{SS}=-3.0V,V_{L1}=-1.0V,V_{L2}=-2.0V,V_{L4}=-3.0V,V_{L5}=-4.0V,f_{OSC1}=32.768kHz,f_{OSC3}=1MHz,Ta=25°C,C1–C8=0.047µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V	K00–03•10–13, P00–03•10–13	0.2•V_{SS}		0	V
Low level input voltage	V_{LIN}	Ta=25°C	P20–P23•30–33, SIN, $\overline{SCLK}$	V_{SS}		0.8•V_{SS}	V
High level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V	$\overline{RESET}$	-0.2		0	V
Low level input voltage	V_{LIN}	Ta=25°C		V_{SS}		V_{SS}+0.2	V
High level input current	I_{IH}	V_{SS}=-3.0V V_{IH}=0V	K00–03•10–13, P00–03•10–13 P20–P23•30–33, SIN, $\overline{SCLK}$ $\overline{RESET}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{SS}=-3.0V V_{IL1}=V_{SS} With pull-up resistor	K00–03•10–13, P00–03•10–13 P20–P23•30–33, SIN, $\overline{SCLK}$ $\overline{RESET}$	-45		-15	µA
Low level input current (2)	I_{IL2}	V_{SS}=-3.0V V_{IL2}=V_{SS} No pull-up resistor	K00–03•10–13, P00–03•10–13 P20–P23•30–33, SIN, $\overline{SCLK}$ $\overline{RESET}$	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03•10–13•20–23•30–33 R00–03•10–13•20–23•30–33 R40•41, SOUT, $\overline{SCLK}$			-1.0	mA
Low level output current (1)	I_{OL1}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	P00–03•10–13•20–23•30–33 R00–03•10–13•20–23•30–33 R40•41, SOUT, $\overline{SCLK}$	4.0			mA
High level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42•43			-2.0	mA
Low level output current (2)	I_{OL2}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	R42•43	8.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–50			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=0V,V_{SS}=-3.0V,V_{L1}=-1.0V,V_{L2}=-2.0V,V_{L4}=-3.0V,V_{L5}=-4.0V,f_{OSC1}=32.768kHz,f_{OSC3}=1MHz,Ta=25°C,C1–C8=0.047µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Liquid crystal drive voltage (Normal mode)	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (No panel load)		1/2•V_{L2} -0.1		1/2•V_{L2} ×0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (No panel load)	LC="0"	Typ.×1.12	-1.80	Typ.×0.88	V
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"		-2.17		
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
			LC="13"		-2.48		
			LC="14"		-2.53		
			LC="15"		-2.59		
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (No panel load)		3/2•V_{L2}		3/2•V_{L2} ×0.95	V
	V_{L5}	Connect 1MΩ load resistor between V_{DD} and V_{L5} (No panel load)		2•V_{L2}		2•V_{L2} ×0.95	V
Liquid crystal drive voltage (Heavy load protection mode)	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (No panel load)	LC="0"	Typ.×1.12	-0.92	Typ.×0.88	V
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"		-1.11		
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
			LC="13"		-1.26		
			LC="14"		-1.29		
			LC="15"		-1.32		
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (No panel load)		2•V_{L1}		2•V_{L1} ×0.90	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (No panel load)		3•V_{L1}		3•V_{L1} ×0.90	V
	V_{L5}	Connect 1MΩ load resistor between V_{DD} and V_{L5} (No panel load)		4•V_{L1}		4•V_{L1} ×0.90	V
SVD voltage	V_{SVD0}	SVC="0"		-2.35	-2.20	-2.05	V
	V_{SVD1}	SVC="1"		-2.70	-2.50	-2.30	V
	V_{SVD2}	SVC="2"		-3.30	-3.10	-2.90	V
	V_{SVD3}	SVC="3"		-4.50	-4.20	-3.90	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{Hlt}	During HALT	No panel load *1		2.5	5.0	µA
	I_{EX1}	During operation at 32kHz			6.5	9.0	µA
	I_{EX2}	During operation at 1MHz	No panel load *2		400	600	µA
	I_{EX3}	During operation at 2MHz	No panel load *3		1,000	1,500	µA
Current consumption (OSC1•CR oscillation)	I_{Hlt}	During HALT	No panel load *4		20	70	µA
	I_{EX1}	During operation at f_{OSC1}			25	80	µA
	I_{EX2}	During operation at 1MHz			420	600	µA
	I_{EX3}	During operation at 2MHz	No panel load *5		1,000	1,500	µA

*1: SVD circuit: OFF status, VSC = "0", OSC1: oscillating with crystal, OSCC= "0"
*2: SVD circuit: OFF status, VSC = "1", OSC1: oscillating with crystal
*3: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with crystal, V_{SS} = -5.0V
*4: SVD circuit: OFF status, VSC = "0" or "1", OSC1: oscillating with CR, OSCC = "0", R_{OSC} for OSC1 = 1.6MΩ
*5: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with CR, OSCC = "0", R_{OSC} for OSC1 = 1.6MΩ

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_{GX}=25pF, C_{DX}=built-in, R_{fX}=10MΩ, VSC="0", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			5	Sec
Built-in capacitance (drain)	C_D	Package as assembled		22		pF
		Bare chip		21		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{S1}	200			MΩ

OSC1 CR oscillation circuit

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, VSC="0" or "1", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		5	%
Oscillation frequency	f_{CR}	R_{OSC}=1.6MΩ	32×70%	32	32×130%	kHz

OSC3 CR oscillation circuit (1)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, VSC="1", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		5	%
Oscillation frequency	f_{CR}	R_{OSC}=40kΩ	860×70%	860	860×130%	kHz

OSC3 CR oscillation circuit (2)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-5.0V, VSC="2", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-5		5	%
Oscillation frequency	f_{CR}	R_{OSC}=20kΩ	1.7×70%	1.7	1.7×130%	MHz

OSC3 ceramic oscillation circuit (1)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, VSC="1", Ceramic: CSB 1000J (Murata Mfg. Co.), C_{GC}=C_{DC}=100pF, R_{fC}=1MΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-3		3	%

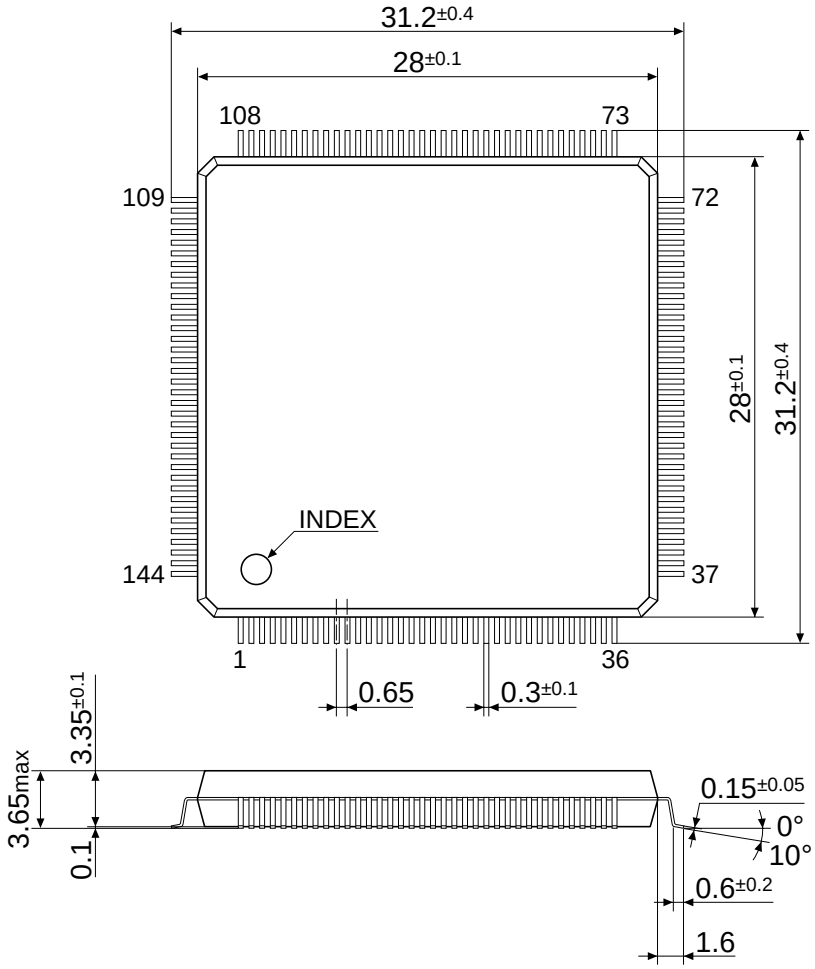
OSC3 ceramic oscillation circuit (2)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-5.0V, VSC="2", Ceramic: CSA 2.00MG (Murata Mfg. Co.), C_{GC}=C_{DC}=100pF, R_{fC}=1MΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-3		3	%

■ PACKAGE DIMENSIONS

Plastic QFP8-144pin



Unit: mm

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Electric Device Information of EPSON WWW server

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