élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1501C—SLIDE*

Differential Line Driver/Receiver

Features

- Complete ADSL differential driver and receiver
- 45 $V_{p\text{-}p}$ differential output drive into 200Ω
- −60 dB typical output distortion at full output at 2 MHz
- −73 dB typical receive distortion at 15 $V_{p\text{-}p}$ levels at 2 MHz
- Drives 8 single-ended video loads, or 4 S-VHS loads, or 4 differential video loads
- Power surface-mount package

Applications

- ADSL line interface
- HDSL line driver
- Video distribution amplifier
- Video twisted-pair line driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1501CM	−40°C to +85°C	20-Lead SO	MDP0027

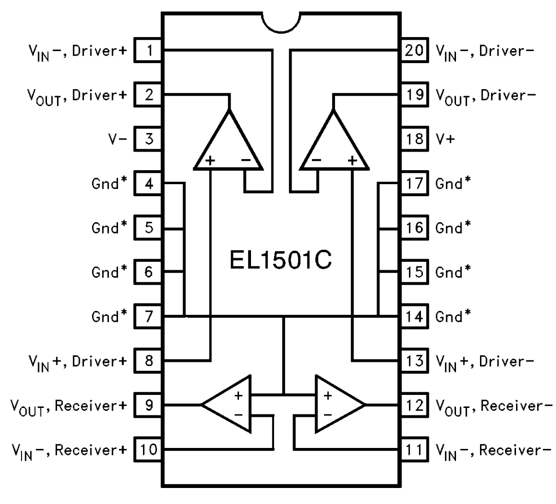
General Description

The EL1501C contains two wideband high-voltage drivers and two receive amplifiers. It is designed to drive 45 $V_{p\text{-}p}$ signals at 2 MHz into a 200Ω load differentially with very low distortion. The receive amplifiers also provide very low distortion and noise, and with external resistors can be wired as a hybrid coupler.

All amplifiers are of the current-feedback type, giving high slewrates while consuming moderate power. They retain frequency response over a wide range of externally set gains.

The EL1501C operates on ±5V to ±15V supplies, and retains its bandwidths and linearities over the supply range.

Eight center package pins are used as ground connections and heat spreaders, allowing a dissipation of 2W at the maximum ambient temperature of 85°C.



*Subscriber Line Interface Device

March 1995 Rev. A

EL1501C—SLIDE*
Differential Line Driver/Receiver

Absolute Maximum Ratings (T_A = 25°C)

V_S	V+ to V− Supply Voltage	33V
V+	V+ Voltage to Ground	−0.3V to +33V
V−	V− Voltage to Ground	−33V to 0.3V
V_{IN}+	Driver V_{IN}+ Voltage	V− to V+
I_{IN}	Current into any Input	8 mA
I_{OUT}, driver	Output Current from Driver (Static)	75 mA
I_{OUT}, rec	Output Current from Receiver (Static)	15 mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Temperature Range	−40°C to +85°C
T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics
Power supplies at ±15V, R_F for both drivers and receivers is 1 kΩ, R_L for driver is 75Ω, R_L for receiver is 200Ω. T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}, driver	Driver Input Offset Voltage	−30		30	I	mV
ΔV_{OS}, drivers	Driver-to-Driver V_{OS} Mismatch	−10		10	I	mV
I_B+, driver	Non-Inverting Driver Input Bias Current	−10		10	I	μA
I_B−, driver	Inverting Driver Input Bias Current	−40		40	I	μA
ΔI_B−, drivers	Driver-to-Driver I_B− Mismatch	−36		36	I	μA
R_{OL}, drivers	Driver Transimpedance, V_{OUT} from −12V to +12V	0.4	1.6		I	MΩ
V_{OUT}, driver	Driver Loaded Output Swing	±12.0	±13		I	V
V_{OS}, receiver	Receiver Input Offset Voltage	−30		30	I	mV
ΔV_{OS}, receivers	Receiver-to-Receiver V_{OS} Mismatch	−10		10	I	mV
I_B−, receiver	Receiver Inverting Input Bias Current	−15		15	I	μA
ΔI_B−, receiver	Receiver-to-Receiver I_B− Mismatch	−16		16	I	μA
R_{OL}, receiver	Receiver Transimpedance, V_{OUT} from −4V to +4V	2	6		I	MΩ
V_{OUT}, receiver	Receiver Loaded Output Swing	±6.25	±10		I	V
I_S	All Outputs at 0V	30	36	45	I	mA

TD is 3.0in

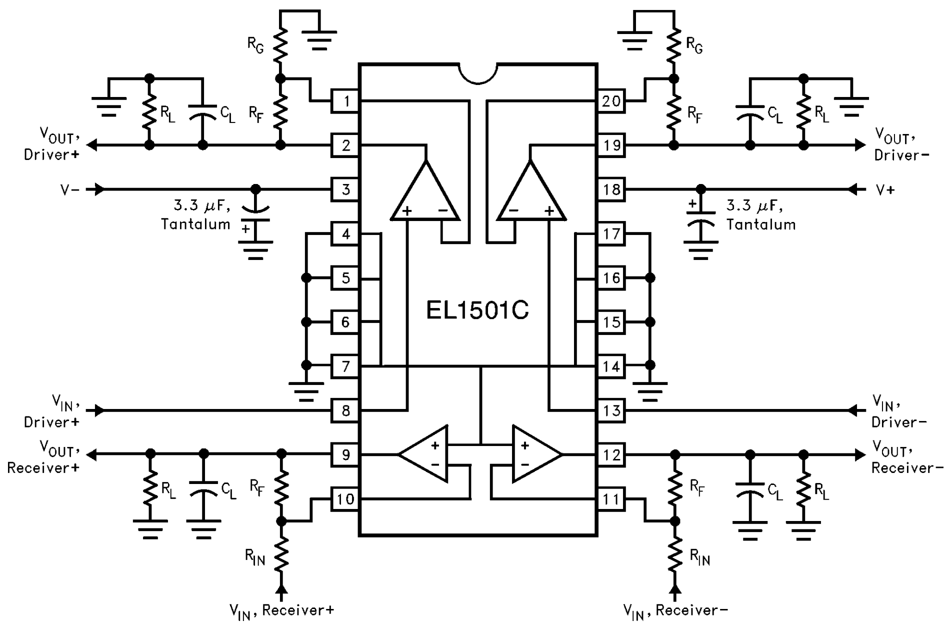
Closed-Loop AC Electrical Characteristics

Power supplies at ±15V, R_F for both drivers and receivers is 510Ω, R_L for drivers is 75Ω, R_L for receivers is 200Ω. C_L = 15 pF. Driver gain is +10 and receiver gain is −1. T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, driver	−3 dB Bandwidth of Driver Amplifiers		63		V	MHz
HD, driver	Total Harmonic Distortion of Driver					
	f = 2 MHz, Supplies at ±15V, 22.5 V_{p-p} Output		−60		V	dBc
	f = 2 MHz, Supplies at ±9V, 10.5 V_{p-p} Output		−66		V	dBc
	f = 300 kHz, Supplies at ±5V, 6 V_{p-p} Output		−71		V	dBc
dG, driver	Driver Differential Gain Error, Standard NTSC Test A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.17		V	%
dθ, driver	Driver Differential Phase Error, Standard NTSC Test A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.06		V	°
SR, driver	Driver Slewrate, V_{OUT} from −10V to +10V Measured at ±5V	TBD	1000		I	V/μsec
e_N, driver	Driver Input Noise Voltage		3.3		V	$nV/\sqrt{Hz}$
i_N, driver	Driver −Input Noise Current		18		V	$pA/\sqrt{Hz}$
BW, receiver	−3 dB Bandwidth of Receive Amplifiers		80		V	MHz
HD, receiver	Total Harmonic Distortion of Receive Amplifiers					
	f = 2 MHz, Supplies at ±15V, 11.25 V_{p-p} Output		−72		V	dBc
	f = 2 MHz, Supplies at ±9V, 5.25 V_{p-p} Output		−71		V	dBc
	f = 300 kHz, Supplies at ±5V, 3 V_{p-p} Output		−73		V	dBc
SR, receiver	Receiver Slewrate, V_{OUT} from −4V to +4V Measured at ±2.5V	TBD	600		I	V/μsec
e_N, receiver	Receiver Input Noise Voltage		3		V	$nV/\sqrt{Hz}$
i_N, receiver	Receiver −Input Noise Current		12		V	$pA/\sqrt{Hz}$

TD is 3.6in

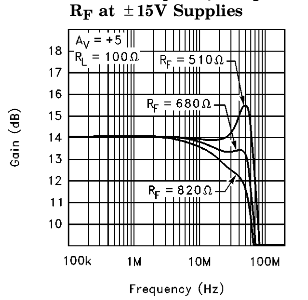
Test Circuit



1501–2

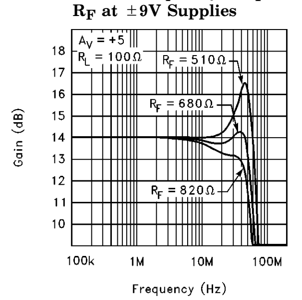
Typical Performance Curves

Driver Frequency Response vs R_F at ±15V Supplies



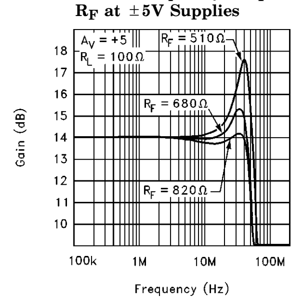
1501–3

Driver Frequency Response vs R_F at ±9V Supplies



1501–4

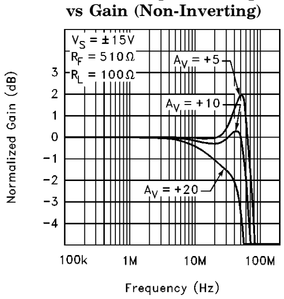
Driver Frequency Response vs R_F at ±5V Supplies



1501–5

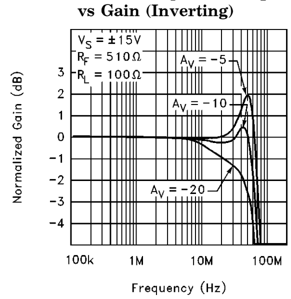
Typical Performance Curves — Contd.

Driver Frequency Response vs Gain (Non-Inverting)



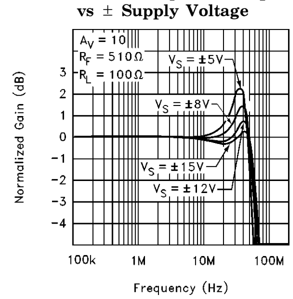
1501-6

Driver Frequency Response vs Gain (Inverting)



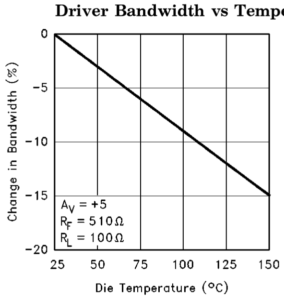
1501-7

Driver Frequency Response vs ± Supply Voltage



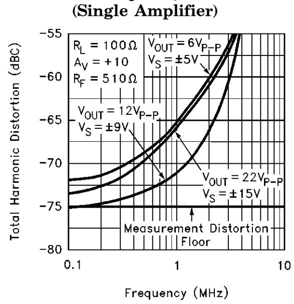
1501-8

Driver Bandwidth vs Temperature



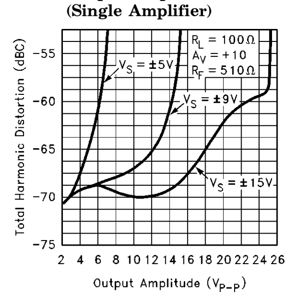
1501-9

Driver Harmonic Distortion vs Frequency (Single Amplifier)



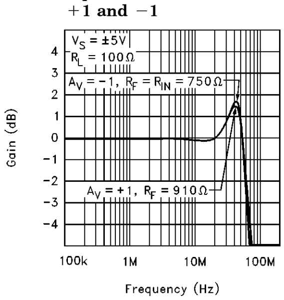
1501-10

Driver Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)



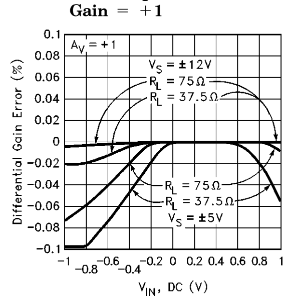
1501-11

Driver Frequency Responses Equalized for Gains of +1 and −1



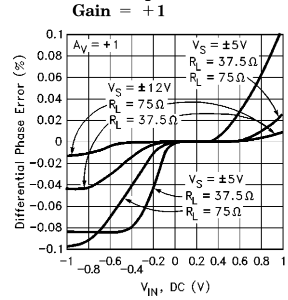
1501-12

Driver Differential Gain Error vs DC Input Offset Gain = +1



1501-13

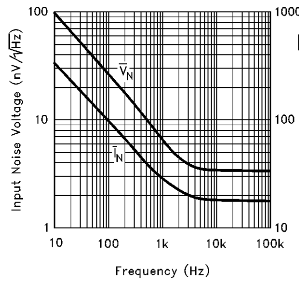
Driver Differential Phase Error vs DC Input Offset Gain = +1



1501-14

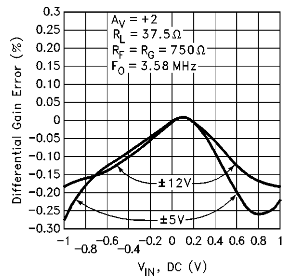
Typical Performance Curves — Contd.

Driver Input Noise Voltage and Current over Frequency



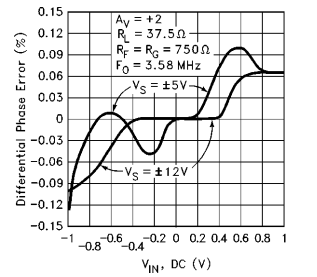
1501-15

Driver Differential Gain Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2



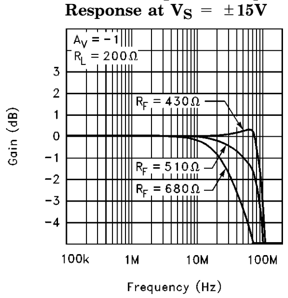
1501-16

Driver Differential Phase Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2



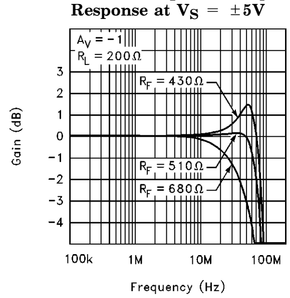
1501-17

Receive Amplifier Frequency Response at $V_S = \pm 15V$



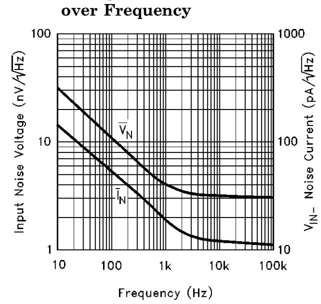
1501-18

Receive Amplifier Frequency Response at $V_S = \pm 5V$



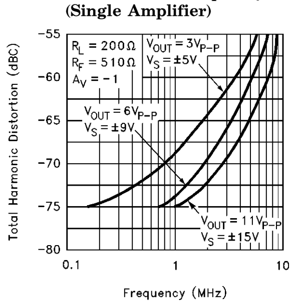
1501-19

Receive Amplifier Input Voltage and Current Noise over Frequency



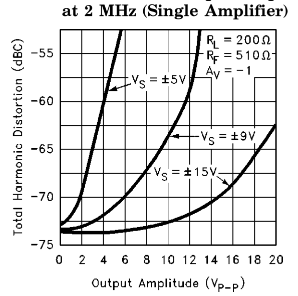
1501-20

Receive Amplifier Harmonic Distortion vs Frequency (Single Amplifier)



1501-21

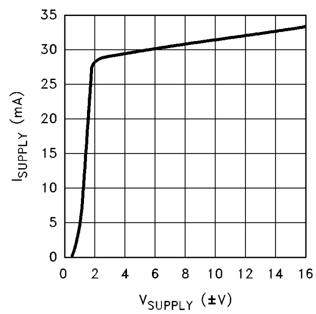
Receive Amplifier Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)



1501-22

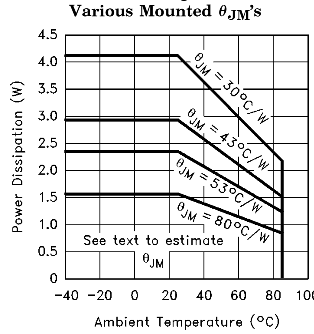
Typical Performance Curves — Contd.

Total Supply Current vs Supply Voltage (All Amplifiers)



1501-23

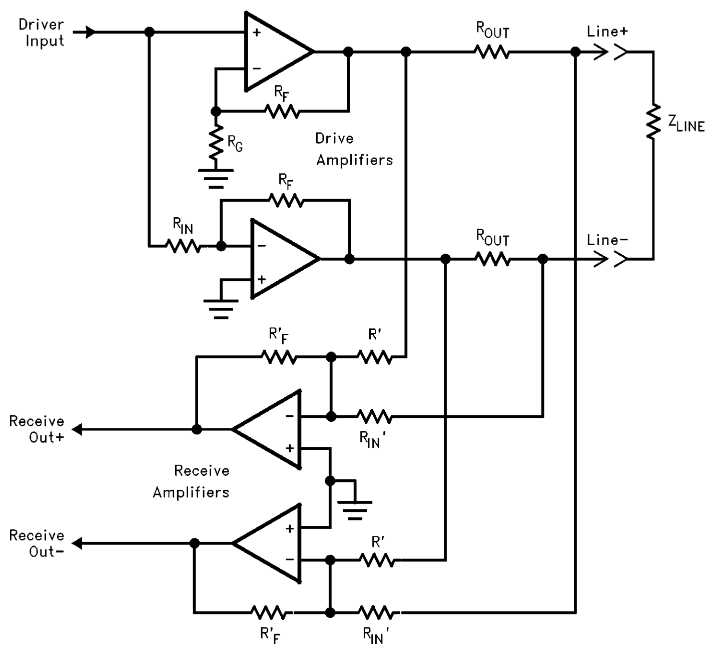
Power Dissipation vs Ambient Temperature for Various Mounted θ_{JM}'s



1501-24

Applications Information

The EL1501C consists of two power line drivers and two receiver amplifiers that can be connected for full duplex differential line transmission and reception. The amplifiers are designed to be used with signals up to 4 MHz and produce low distortion levels. Here is a typical interface circuit:



1501-25

Typical Line Interface Connections

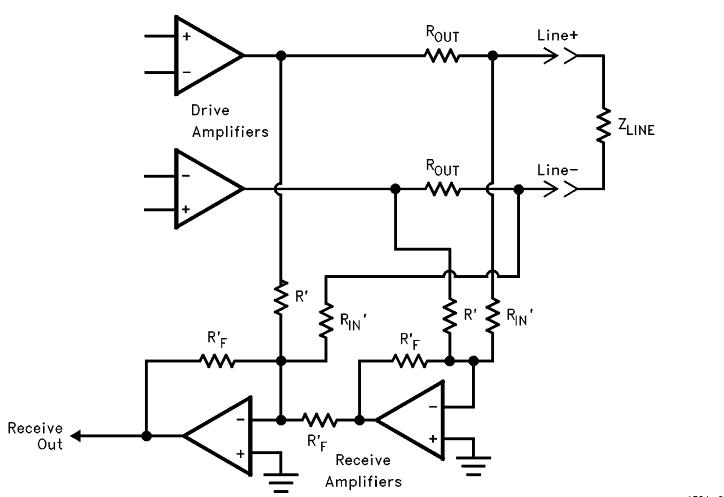
Applications Information — Contd.

The drive amplifiers are wired one in positive gain and the other in negative gain configurations to generate a differential output for a single-ended input. The drivers will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver. The Typical Performance Curves section of this data sheet has a plot of driver responses matched at gains of +1 and −1 using feedback resistors of 910Ω and 750Ω, respectively.

The receiver amplifiers are wired as a hybrid coupler in the circuit. They reject the drivers' output signal (to the matching accuracy of the line impedance and resistors) while passing the signal coming from the line. Their outputs are still differential signals and can be converted to single-ended form by using a wideband instrumentation amplifier such as the EL4430. In a simplistic analysis we set $R_{OUT} = Z_{LINE}/2$ and $R' = 2{*}R_{IN}'$. Signals coming in from the line convert to currents through the R_{IN}'s and pass through the receive amplifiers. Driver outputs pass through the R′ resistors and produce signal currents, but they are cancelled by opposite-polarity currents through the R_{IN}' resistors.

The actual value of R_{OUT} is increased from $Z_{LINE}/2$ to make its value in parallel R_{IN}' equal $Z_{LINE}/2$ and better match the line. For proper hybrid balance, R′ is increased to compensate for R_{OUT}'s adjustment. For $Z_{LINE} = 130\Omega$ and $R_{IN}' = 510\Omega$, we set $R_{OUT} = 74.5\Omega$ and $R' = 1.17\ k\Omega$.

For operating frequencies below 1 MHz, or in cases where the hybrid rejection of the drive signal is not very critical, the receive amplifiers can be wired to provide a single-ended hybrid coupler output:



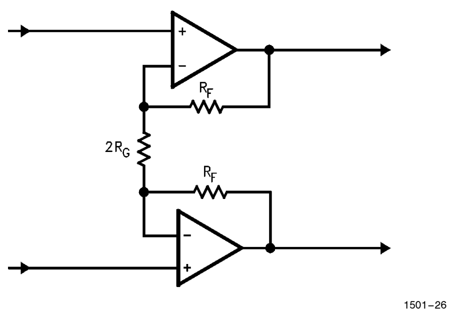
Receive Amplifiers Providing Hybrid and Differential Conversion

Applications Information — Contd.

Common-mode rejection is as good as resistor and line impedance match, as before, but there is a 4 ns time mismatch due to cascading the receive amplifiers. Thus, rejection of common-mode interference will degrade above 1 MHz.

If the receiver amplifiers are not used, their −inputs and outputs may simply be left open. This will reduce power consumption by 2 mA per amplifier.

If a differential signal is available to the drive amplifiers, they may be wired so:



Drivers Wired for Differential Input

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The receiver amplifiers are not sensitive to source impedances, since they are wired for inverting gain. The drivers are somewhat sensitive to source impedance, however. In particular, they do not like being driven by inductive sources. More than 100 nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4″ of unshielded wiring, or 6″ of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Resistive sources greater than 2 kΩ will cause the driver to exhibit increased harmonic distortion. Most amplifier output stages are much lower in impedance and give no problem.

Power Supplies

The EL1501C works well over the ±5V to ±15V supply range. Frequency response varies only slightly, and output drive capability is constant. The major supply voltage issue is power dissipation. The internal dissipation P_D for an EL1501C running on supply voltages of $\pm V_S$ and delivering a DC output voltage V_O into a load of R_L is

$$P_D = 2 \times V_S \times I_S + \Sigma\,(V_S - V_O) \times V_O / R_L,$$

where the Σ indicates that all four amplifiers can produce dissipation by each driving a load. If outputs are sinusoidal signals of V_O volts per amplifier peak-to-peak rather than DC the dissipation is

$$P_D = 2 \times V_S \times I_S + \sum \frac{\sqrt{\dfrac{V_S^2 \times V_O^2}{8} - \dfrac{V_S \times V_O^3}{3\pi} + \dfrac{3 \times V_O^4}{128}}}{R_L}$$

Formula 1

As a worst-case example, assume the drivers are running on ±15.75V supplies, each delivering 19.4 $V_{p\text{-}p}$ outputs into 119Ω (the parallel of resistors the driver in the first schematic would see), and quiescent supply current I_S is the maximum 43 mA, and is substantially constant over temperature. The quiescent dissipation (the first term of the equation) is 1.42W, and each driver adds 0.44W, for a total of 2.24W dissipation. The 19.4 $V_{p\text{-}p}$ output level was chosen to produce the maximum internal dissipation: that is, $V_O = 1.234 \times V_S$ is the most dissipative output level.

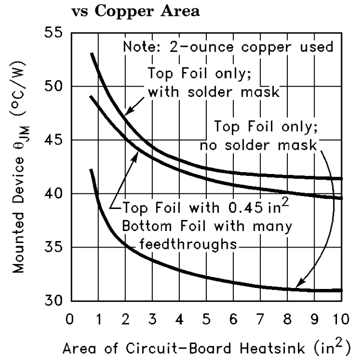
The power supplies should be well bypassed close to the EL1501C. 3.3 μF tantalum capacitors work well. Since the load currents are differential, they need not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no ground loops will occur. This scheme is employed in the layout of the EL1501C demonstration board, and documentation can be obtained from the factory.

Heat-Sinking

To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreading and convecting to air. Thus, the ground plane on the component side of the board becomes the heatsink for the EL1501C. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JM}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask can be cut away from the EL1501C to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

The package will exhibit a θ_{JM} of 80°C/W with no assistance from circuit board heatsinks. This will suffice for the lowest supply voltages and output levels. The best θ_{JM} that can be obtained is about 30°C/W, and a practical layout would produce 43°C/W. More detail is available from the Elantec application note *Measuring the Thermal Resistance of Power Surface-Mount Packages.* This plot summarizes the note's results:

Thermal Resistance of EL1501C vs Copper Area



1501-28

For a given θ_{JM}, the maximum P_D is

$$P_D = (T_{MAX} - T_A)\theta_{JM},$$

where T_{MAX} = 150°C, the maximum die temperature in a plastic package, and T_A is the ambient air temperature.

Output Loading

While the drive amplifiers can output in excess of 250 mA, the internal metallization is not designed to carry more than 75 mA of steady DC current and there is no current-limit mechanism. This allows safely driving peak sinusoidal currents of $\pi \times 75$ mA, or 236 mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25 pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The receive amplifiers are connected in inverting mode and will produce a narrow range of characteristics, but the drives can be used for a wide range of gains. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1 dB peaking) for different supply voltages and gains:

Optimum Driver Feedback Resistor for Various Gains and Supply Voltages

Supply Voltage	Driver Voltage Gain				
	−1	+1	2.5	5	10
±5V	750Ω	910Ω	750Ω	680Ω	620Ω
±9V	680Ω	820Ω	680Ω	620Ω	510Ω
±15V	620Ω	750Ω	620Ω	510Ω	470Ω

Driving Video Loads

Each driver amplifier can drive four doubly-terminated video loads while operating on ±5V supplies. Larger supply voltages slightly improve differential gain and phase distortions, which are around 0.2% and 0.1° for single-ended outputs with the standard NTSC test. Differential-output distortion drops to 0.09% and 0.08°.

EL1501 Macromodel

```
********************************************************************
Applications Hint. Pins 4, 5, 6, 7, 14, 15, 16 & 17 must be connected to
ground (node 0) for proper operation. Use resistors whose value is le-6 ohms.
********************************************************************
* Connections:
* VIN−, DR+
*  |          VOUT, DR+
*  |          |     V−
*  |          |     |     GND
*  |          |     |     |       GND
*  |          |     |     |       |       GND
*  |          |     |     |       |       |      GND
*  |          |     |     |       |       |      |      VIN+, DR+
*  |          |     |     |       |       |      |      |      VOUT, Rcvr+
*  |          |     |     |       |       |      |      |      |       VIN−, Rcvr+
*  |          |     |     |       |       |      |      |      |       |
*  1          2     3     4       5       6      7      8      9       10
*
*VIN−, Rcvr−
*  |          VOUT, Rcvr−
*  |          |     VIN+, DR−
*  |          |     |     GND
*  |          |     |     |       GND
*  |          |     |     |       |       GND
*  |          |     |     |       |       |      GND
*  |          |     |     |       |       |      |      V+
*  |          |     |     |       |       |      |      |      VOUT, DR−
*  |          |     |     |       |       |      |      |      |       VIN−, DR−
*  |          |     |     |       |       |      |      |      |       |
*  11         12    13    14      15      16     17     18     19      20
.subckt EL1501/EL 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
*
***************************
*Driver+ (Amplifier A)
*
e1a 30 0 8 0 1.0
visa 30 43 0V
h2a 43 44 v1a 1.0
r1a 1 45 25
l1a 45 44 2.5nH
i1a 8 0 1µA
i2a 1 0 5µA
h1a 46 0 visa 600
r2a 46 31 1K
d1a 31 0 dclamp
d2a 0 31 dclamp
e2a 32 0 31 0 0.0016666
```

EL1501 Macromodel — Contd.

```
l3a 32 33 0.5µH
c1a 33 0 1pF
r5a 33 0 200
g1a 0 34 33 0 1.0
rola 34 0 2Meg
c2a 34 0 3pF
q1a 3 34 35 qp
q2a 18 34 36 qn
q3a 18 35 37 qn
q4a 3 36 38 qp
r7a 37 2 2
r8a 38 2 2
i3a 18 35 3.3mA
i4a 36 3 3.3mA
ivosa 0 42 2mA
v1a 42 0 0V
*************************************
*Driver— (Amplifier B)
*
e1b 50 0 13 0 1.0
visb 50 63 0V
h2b 63 64 v1b 1.0
r1b 20 65 25
l1b 65 64 2.5nH
i1b 13 0 1µA
i2b 20 0 5µa
h1b 66 0 visb 600
r2b 66 51 1K
d1b 51 0 dclamp
d2b 0 51 dclamp
e2b 52 0 51 0 0.0016666
l3b 52 53 0.5µH
c1b 53 0 1pF
r5b 53 0 200
g1b 0 54 53 0 1.0
rolb 54 0 2Meg
c2b 54 0 3pF
g1b 3 54 55 qp
q2b 18 54 56 qn
q3b 18 55 57 qn
q4b 3 56 58 qp
r7b 57 19 2
r8b 58 19 2
i3b 18 55 3.3mA
i4b 56 3 3.3mA
ivosb 0 62 2mA
v1b 62 0 0V
```

TD is 6.5in

EL1501 Macromodel — Contd.

```
************************************
*Receiver+ (Amplifier C)
*
rpin1 4 5 1e-6
rpin2 5 6 1e-6
rpin3 6 7 1e-6
rpin4 7 14 1e-6
elc 70 0 7 0 1.0
visc 70 83 0V
h2c 83 84 v1b 1.0
rlc 10 85 25
l1c 85 84 2.5nH
i1c 7 0 1µA
i2c 10 0 5µA
h1c 86 0 visc 600
r2c 86 71 1K
d1c 71 0 dclamp
d2c 0 71 dclamp
e2c 72 0 71 0 0.0016666
l3c 72 73 0.5µH
c1c 73 0 1pF
r5c 73 0 200
g1c 0 74 73 0 1.0
rolc 74 0 2Meg
c2c 74 0 4.1pF
q1c 3 74 75 qp
q2c 18 74 76 qn
q3c 18 75 77 qn
q4c 3 76 78 qp
r7c 77 9 2
r8c 78 9 2
i3c 18 75 3.3mA
14c 76 3 3.3mA
ivosc 0 82 2mA
v1c 82 0 0V
************************************
*Receiver- (Amplifier D)
*
rpin5 17 16 le-6
rpin6 16 15 le-6
rpin7 15 14 le-6
eld 90 0 14 0 1.0
visd 90 103 0v
h2d 103 104 vld 1.0
rld 11 105 25
l1d 105 104 2.5nH
i1d 7 0 1µA
i2d 11 0 5µA
hld 106 0 visd 600
r2d 106 91 1K
```

TD is 6.9in

EL1501 Macromodel — Contd.

```
d1d 91 0 dclamp
d2d 0 91 dclamp
e2d 92 0 91 0 0.0016666
l3d 92 93 0.5µH
cld 93 0 1pF
r5d 93 0 200
gld 0 94 93 0 1.0
rold 94 0 2Meg
c2d 94 0 4.1pF
q1d 3 94 95 qp
q2d 18 94 96 qn
q3d 18 95 97 qn
q4d 3 96 98 qp
r7d 97 12 2
r8d 98 12 2
i3d 18 95 3.3mA
i4d 96 3 3.3mA
ivosd 0 102 2mA
vld 102 0 0V
*
* Model
*
.model qn npn(is=5e-15 bf=350 tf=0.1nS)
.model qp pnp(is=5e-15 bf=350 tf=0.1nS)
.model dclamp d(is=le-30 ibv=0.266 bv=1.9 n=4)
.ends
```

TD is 3.6in

*EL1501C—SLIDE**

Differential Line Driver/Receiver

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