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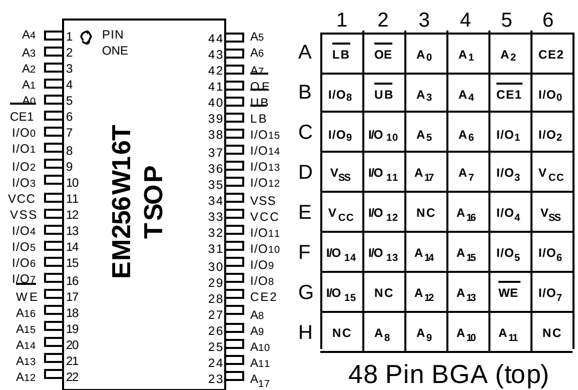
EM256W16 Family

256Kx16 bit Ultra-Low Power Asynchronous Static RAM

Overview

The EM256W16 is an integrated memory device containing a low power 4 Mbit Static Random Access Memory organized as 262,144 words by 16 bits. The device is fabricated using NanoAmp's advanced CMOS process and high-speed/ultra low-power/low-voltage circuit technology. The device pinout is compatible with other standard 256K x 16 SRAMs. The device is designed such that a creative user can improve system power parameters through use of it's unique page mode operation.

FIGURE 1: Pin Configuration



48 Pin BGA (top)
6 x 8 mm

Features

- **Wide Voltage Range:**
  1.65 to 2.25 Volts
- **Extended Temperature Range:**
  -40 to +85 ^oC
- **Fast Cycle Time:**
  T_{ACC} < 70 ns @ 1.8V
  T_{ACC} < 85 ns @ 1.65V

Very Low Operating Current:
  I_{CC} < 1.0 mA typical at 1.8V, 1 Mhz
- **Very Low Standby Current:**
  I_{SB} = 2 µ**A** @ 55 ^oC
- **44-Pin TSOP, 48-Pin BGA or Known Good Die available**

TABLE 1: Pin Descriptions

Pin Name	Pin Function
A_0-A_{17}	Address Inputs
WE	Write Enable Input
CE1, CE2	Chip Enable Inputs
OE	Output Enable Input
UB	Upper Byte Enable Input
LB	Lower Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground

FIGURE 1: Typical Operating Envelope (R/W Mix)

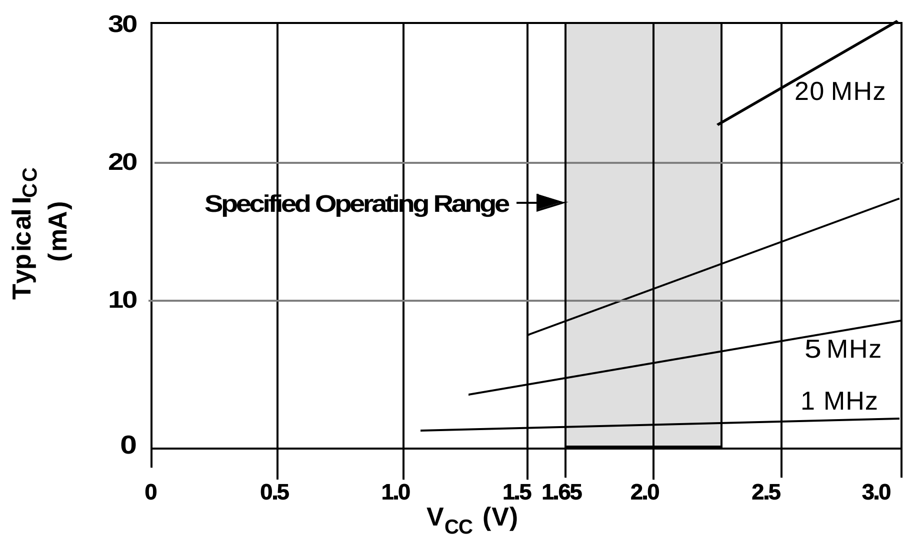


FIGURE 3: Functional Block Diagram

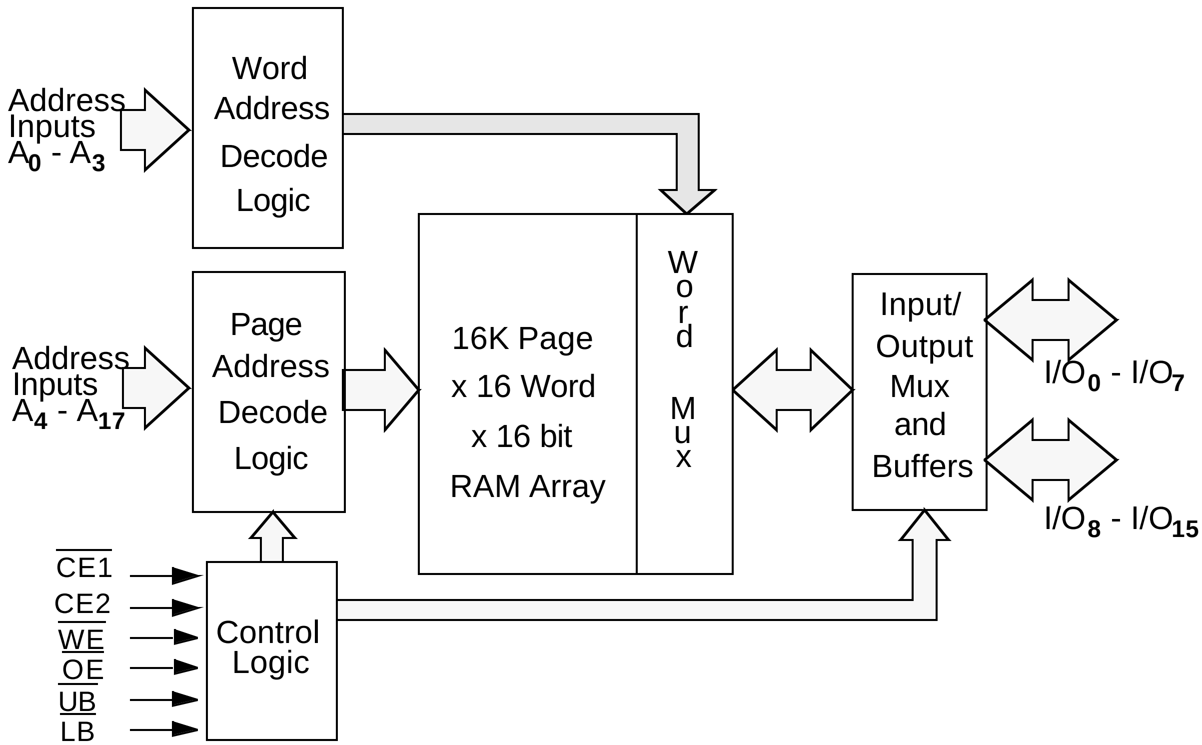


TABLE 2: Functional Description

$\overline{\text{CE1}}$	CE2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	I/O_0 - I/O_{15} [1]	MODE	POWER
H	X	X	X	X	X	High Z	Standby[2]	Standby
X	L	X	X	X	X	High Z	Standby[2]	Standby
X	X	X	X	H	H	High Z	Standby[2]	Standby
L	H	L	X[3]	L[1]	L[1]	Data In	Write[3]	Active -> Standby[4]
L	H	H	L	L[1]	L[1]	Data Out	Read	Active -> Standby[4]
L	H	H	H	L[1]	L[1]	High Z	Active	Standby[4]

1. When $\overline{\text{UB}}$ and $\overline{\text{LB}}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When LB# only is in the select mode only I/O_0 - IO_7 are affected as shown. When $\overline{\text{UB}}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown. If both $\overline{\text{UB}}$ and $\overline{\text{LB}}$ are in the deselect mode (high), the chip is in a standby mode.
2. When the device is in standby mode, control inputs ($\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{UB}}$, and $\overline{\text{LB}}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{\text{WE}}$ is invoked, the $\overline{\text{OE}}$ input is internally disabled and has no effect on the circuit.
4. The device will consume active power in this mode whenever addresses are changed. Data inputs are internally isolated from any external influence.

TABLE 3: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

Note: These parameters are verified in device characterization and are not 100% tested

TABLE 4: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 3.0	V
Power Dissipation (TSOP)	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	^oC
Operating Temperature	T_A	–-40 to +85	^oC
Soldering Temperature and Time	T_{SOLDER}	260 ^oC, 10sec(Lead only)	^oC

* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: Operating Characteristics (Over specified Temperature Range)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		1.65		2.25	V
Data Retention Voltage	V_{DR}	Chip Disabled (Note 3)	1.0			V
Input High Voltage	V_{IH}		0.7V_{CC}		V_{CC}+0.5	V
Input Low Voltage	V_{IL}		–0.5		0.3V_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	V_{CC}–0.3			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.3	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	OE# = V_{IH} or Chip Disabled			0.5	µA
Read/Write Operating Supply Current - Page Access Mode (Note 1)	I_{CC1}	V_{IN} = V_{IH} or V_{IL} Chip Enabled, IOL = 0		10	20	mA
Read/Write Operating Supply Current - Word Access Mode (Note 1)	I_{CC2}	V_{IN} = V_{IH} or V_{IL} Chip Enabled, IOL = 0		5	8	mA
Read/Write Quiescent Operating Supply Current (Note 2)	I_{CC3}	V_{IN} = V_{CC} or 0V Chip Enabled, IOL = 0 f = 0, t_A= 85^{o}C			20	µA
Typical Operation Standby Current (Note 2)	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled, t_A= 55^{o}C			2	µA
Maximum Standby Current (Note 2)	I_{SB2}	V_{IN} = V_{CC} or 0V Chip Disabled, t_A= 85^{o}C			10	µA
Maximum Data Retention Current (Note 2)	I_{DR}	Vcc = 1.0V, V_{IN} = V_{CC} or 0 Chip Disabled, t_A= 85^{o}C			5	µA

1. Operating current is a linear function of operating frequency and voltage. You may calculate operating current using the formula shown with operating frequency (f) expressed in MHz and operating voltage (V) in volts. Example: When operating at 2 MHz at 2.0 volts the device will draw a typical active current of 0.8*2*2 = 3.2 mA in the page access mode. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
2. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) regardless of the state of CE1 or CE2. In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.
3. The Chip is Disabled when $\overline{CE1}$ is high or CE2 is low. The Chip is Enabled when $\overline{CE1}$ is low and CE2 is high.

TABLE 6: Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9\ V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5\ V_{CC}$
Operating Temperature	-40 to +85 ^{o}C
Output Loading	30 pF

TABLE 7: Read Cycle Timing

Item	Symbol	1.65 - 2.25 V		1.8 - 2.25 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		70		ns
Address Access Time	t_{AA}		85		70	ns
Chip Enable to Valid Output	t_{CO}		85		70	ns
Output Enable to Valid Output	t_{OE}		30		25	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		85		70	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		10		ns
Chip Enable to High-Z Output	t_{HZ}	10	30	10	25	ns
Output Disable to High-Z Output	t_{OHZ}	10	30	10	25	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	10	30	10	25	ns
Output Hold from Address Change	t_{OH}	5		5		ns

FIGURE 4: Timing of Read Cycle (1) ($\overline{CE1} = \overline{OE} = V_{IL}$, CE2, $\overline{WE} = V_{IH}$)

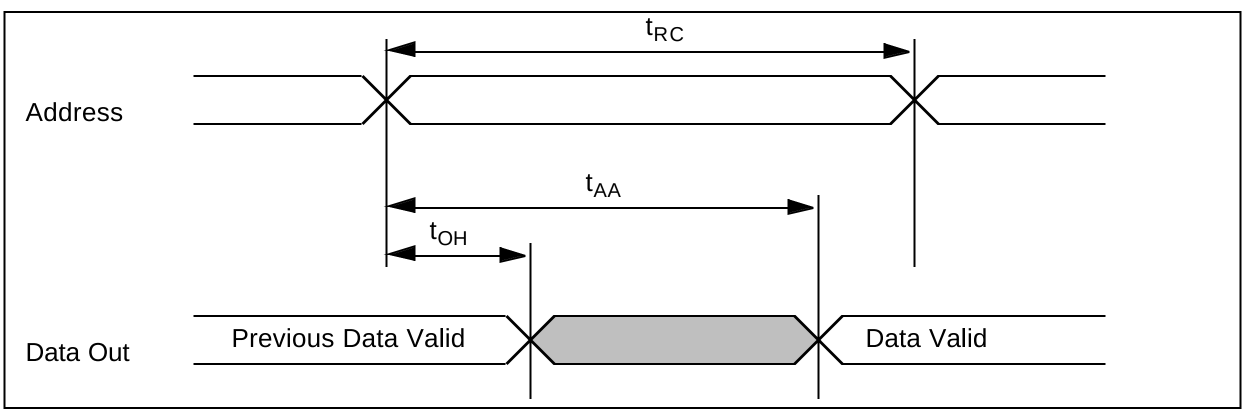


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FIGURE 5: Timing Waveform of Read Cycle (2) ($\overline{WE}$ = V_{IH})

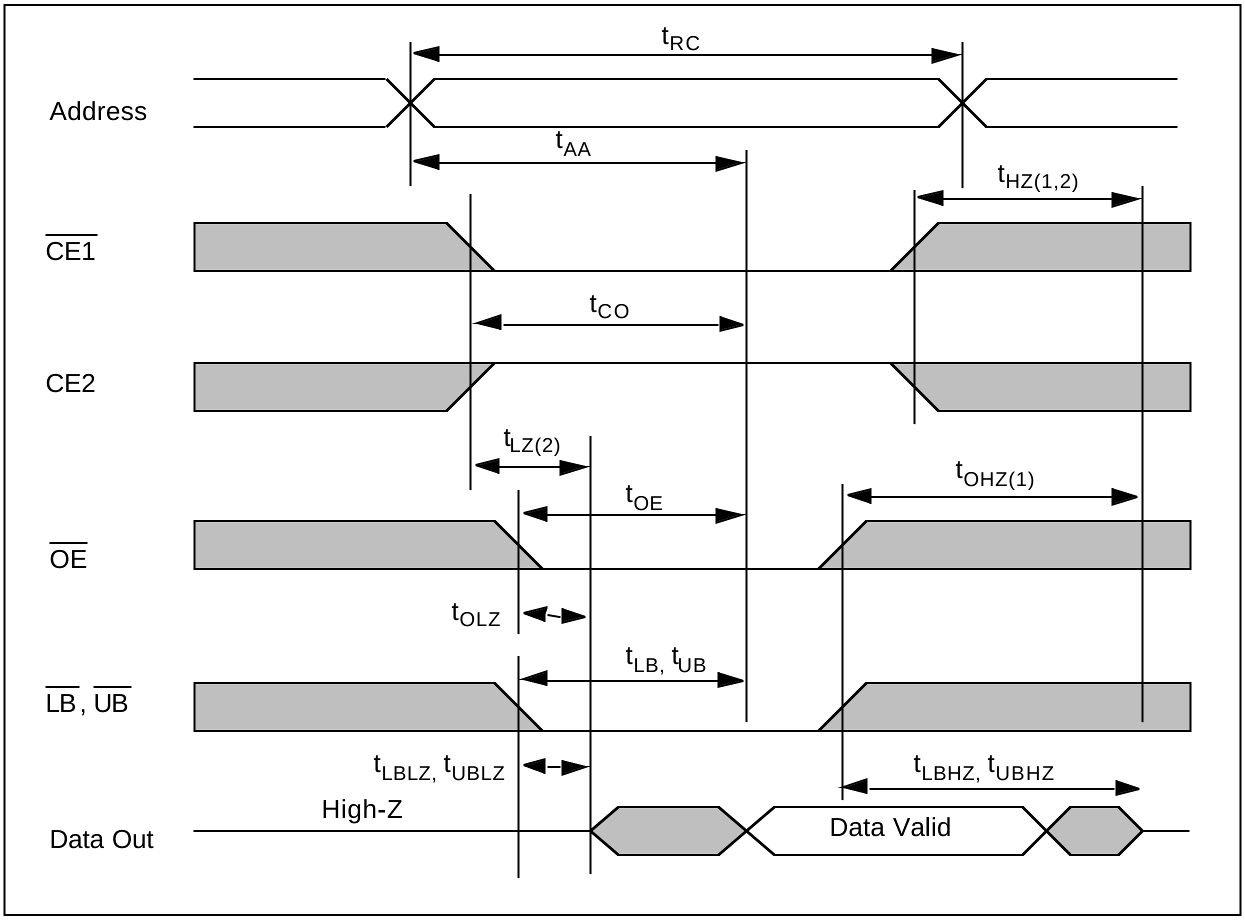


TABLE 8: Write Cycle Timing

Item	Symbol	1.65 - 2.25 V		1.8 - 2.25 V		Units
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		70		ns
Chip Enable to End of Write	t_{CW}	50		40		ns
Address Valid to End of Write	t_{AW}	50		40		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	50		40		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	50		40		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		25		20	ns
Data to Write Time Overlap	t_{DW}	30		25		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	10		10		ns

FIGURE 6: Timing Waveform of Write Cycle (1) ($\overline{WE}$ control)

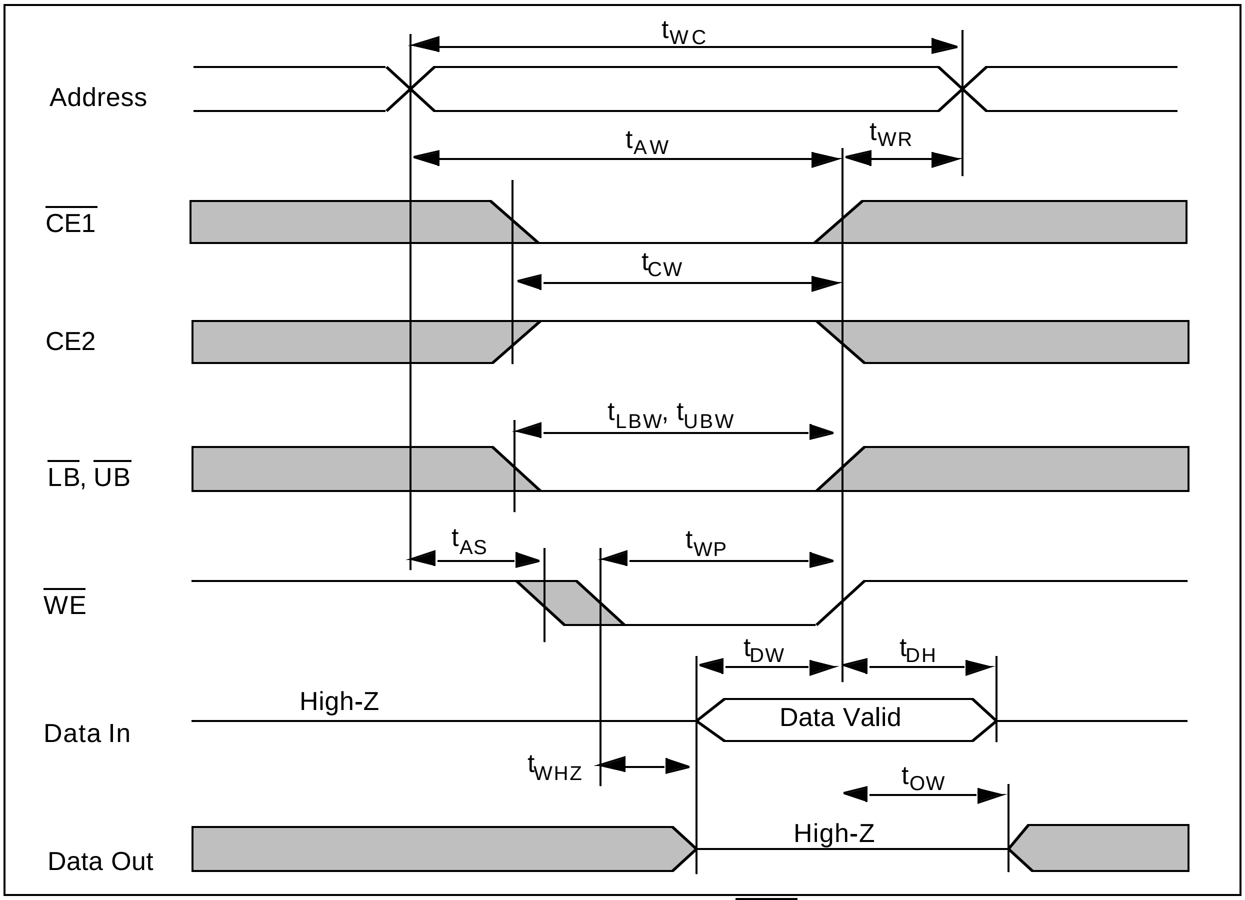


FIGURE 7: Timing Waveform of Write Cycle (2) ($\overline{CE1}$ Control)

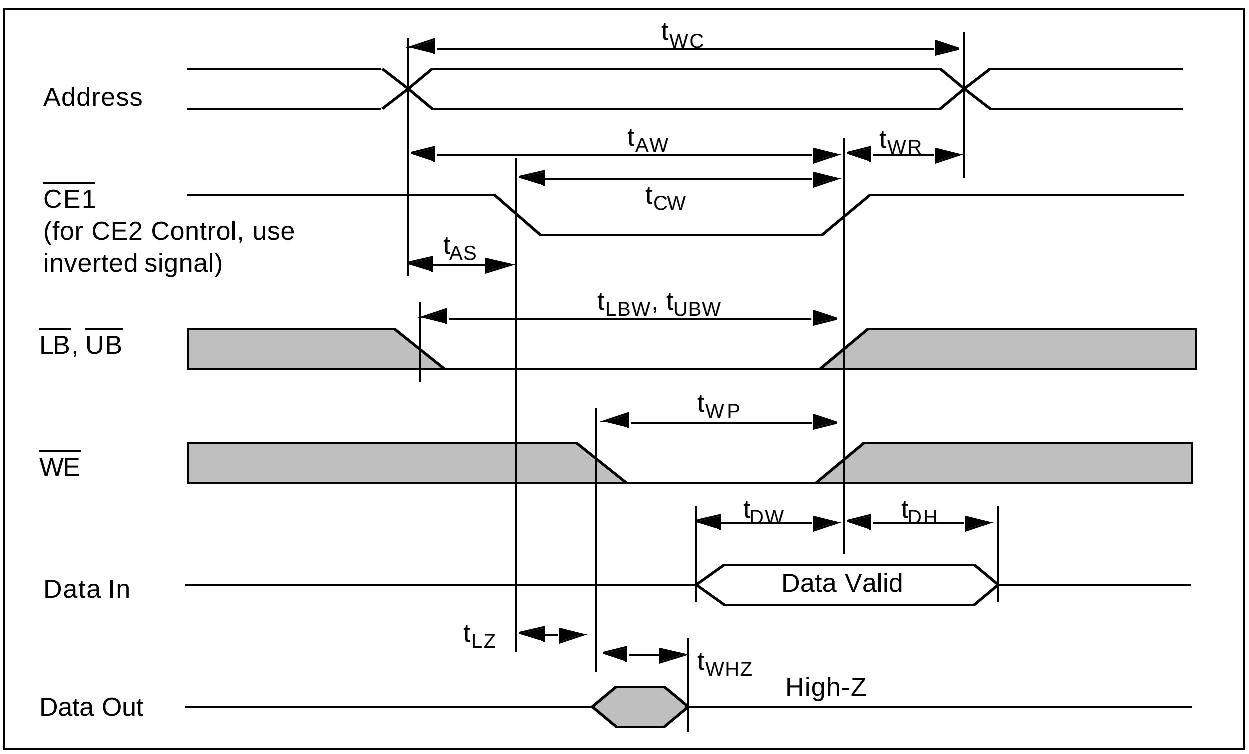
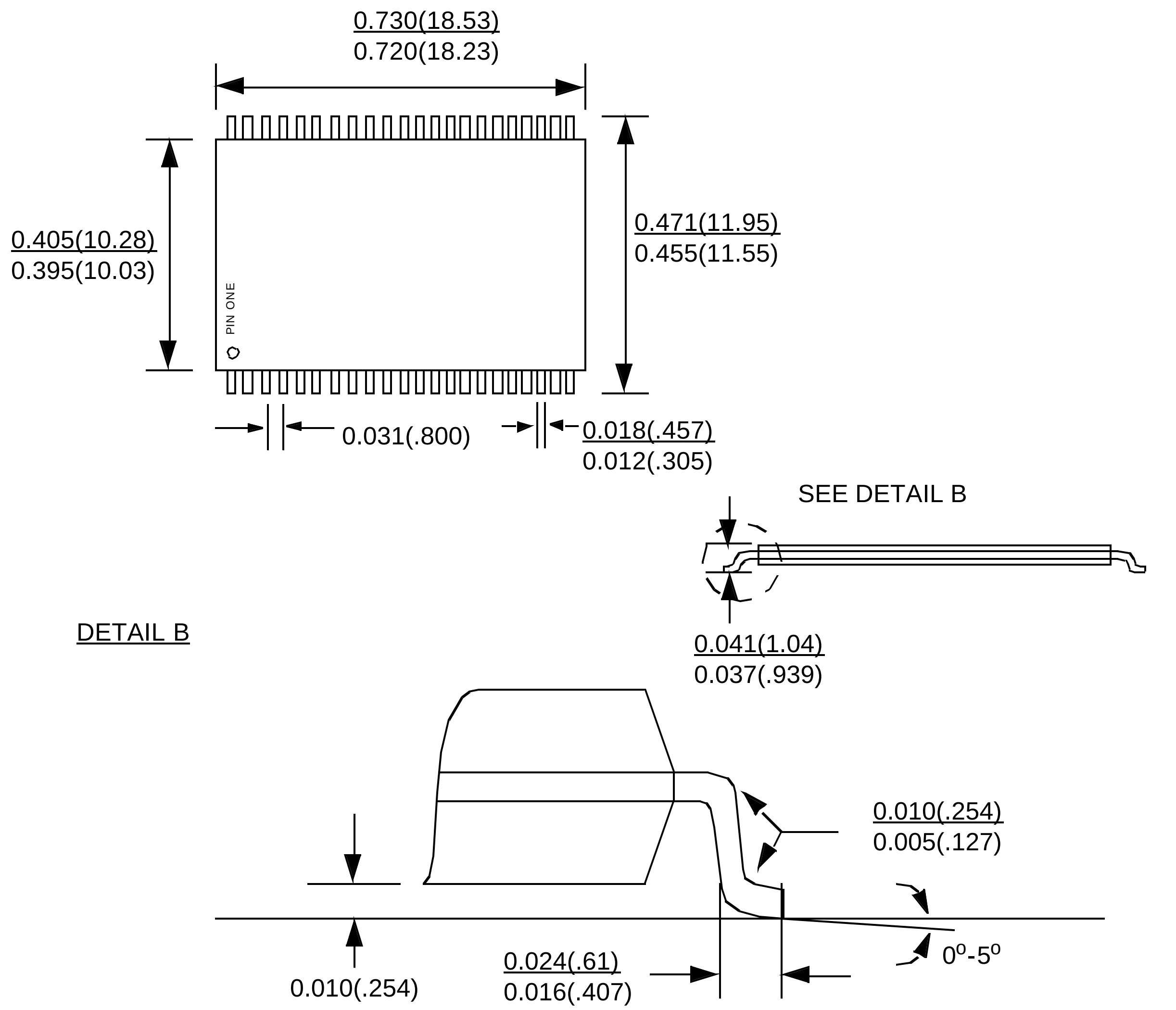
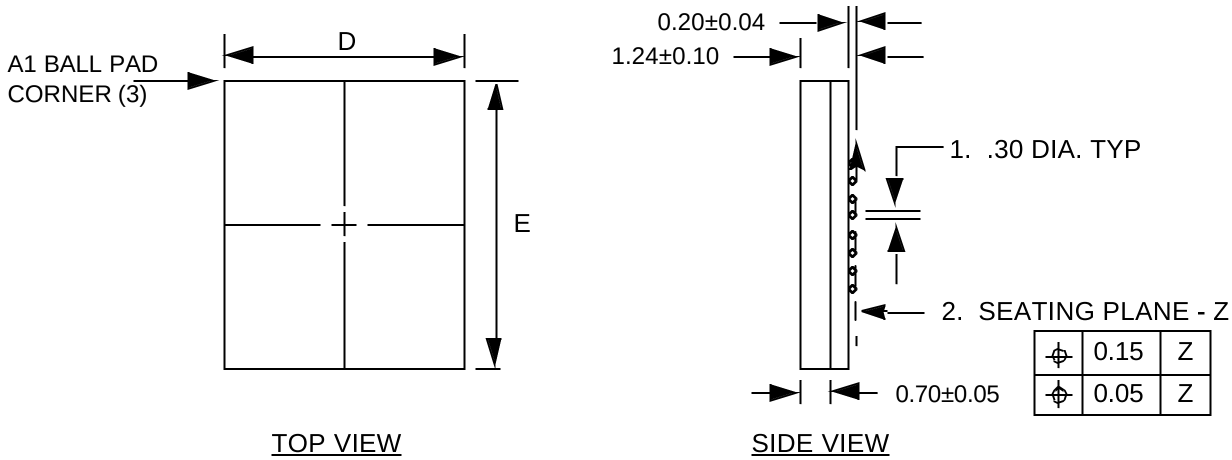


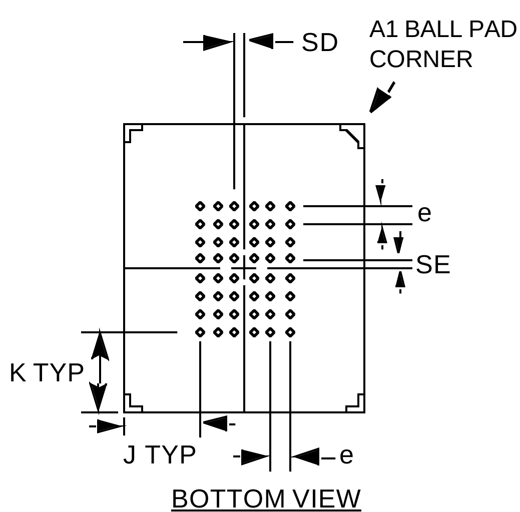
FIGURE 8: 44-LEAD TSOP PACKAGE (T44)



Note:
1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

FIGURE 9: BALL GRID ARRAY PACKAGING





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

TABLE 9: Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6	8	0.375	0.375	1.125	1.375	FULL

TABLE 10: Revision History

Revision #	Date	Change Description
01	Sept. 19, 2000	Production Release
02	Mar 2001	Changed BGA package dimensions to 6x8 mm, other minor edits
03	May 2001	Corrected BGA mechanical drawing dimension K