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# *EM256L08 Family*

***256Kx8 Bit Ultra-Low Power Asynchronous Static RAM***

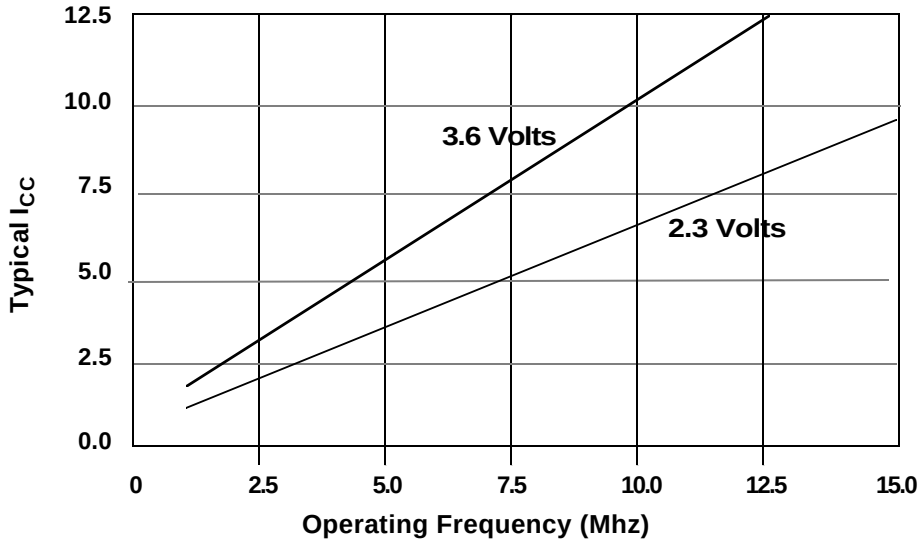
## Overview

The EM256L08 is an integrated memory device containing a low power 2 Mbit Static Random Access Memory organized as 262,144 words by 8 bits. The device is fabricated using NanoAmp's advanced CMOS process and high-speed/low-power circuit technology. This device is designed for very low voltage operation making it quite suitable for battery powered devices. It is also designed for both very low operating and standby-currents. The device pinout is compatible with other standard 256Kx8 SRAMs.

## Features

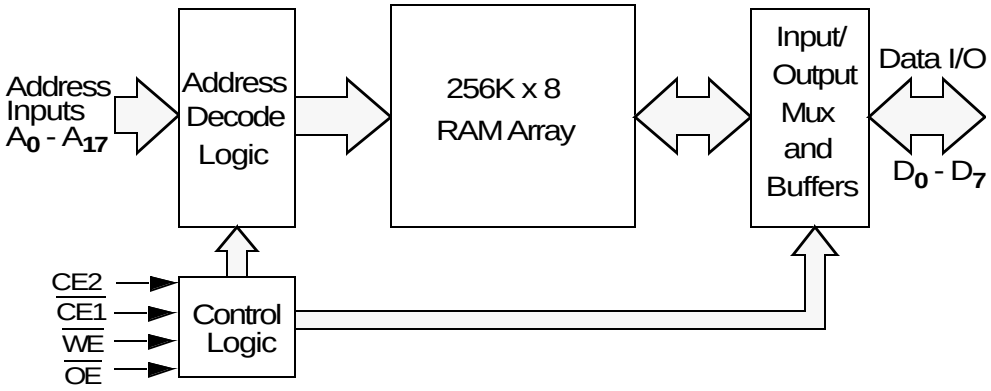
- **Wide Voltage Range:**
  2.3 to 3.6 Volts
- **Extended Temperature Range:**
  -40 to +85 $^{o}$C
- **Fast Cycle Time:**
  $T_{ACC}$ < 55 ns @ 3.0V
- **Very Low Operating Current:**
  $I_{CC}$ < 10 mA typical at 3V, 10 Mhz
- **Very Low Standby Current:**
  $I_{SB}$ < 10 µA @ 55 $^{o}$C
- **32-Pin TSOP, STSOP Packages Available**

**FIGURE 1: Typical Operating Current Curves**



## FIGURE 2: Pin Configuration


## FIGURE 3: Functional Block Diagram




## TABLE 1: Pin Description

| Pin Name | Pin Function | Pin Name | Pin Function |
|---|---|---|---|
| A0-A17 | Address Inputs | $\overline{WE}$ | Write Enable (Active Low) |
| D0-D7 | Data Inputs/Outputs | $V_{CC}$ | Power |
| $\overline{CE1}$, CE2 | Chip Enable (Active Low/High) | $V_{SS}$ | Ground |
| $\overline{OE}$ | Output Enable (Active Low) | NC | Not Connected (Do not connect signal) |

## TABLE 2: Functional Description

| $\overline{CE1}$ | CE2 | $\overline{WE}$ | $\overline{OE}$ | D0-D7 | MODE | POWER |
|---|---|---|---|---|---|---|
| H | X | X | X | High Z | Standby | Standby |
| X | L | X | X | High Z | Standby | Standby |
| L | H | L | X | Data In | Write | Active |
| L | H | H | L | Data Out | Read | Active |
| L | H | H | H | High Z | Active | Active |

*The device will consume active power in this mode whenever addresses are changed

## TABLE 3: Capacitance*

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V, f = 1 Mhz, $T_A$ = 25°C | | 8 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{IN}$ = 0V, f = 1 Mhz, $T_A$ = 25°C | | 8 | pF |

Note: These parameters are verified in device characterization and are not 100% tested

## TABLE 4: Absolute Maximum Ratings*

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN,OUT}$ | –0.3 to $V_{CC}$+0.3 | V |
| Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{CC}$ | –0.3 to 5.0 | V |
| Power Dissipation | $P_D$ | 500 | mW |
| Storage Temperature | $T_{STG}$ | –40 to 125 | °C |
| Operating Temperature | $T_A$ | -40 to +85 | °C |
| Soldering Temperature and Time | $T_{SOLDER}$ | 260 °C, 10sec(Lead only) | °C |

* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## TABLE 5: Operating Characteristics (Over specified Temperature Range)

| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 2.3 | | 3.6 | V |
| Data Retention Voltage | $V_{DR}$ | Chip Disabled (Note 3) | 1.8 | | | V |
| Input High Voltage | $V_{IH}$ | | $0.7V_{CC}$ | | $V_{CC}$+0.5 | V |
| Input Low Voltage | $V_{IL}$ | | –0.5 | | $0.3V_{CC}$ | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = 0.2mA | $V_{CC}$–0.2 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = -0.2mA | | | 0.2 | V |
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = 0 to $V_{CC}$ | | | 0.5 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{OE}$ = $V_{IH}$ or Chip Disabled | | | 0.5 | µA |
| Read/Write Operating Supply Current @ 1 µS Cycle Time | $I_{CC1}$ | VCC=3.6 V, $V_{IN}$=$V_{IH}$ or $V_{IL}$ Chip Enabled, IOL = 0 | | | 3.0 | mA |
| Read/Write Operating Supply Current @ 70 nS Cycle Time | $I_{CC2}$ | VCC=3.6 V, $V_{IN}$=$V_{IH}$ or $V_{IL}$ Chip Enabled, IOL = 0 | | | 14.0 | mA |
| Read/Write Quiescent Operating Supply Current (Note 1) | $I_{CC3}$ | $V_{IN}$ = $V_{CC}$ or 0V Chip Enabled, IOL = 0 f = 0, $t_A$= 85°C, VCC = 3.6V | | | 2 | mA |
| Operating Standby Current (Note 1) | $I_{SB1}$ | $V_{IN}$ = $V_{CC}$ or 0V Chip Disabled $t_A$= 55°C, VCC = 3.6V | | | 10 | µA |
| Maximum Standby Current (Note 1) | $I_{SB2}$ | $V_{IN}$ = $V_{CC}$ or 0V Chip Disabled $t_A$= 85°C, VCC = 3.6V | | | 20 | µA |
| Maximum Data Retention Current (Note 1) | $I_{DR}$ | Vcc = 2.0V, $V_{IN}$ = $V_{CC}$ or 0 Chip Disabled, $t_A$= 85°C | | | 10 | µA |

Note 1. This device assumes a standby mode if either $\overline{CE1}$ is disabled (high) or CE2 is disabled (low). In order to achieve low standby current in the enabled mode ($\overline{CE1}$ low and CE2 high), all inputs must be within 0.2 volts of either $V_{CC}$ or $V_{SS}$.

## TABLE 6: Timing Test Conditions

| Item | |
|---|---|
| Input Pulse Level | $0.1V_{CC}$ to $0.9\ V_{CC}$ |
| Input Rise and Fall Time | 5ns |
| Input and Output Timing Reference Levels | $0.5\ V_{CC}$ |
| Output Load | CL = 30pF |
| Operating Temperature | -40 to +85 °C |

## TABLE 7: Timing

| Item | Symbol | 2.3 - 3.6 V | | 3.0 - 3.6 V | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle Time | $t_{RC}$ | 70 | | 55 | | ns |
| Address Access Time | $t_{AA}$ | | 70 | | 55 | ns |
| Chip Enable to Valid Output | $t_{CO}$ | | 70 | | 55 | ns |
| Output Enable to Valid Output | $t_{OE}$ | | 25 | | 20 | ns |
| Chip Enable to Low-Z output | $t_{LZ}$ | 10 | | 10 | | ns |
| Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | | 5 | | ns |
| Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 20 | 0 | 15 | ns |
| Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 20 | 0 | 15 | ns |
| Output Hold from Address Change | $t_{OH}$ | 10 | | 10 | | ns |
| Write Cycle Time | $t_{WC}$ | 70 | | 55 | | ns |
| Chip Enable to End of Write | $t_{CW}$ | 50 | | 45 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 50 | | 45 | | ns |
| Write Pulse Width | $t_{WP}$ | 40 | | 35 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | ns |
| Write to High-Z Output | $t_{WHZ}$ | | 20 | | 15 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 40 | | 35 | | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | | 0 | | ns |
| End Write to Low-Z Output | $t_{OW}$ | 5 | | 5 | | ns |

**FIGURE 4: Read Cycle Timing ($\overline{WE}$ = $V_{IH}$)**

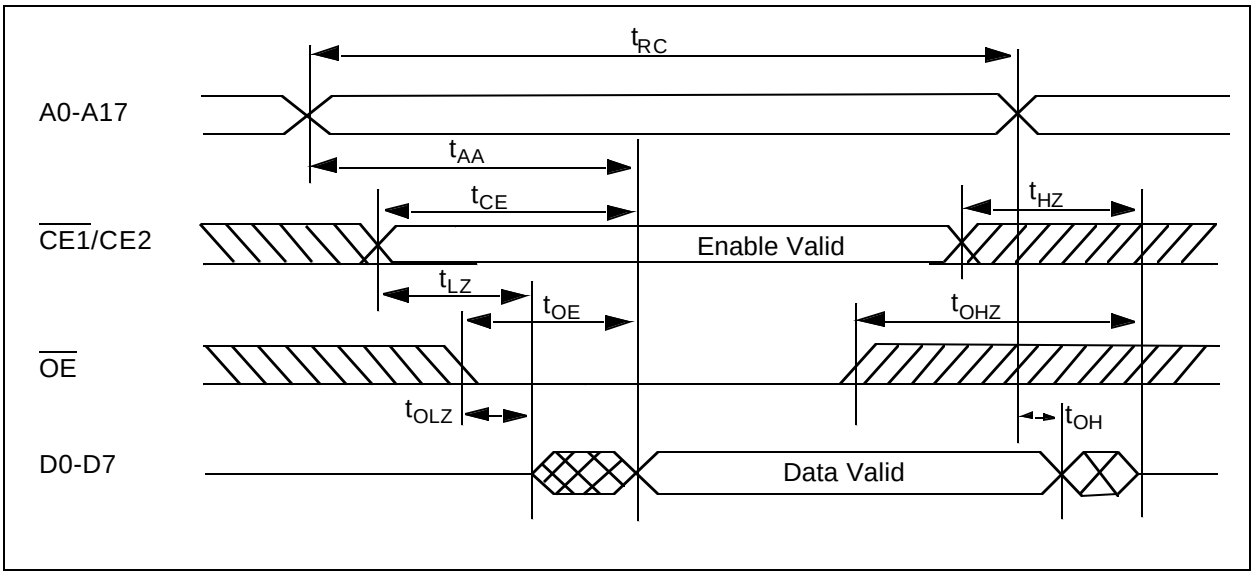
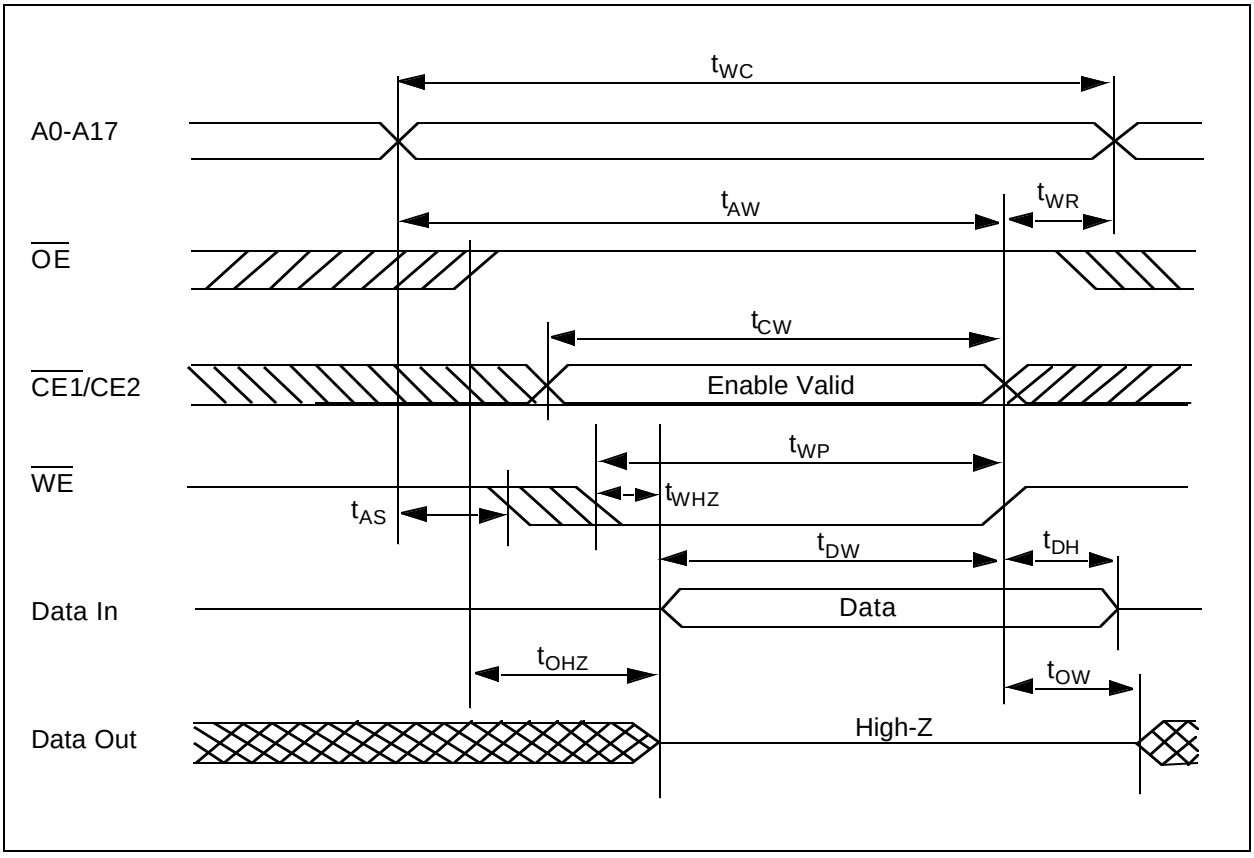
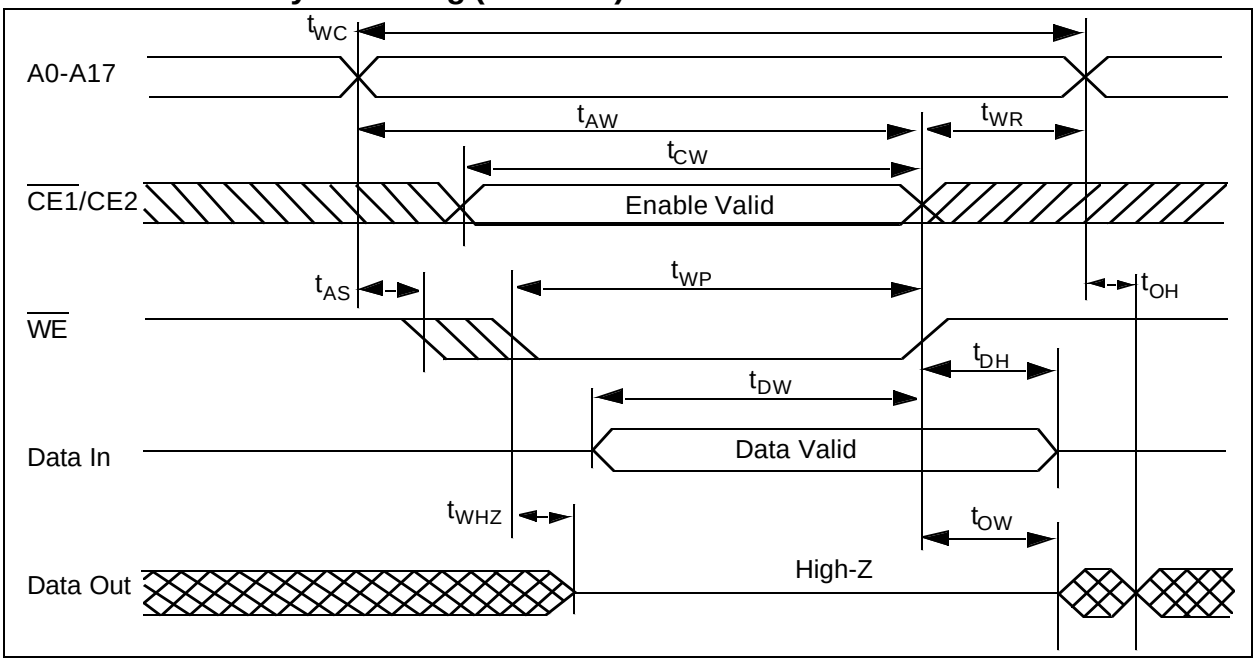



**FIGURE 5: Write Cycle Timing ($\overline{OE}$ clock)**



## FIGURE 6: Write Cycle Timing ($\overline{OE}$ fixed)




## TABLE 8: Ordering Information

| Part Number | Package | Temperature Range | Voltage Range | Speed |
|---|---|---|---|---|
| EM256L08T | 32 pin TSOP | -40 to +85°C | 2.3 to 3.6 V | 55 ns @ 3.0 V |
| EM256L08N | 32 pin STSOP | -40 to +85°C | 2.3 to 3.6 V | 55 ns @ 3.0 V |

## TABLE 9: Revision History

| Revision # | Date | Change Description |
|---|---|---|
| 01 | March 8, 2000 | Initial Preliminary Release |
| 02 | Jan 15, 2001 | Separated single chip enable and dual chip enable into different part numbers |
| 03 | March 2001 | Added Table 3: Capacitance<br>Revised quiescent operating current, modified figures 1-2 and table 1, other minor edits |