**NanoAmp Solutions, Inc.**
1982 Zanker Road, San Jose, CA 95112
ph: 408-573-8878, FAX: 408-573-8877
www.nanoamp.com



# *EM064J16*

## *64Kx16bit Ultra-Low Power Asynchronous Static RAM*

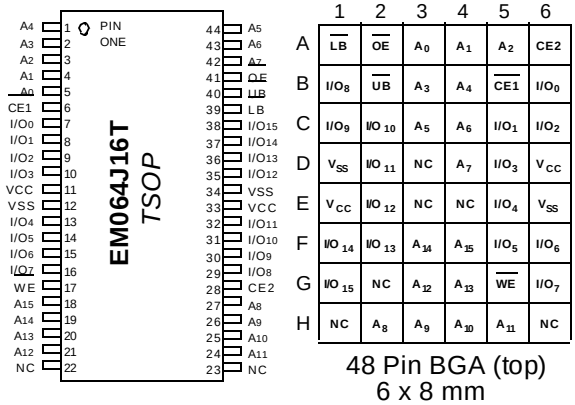
## Overview

The EM064J16 is an integrated memory device containing a low power 1 Mbit Static Random Access Memory organized as 65,536 words by 16 bits. The base design is the same as NanoAmp's EM064U16 which is processed to operate at lower voltages. The device is fabricated using Nano-Amp's advanced CMOS process and high-speed/ ultra low-power/low-voltage circuit technology. The device pinout is compatible with other standard 64K x 16 SRAMs.

## Features

- **Wide Voltage Range:**
  2.3 to 3.6 Volts
- **Extended Temperature Range:**
  -40 to +85 $^{o}$C
- **Fast Cycle Time:**
  $T_{ACC}$ < 70 ns @ 2.7V
- **Very Low Operating Current:**
  $I_{CC}$ < 10 mA typical at 3V, 10 Mhz
- **Very Low Standby Current:**
  $I_{SB}$ < 10 µA @ 55 $^{o}$C
- **44-Pin TSOP, 48-Pin BGA Available**

## FIGURE 1: Pin Configuration



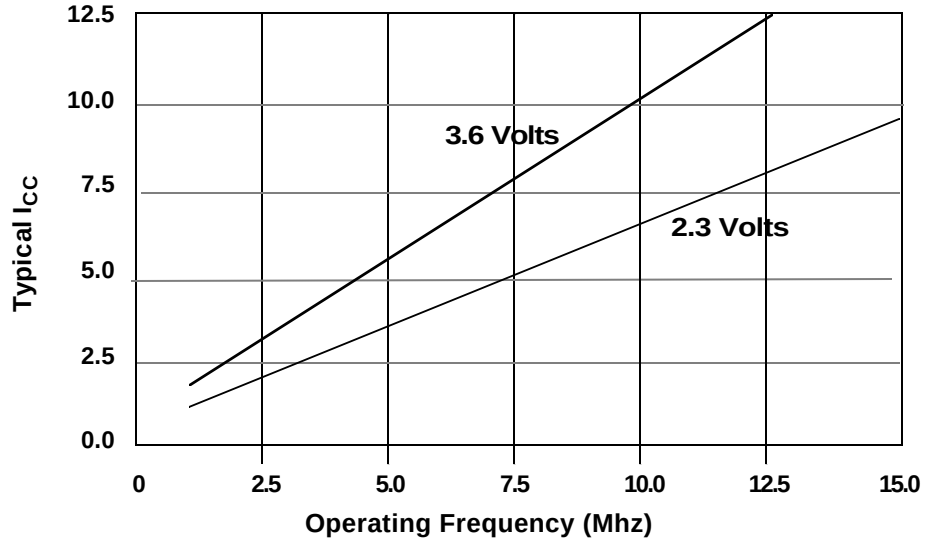

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | $\overline{LB}$ | $\overline{OE}$ | $A_0$ | $A_1$ | $A_2$ | CE2 |
| B | $I/O_8$ | $\overline{UB}$ | $A_3$ | $A_4$ | $\overline{CE1}$ | $I/O_0$ |
| C | $I/O_9$ | $I/O_{10}$ | $A_5$ | $A_6$ | $I/O_1$ | $I/O_2$ |
| D | $V_{SS}$ | $I/O_{11}$ | NC | $A_7$ | $I/O_3$ | $V_{CC}$ |
| E | $V_{CC}$ | $I/O_{12}$ | NC | NC | $I/O_4$ | $V_{SS}$ |
| F | $I/O_{14}$ | $I/O_{13}$ | $A_{14}$ | $A_{15}$ | $I/O_5$ | $I/O_6$ |
| G | $I/O_{15}$ | NC | $A_{12}$ | $A_{13}$ | $\overline{WE}$ | $I/O_7$ |
| H | NC | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | NC |

48 Pin BGA (top)
6 x 8 mm

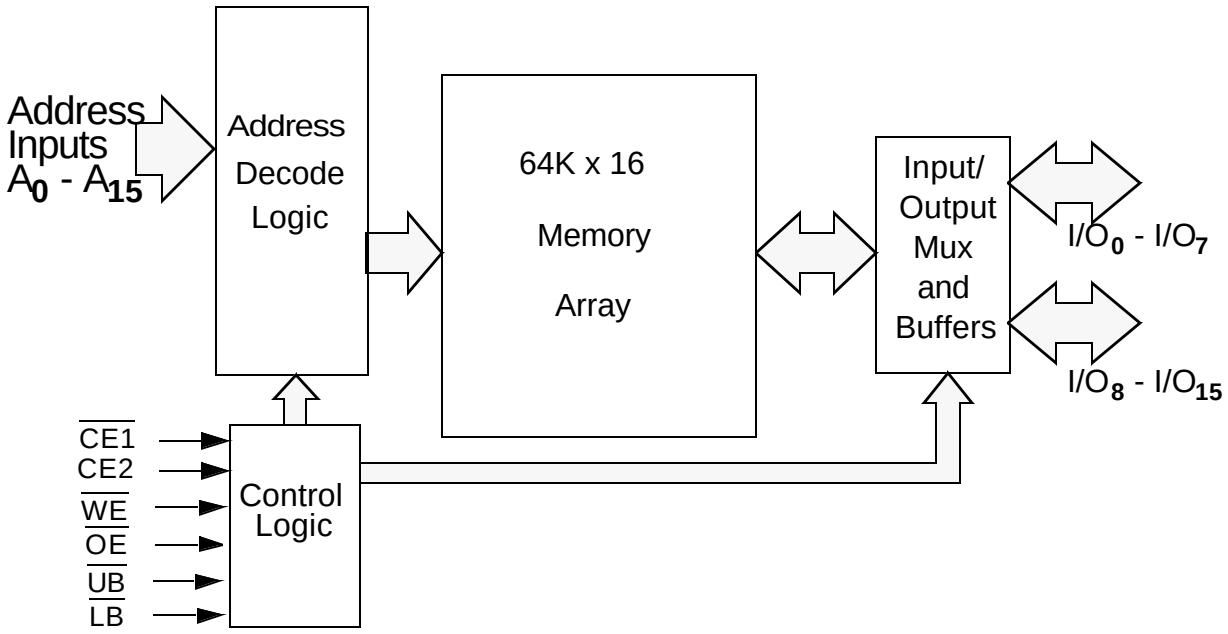
## TABLE 1: Pin Descriptions

| Pin Name | Pin Function |
|---|---|
| $A_0$-$A_{15}$ | Address Inputs |
| $\overline{WE}$ | Write Enable Input |
| $\overline{CE1}$, CE2 | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{UB}$ | Upper Byte Enable Input |
| $\overline{LB}$ | Lower Byte Enable Input |
| $I/O_0$-$I/O_{15}$ | Data Inputs/Outputs |
| $V_{CC}$ | Power |
| $V_{SS}$ | Ground |
| NC | Not Connected |

## FIGURE 1: Typical Operating Current Curves



## FIGURE 3: Functional Block Diagram




## TABLE 2: Functional Description

| $\overline{CE1}$ | CE2 | $\overline{WE}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | $I/O_0$ - $I/O_{15}$[1] | MODE | POWER |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | X | High Z | Standby[2] | Standby |
| X | L | X | X | X | X | High Z | Standby[2] | Standby |
| L | H | X | X | H | H | High Z | Standby | Standby |
| L | H | L | X[3] | L[1] | L[1] | Data In | Write[3] | Active |
| L | H | H | L | L[1] | L[1] | Data Out | Read | Active |
| L | H | H | H | L[1] | L[1] | High Z | Active | Active |

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), $I/O_0$ - $I/O_{15}$ are affected as shown. When $\overline{LB}$ only is in the select mode only $I/O_0$ - $IO_7$ are affected as shown. When $\overline{UB}$ is in the select mode only $I/O_8$ - $I/O_{15}$ are affected as shown. If both $\overline{UB}$ and $\overline{LB}$ are in the deselect mode (high), the chip is active but unaffected by the state of $\overline{WE}$ or $\overline{OE}$.
2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

## TABLE 3: Capacitance*

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V, f = 1 MHz, $T_A$ = 25°C | | 8 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{IN}$ = 0V, f = 1 MHz, $T_A$ = 25°C | | 8 | pF |

Note: These parameters are verified in device characterization and are not 100% tested

## TABLE 4: Absolute Maximum Ratings*

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN,OUT}$ | –0.3 to $V_{CC}$+0.3 | V |
| Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{CC}$ | –0.3 to 4.0 | V |
| Power Dissipation | $P_D$ | 500 | mW |
| Storage Temperature | $T_{STG}$ | –40 to 125 | °C |
| Operating Temperature | $T_A$ | -40 to +85 | °C |
| Soldering Temperature and Time | $T_{SOLDER}$ | 260 °C, 10sec(Lead only) | °C |

* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## TABLE 5: Operating Characteristics (Over specified Temperature Range)

| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 2.3 | | 3.6 | V |
| Data Retention Voltage | $V_{DR}$ | Chip Disabled (Note 3) | 1.8 | | | V |
| Input High Voltage | $V_{IH}$ | | $0.7V_{CC}$ | | $V_{CC}$+0.5 | V |
| Input Low Voltage | $V_{IL}$ | | –0.5 | | $0.3V_{CC}$ | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = 0.2mA | $V_{CC}$–0.2 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = -0.2mA | | | 0.2 | V |
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = 0 to $V_{CC}$ | | | 0.5 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{OE}$ = $V_{IH}$ or Chip Disabled | | | 0.5 | µA |
| Read/Write Operating Supply Current @ 1 µS Cycle Time (Note 1) | $I_{CC1}$ | VCC=3.6 V, $V_{IN}$=$V_{IH}$ or $V_{IL}$ Chip Enabled, IOL = 0 | | | 3.0 | mA |
| Read/Write Operating Supply Current @ 70 nS Cycle Time (Note 1) | $I_{CC2}$ | VCC=3.6 V, $V_{IN}$=$V_{IH}$ or $V_{IL}$ Chip Enabled, IOL = 0 | | | 14.0 | mA |
| Read/Write Quiescent Operating Supply Current (Note 2) | $I_{CC3}$ | $V_{IN}$ = $V_{CC}$ or 0V Chip Enabled, IOL = 0 f = 0, $t_A$= 85°C, VCC = 3.6V | | | 3 | mA |
| Operating Standby Current (Note 2) | $I_{SB1}$ | $V_{IN}$ = $V_{CC}$ or 0V Chip Disabled $t_A$= 55°C, VCC = 3.6V | | | 10 | µA |
| Maximum Standby Current (Note 2) | $I_{SB2}$ | $V_{IN}$ = $V_{CC}$ or 0V Chip Disabled $t_A$= 85°C, VCC = 3.6V | | | 20 | µA |
| Maximum Data Retention Current (Note 2) | $I_{DR}$ | Vcc = 2.0V, $V_{IN}$ = $V_{CC}$ or 0 Chip Disabled, $t_A$= 85°C | | | 10 | µA |

1. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
2. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.
3. The Chip is Disabled when $\overline{CE1}$ is high or CE2 is low. The Chip is Enabled when $\overline{CE1}$ is low and CE2 is high.

## TABLE 6: Timing Test Conditions

| Item | |
|---|---|
| Input Pulse Level | $0.1V_{CC}$ to $0.9\ V_{CC}$ |
| Input Rise and Fall Time | 5ns |
| Input and Output Timing Reference Levels | $0.5\ V_{CC}$ |
| Output Load | CL = 30pF |
| Operating Temperature | -40 to +85 °C |

## TABLE 7: Timing

| Item | Symbol | 2.3 - 3.6 V | | 2.7 - 3.6 V | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle Time | $t_{RC}$ | 85 | | 70 | | ns |
| Address Access Time | $t_{AA}$ | | 85 | | 70 | ns |
| Chip Enable to Valid Output | $t_{CO}$ | | 85 | | 70 | ns |
| Output Enable to Valid Output | $t_{OE}$ | | 30 | | 25 | ns |
| Byte Select to Valid Output | $t_{LB}$, $t_{UB}$ | | 85 | | 70 | ns |
| Chip Enable to Low-Z output | $t_{LZ}$ | 10 | | 10 | | ns |
| Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | | 5 | | ns |
| Byte Select to Low-Z Output | $t_{LBZ}$, $t_{UBZ}$ | 10 | | 10 | | ns |
| Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 20 | 0 | 20 | ns |
| Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 20 | 0 | 20 | ns |
| Byte Select Disable to High-Z Output | $t_{LBHZ}$, $t_{UBHZ}$ | 0 | 20 | 0 | 20 | ns |
| Output Hold from Address Change | $t_{OH}$ | 10 | | 10 | | ns |
| Write Cycle Time | $t_{WC}$ | 85 | | 70 | | ns |
| Chip Enable to End of Write | $t_{CW}$ | 50 | | 50 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 50 | | 50 | | ns |
| Byte Select to End of Write | $t_{LBW}$, $t_{UBW}$ | 50 | | 50 | | ns |
| Write Pulse Width | $t_{WP}$ | 40 | | 40 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | ns |
| Write to High-Z Output | $t_{WHZ}$ | | 20 | | 20 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 40 | | 40 | | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | | 0 | | ns |
| End Write to Low-Z Output | $t_{OW}$ | 5 | | 5 | | ns |

**FIGURE 4: Timing of Read Cycle (1) ($\overline{CE1}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = CE2 = $V_{IH}$)**

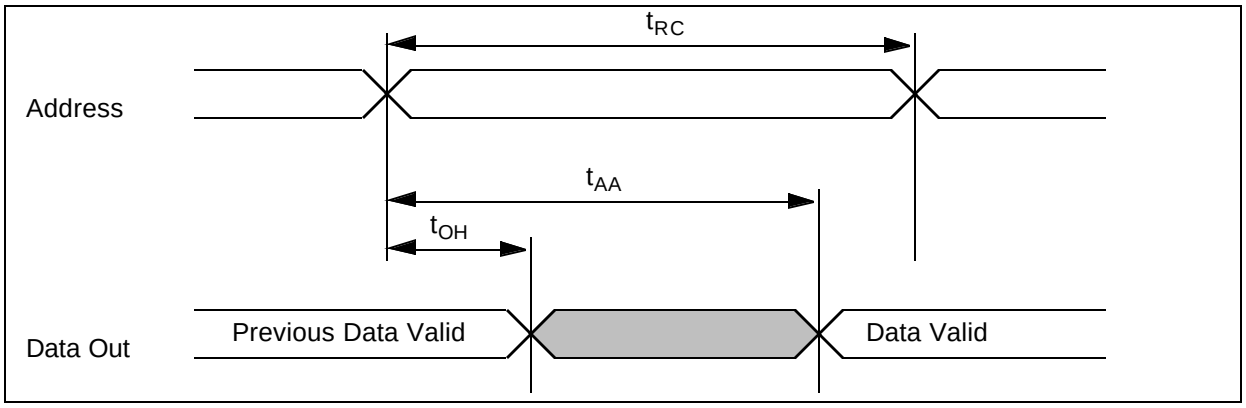



**FIGURE 5: Timing Waveform of Read Cycle (2) ($\overline{WE}$ = $V_{IH}$)**

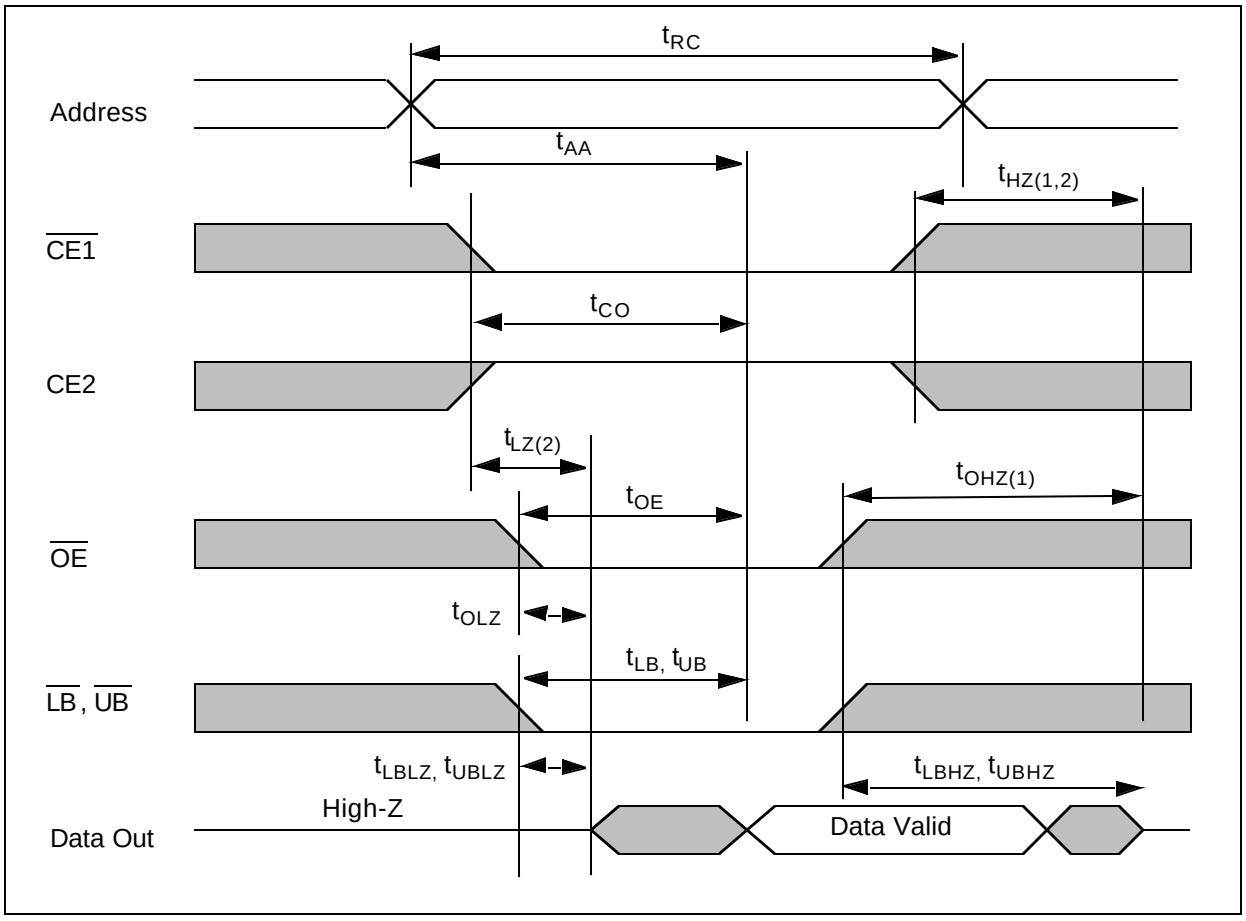


**FIGURE 6: Timing Waveform of Write Cycle (1) ($\overline{WE}$ control)**

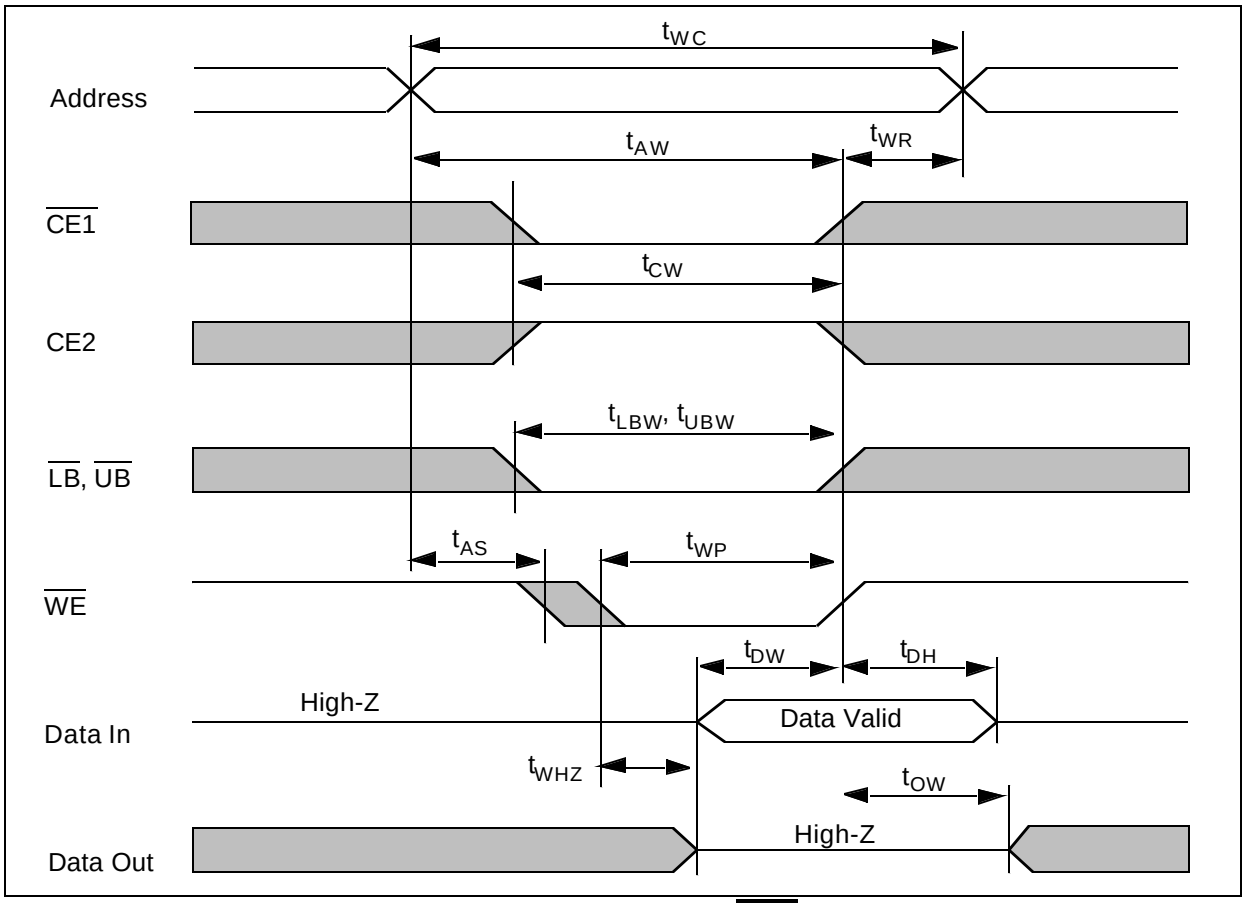
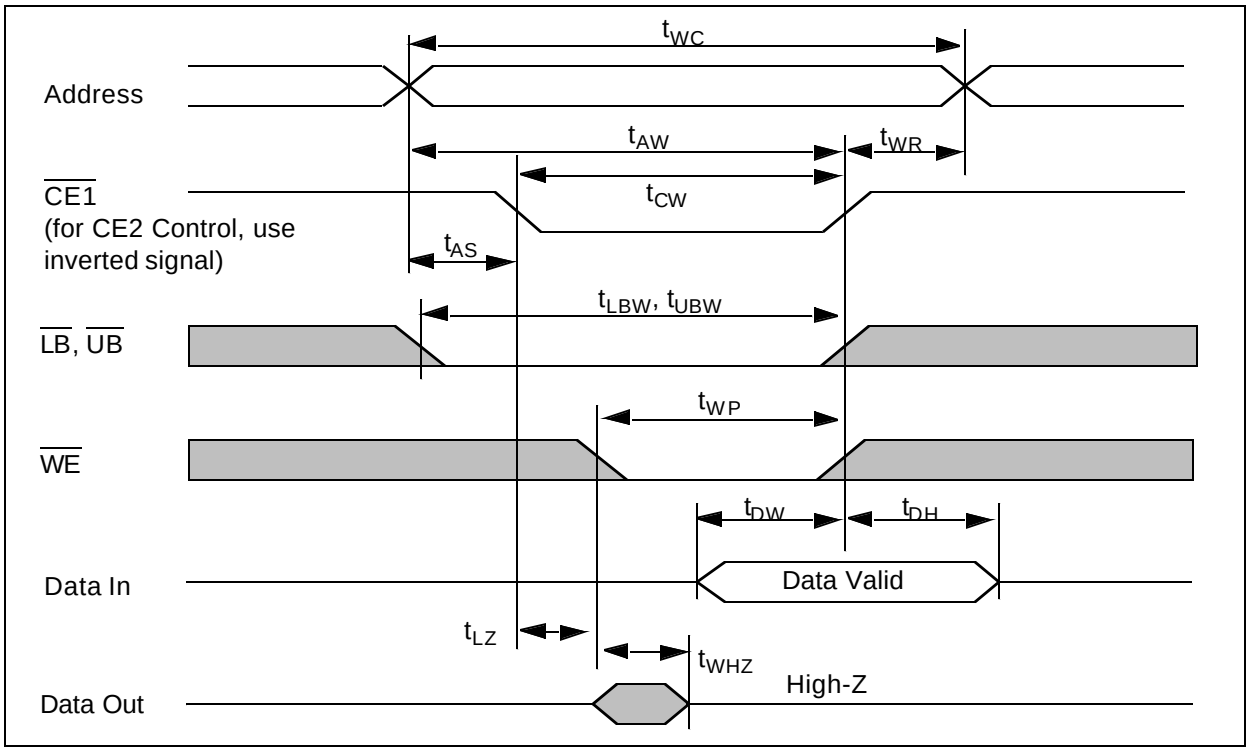
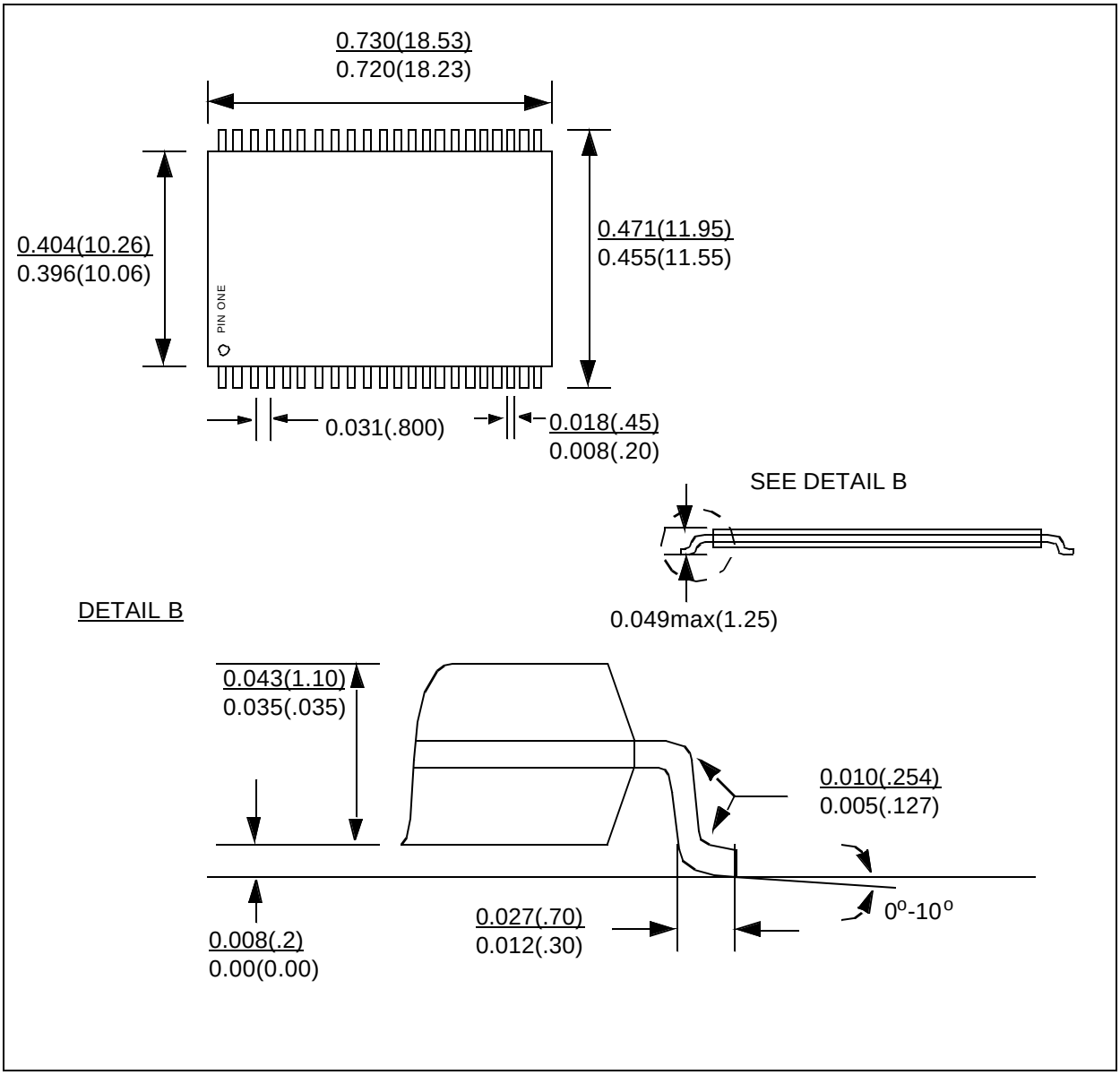



**FIGURE 7: Timing Waveform of Write Cycle (2) ($\overline{CE1}$ Control)**

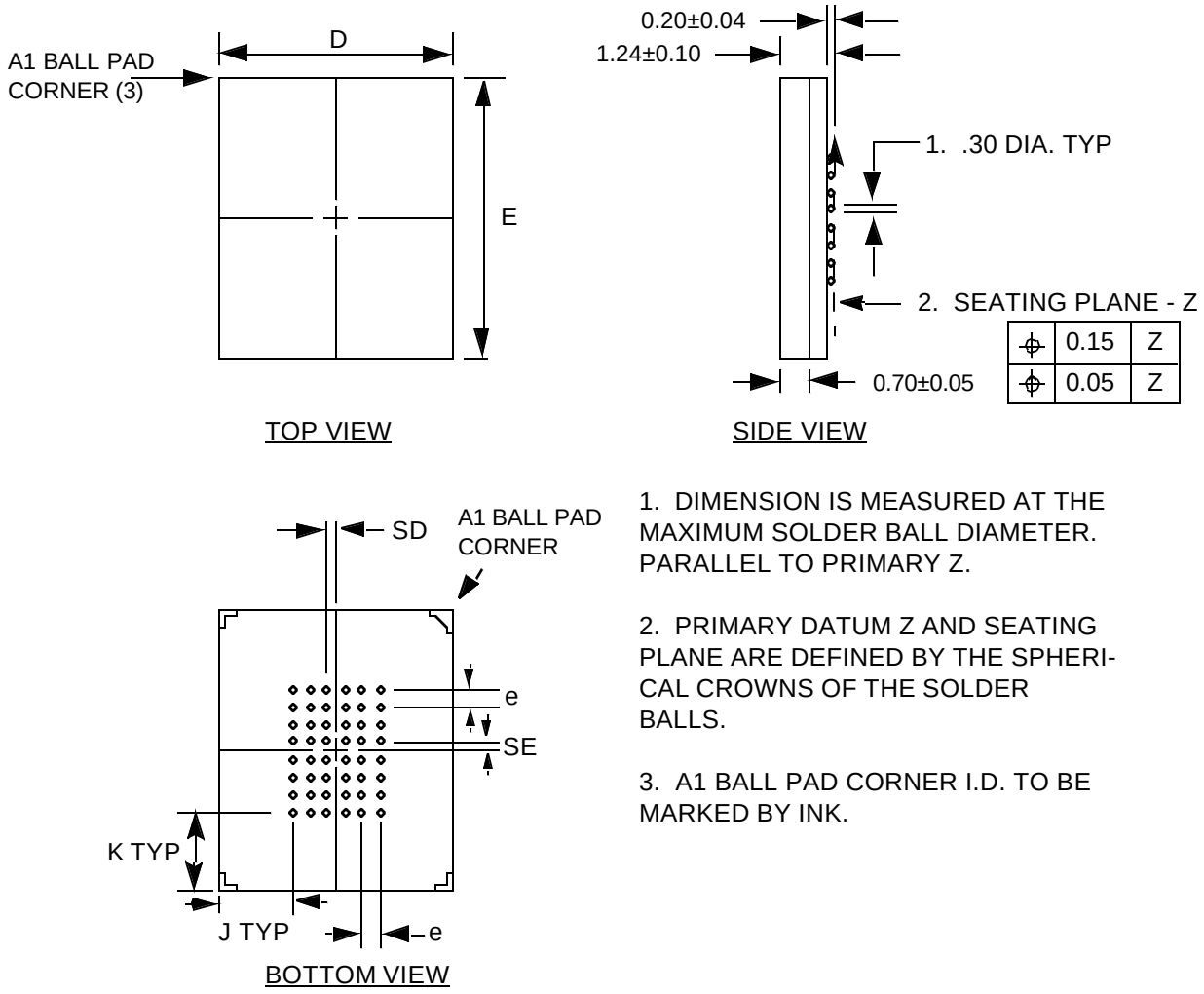


## FIGURE 8: 44-LEAD TSOP PACKAGE (T44)




Note:
1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

## FIGURE 9: BALL GRID ARRAY PACKAGING




1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

## TABLE 8: Dimensions (mm)

| D | E | e = 0.75 | | | | BALL MATRIX TYPE |
|---|---|---|---|---|---|---|
| | | SD | SE | J | K | |
| 6 | 8 | 0.375 | 0.375 | 1.125 | 1.375 | FULL |

## TABLE 9: Ordering Information

| Part Number* | Package | Temperature Range | Voltage Range | Speed |
|---|---|---|---|---|
| EM064J16B | 48 pin BGA | -40 to +85°C | 2.3 to 3.6 V | 70 ns |
| EM064J16T | 44 pin TSOP | -40 to +85°C | 2.3 to 3.6 V | 70 ns |

* This part number must appear on your order.

## TABLE 10: Revision History

| Revision | Date | Change Description |
|---|---|---|
| 01 | Jan 2001 | Initial preliminary release |
| 02 | Mar 2001 | Corrected Figure 1: TSOP Pin Configuration, pins 18-22. Modified $I_{CC3}$ and figure 8, other minor edits |