ESS Technology, Inc.

ES4408FD
DVD Processor
Product Brief

DESCRIPTION

The ES4408FD processor provides a single-chip solution for a Digital Versatile Disc (DVD) player that integrates MPEG video decoding, DVD system navigation, Content Scrambling System (CSS) protection, and both Dolby™ Digital (AC-3), Digital Theater System (DTS), and MPEG audio decoding. The fully programmable ES4408FD offers the best feature set in comparison to any currently existing DVD processor. The ES4408FD includes a glueless interface to various peripheral components, making it the most cost effective solution in its class with an integration level and quality that set new benchmarks.

The ES4408FD DVD processor is capable of decoding Dolby™ Digital (AC-3), DTS and MPEG audio up to 7.1 channels simultaneously with MPEG-1 or MPEG-2 video. For embedded applications, the internal 32-bit RISC processor of the ES4408FD can be used in place of a microcontroller to provide all system control, DVD system navigation, CSS decryption, and many other features. On-chip, multi-tap filters provide arbitrary scaling with state of the art SmartScale™ technology useful for video standards conversion. SmartStream™ technology from ESS provides video error concealment and video post-processing, leading to the highest playability and video quality. The ES4408FD also supports both letterbox and pan and scan displays, DVD subpicture overlay, and On-Screen Display.

The ES4408FD provides a glueless 8/16-bit parallel interface to many DVD servo/loaders. It connects directly with 8/16-bit ROM and 16-bit SDRAM/EDO memories. An 8-bit YUV video interface supports many TV encoders. General purpose auxiliary pins are provided to control various peripheral devices. A standard I^2S interface supports popular audio DACs and ADCs. The ES4408FD also features a direct S/PDIF output.

The media bitstream from a DVD disc is passed to the ES4408FD through a 8-bit/16-bit parallel host interface. The ES4408FD parses the system layer and demultiplexes the audio and video streams. Audio is decoded and passed through the I^2S audio serial bus to an external audio DAC for audio playback. Video is decoded and output as YUV pixels to an NTSC or PAL video encoder. System control and housekeeping functions (keypad and remote control) are also provided on-chip.

The ES4408FD is available in an industry-standard 208-pin Plastic Quad Flat Package (PQFP).

FEATURES

- Single-chip DVD processor in a 208-pin PQFP package
- Supports MPEG-1 system and MPEG-2 program streams
- Programmable multimedia processor architecture
- Compatible with Audio CD, VideoCD 1.1, 2.0, Interactive VCD 3.0, and Super VideoCD (SVCD)
- DVD Navigation 1.0
- Built-in Content Scrambling System (CSS) protection
- On-chip DVD Control Interface supports ATAPI and A/V DVD loaders.
- On-chip, 4-bit On-Screen Display (OSD) controller supports standard television remote control functions, DVD/VCD/SVCD navigation functions and performs 4-bit pixel blending.
- On-chip Subpicture Unit (SPU) decoder supports karaoke lyric, closed captioning and subtitle text display functions.
- Supports up to 8 MB of SDRAM
- Independent audio bit clock for transmit and receive port
- Single 27 MHz clock input

Video

- Pan and scan and letterbox widescreen DVD video display playback modes supported.
- SmartScale™ for NTSC to PAL conversion and vice versa supported.
- SmartStream™ for video error concealment supported.
- SmartZoom™ for motion zoom and pan supported.
- 8-bit YUV output

Audio

- Karaoke function
- Dolby™ Digital (AC-3) and DTS S/PDIF digital audio output
- Dolby™ Digital (AC-3) and DTS 5.1 channel audio decoded
- Dolby™ Digital Class A and DTS certified
- MPEG audio up to 7.1 channel
- Linear PCM streams from 48 kHz to 96 KHz
- Supports 256/384/512 frame sync audio system clock

PINOUT

Figure 1 shows the device pinout for the ES4408FD.

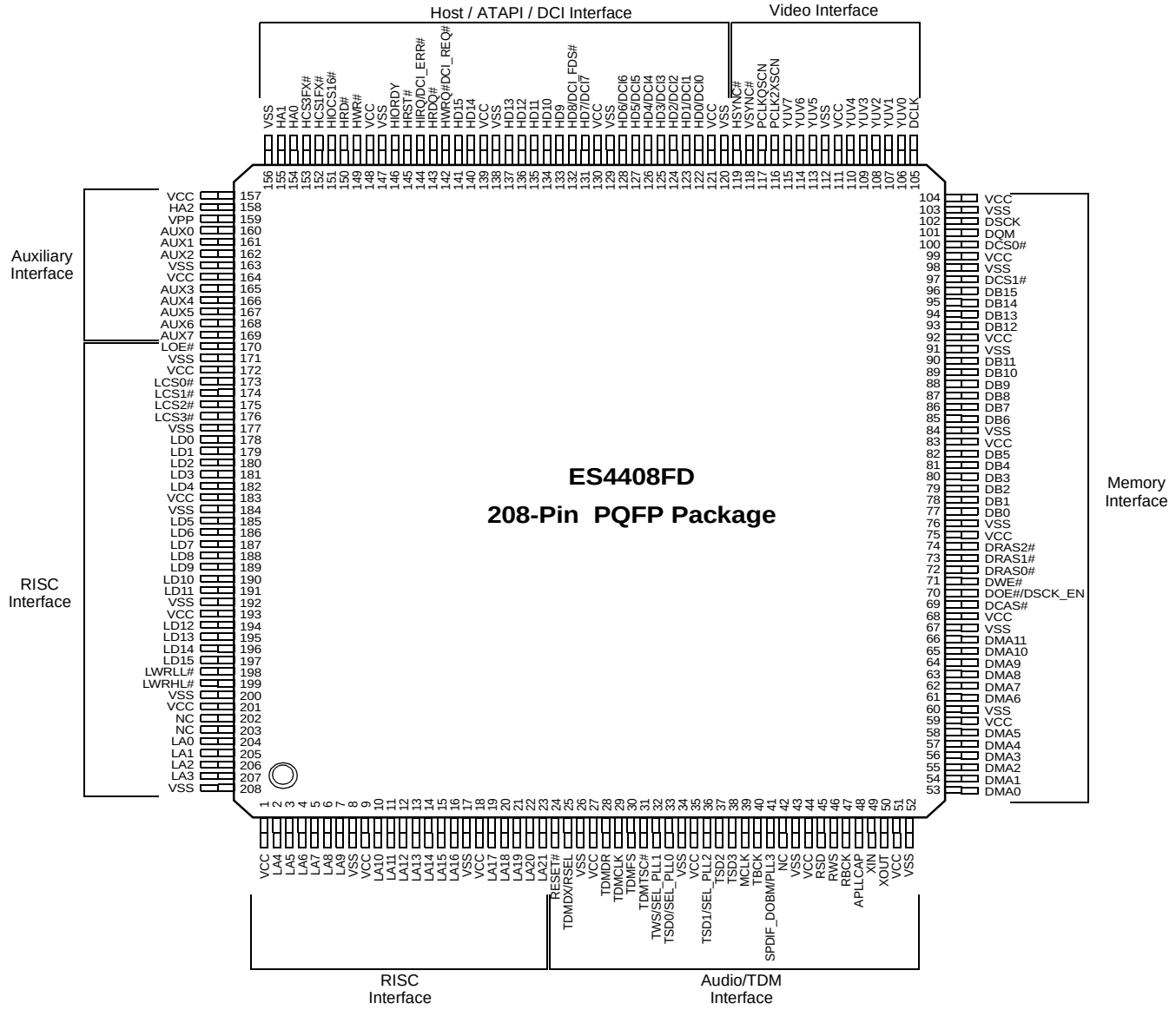


Figure 1 ES4408FD Device Pinout

PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES4408FD.

Table 1 ES4408FD Pin Descriptions

Name	Number	I/O	Definition
VCC	1, 9, 18, 27, 35, 44, 51, 59, 68, 75, 83, 92, 99, 104, 111, 121, 130, 139, 148, 157, 164, 172, 183, 193, 201	I	Supply voltage.

Table 1 ES4408FD Pin Descriptions (Continued)

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>LA[21:0]</td><td>23:19,16:10,7:2, 207:204</td><td>O</td><td>Device address output.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>I</td><td>Ground.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data.</td></tr>
<tr><td>RSEL</td><td>I</td><td>ROM Select
<table><tr><th>RSEL</th><th>Selection</th></tr><tr><td>0</td><td>16-bit ROM</td></tr><tr><td>1</td><td>8-bit ROM</td></tr></table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable, active low.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>Select PLL2 input.</td></tr>
<tr><td>TSD[0]</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data output 0.</td></tr>
<tr><td>SEL_PLL 0</td><td>I</td><td>Select PLL0 input.
<table><tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Output</th></tr><tr><td>0</td><td>0</td><td>0</td><td>VCO Off</td></tr><tr><td>0</td><td>0</td><td>1</td><td>27.0 MHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Bypass</td></tr><tr><td>0</td><td>1</td><td>1</td><td>54.0 MHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>121.5 MHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>81.0 MHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>94.0 MHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>108.0 MHz</td></tr></table></td></tr>
<tr><td>TSD[1]</td><td rowspan="2">36</td><td>O</td><td>Audio transmit serial data output 1.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Select PLL1 input</td></tr>
<tr><td>TSD[2]</td><td>37</td><td>O</td><td>Audio transmit serial data output 2.</td></tr>
<tr><td>TSD[3]</td><td>38</td><td>O</td><td>Audio transmit serial data output 3.</td></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>I/O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPDIF_DOBM</td><td rowspan="2">41</td><td>O</td><td>S/PDIF (IEC958) Format Output.</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock Source Select.
<table><tr><th>SEL_PLL3</th><th>Clock Source</th></tr><tr><td>0</td><td>Crystal oscillator</td></tr><tr><td>1</td><td>DCLK input</td></tr></table></td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync.</td></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock.</td></tr>
<tr><td>APLLCAP</td><td>48</td><td>I</td><td>Analog PLL Capacitor.</td></tr>
</table>

Table 1 ES4408FD Pin Descriptions (Continued)

Name	Number	I/O	Definition
XIN	49	I	Crystal input.
XOUT	50	O	Crystal output.
DMA[11:0]	66:61,58:53	O	DRAM address bus.
DCAS#	69	O	DRAM Column address strobe, active low.
DOE#	70	O	DRAM Output enable, active low.
DSCK_EN		I	DRAM Clock Enable, active low.
DWE#	71	O	DRAM write enable, active low.
DRAS[2:0]#	74:72	O	DRAM Row address strobe, active low.
DB[15:0]	96:93,90:85,82:77	I/O	DRAM data bus.
DCS[1:0]#	97,100	O	SDRAM chip select [1:0], active low.
DQM	101	O	Data input/output mask.
DSCK	102	O	Clock to SDRAM.
DCLK	105	I	Clock Input (27 MHz)
YUV[7:0]	115:113,110:106	O	8-bit YUV output.
PCLK2XSCN	116	I/O	Doubled screen 27-MHz pixel clock.
PCLKQSCN	117	I/O	Screen Pixel clock.
VSYNC#	118	I/O	Vertical sync for video display interface, programmable for rising or falling edge, active low.
HSYNC#	119	I/O	Horizontal sync for screen video interface, programmable for rising or falling edge, active low.
HD[15:0]	141:140,137:131, 128:122	O	Host data bus
HCS1FX#	152	O	Host select 1.
HCS3FX#	153	O	Host select 3.
HIOCS16#	151	I	Device 16-bit data transfer.
HA[2:0]	158, 155:154	I/O	Host address bus.
VPP	159	I	Peripheral protection voltage.
HWR#/ DCI_ACK#	149	I,O	Host write/DCI Interface Acknowledge Signal, active low.
HRD#/ DCI_CLK	150	O,O	Host read/DCI Interface Clock.
HWRQ#	142	O	Host write request.
HRDQ#	143	O	Host read request.
HIRQ	144	I/O	Host interrupt.
HRST#	145	O	Host reset.
HIORDY	146	I	Host I/O ready.
AUX[7:0]	169:165,162:160	I/O	Auxiliary ports.
LOE#	170	O	Device output enable, active low.
LCS[3:0]#	176:173	O	Chip select [3:0], active low.
LD[15:0]	197:194, 191:185, 182:178	I/O	Device data bus.
LWRLL#	198	O	Device write enable, active low.
LWRHL#	199	O	Device write enable, active low.
NC	37,38,42,203:202	—	No connect pins. Leave open.

SYSTEM BLOCK DIAGRAM

Figure 2 shows a sample system block diagram using the ES4408FD.

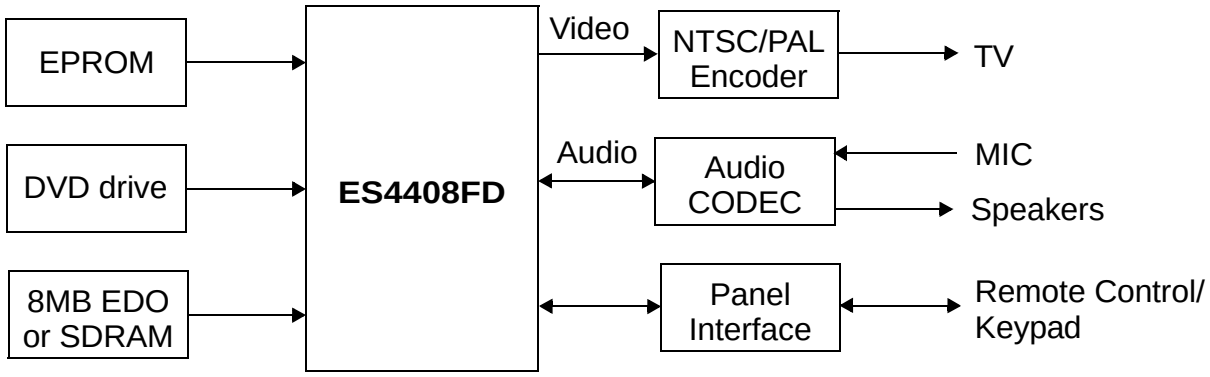
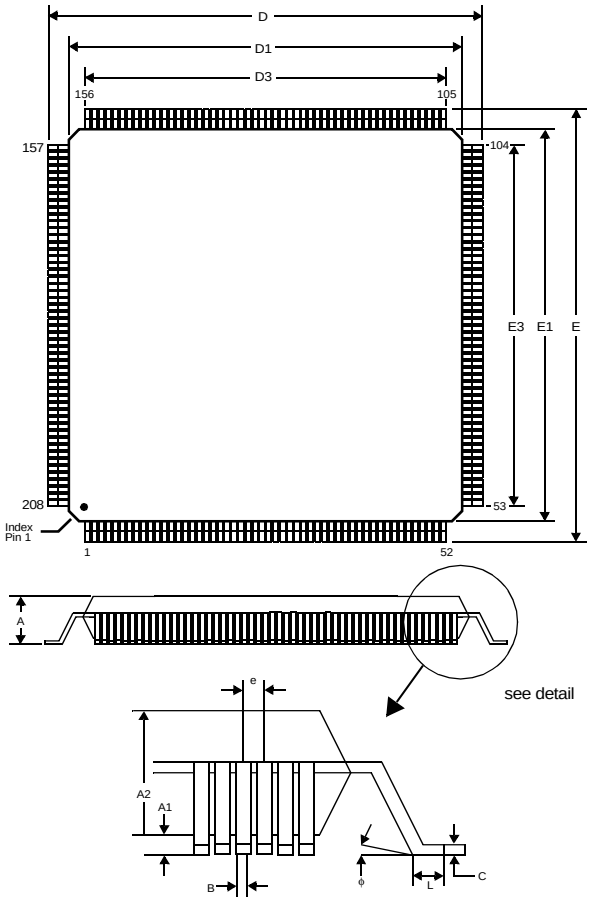


Figure 2 ES4408FD System Block Diagram

MECHANICAL DIMENSIONS

Figure 3 shows the mechanical dimensions of the ES4408FD.



Note:
1. All dimensions are in inches (millimeters).
2. Actual package used has millimeter native dimensions – take care with rounding from metric to imperial.

Symbol	Min	Nom	Max
A	–	–	0.165
A1	0.010 (0.25)	–	–
A2	0.130 (3.30)	0.134 (3.40)	0.138 (3.50)
B	0.007 (0.18)	0.009 (0.23)	0.011 (0.28)
C	0.005 (0.12)	0.006 (0.16)	0.008 (0.20)
D	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
D1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
D3	1.004 (25.50) REF		
e	0.0197 (0.50) BASIC		
E	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
E1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
E3	1.004 (25.50) REF		
L	0.016 (0.40)	0.020 (0.50)	0.024 (0.60)
f	0 i	2.5 i	5.0 i

Figure 3 ES4408FD Mechanical Dimensions

ORDERING INFORMATION

Part Number	Description	Package
ES4408FD	DVD Processor	208-pin PQFP

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