Features

- 8 Meg x 64 organization
- Extended Data Out (EDO)
- CAS-before RAS refresh capability
- TTL compatible inputs and outputs
- Fast access time - 60ns and 70ns
- JEDEC Standard 168 pin DIMM
- Single +3.3Volt ±10%
- On Board Decoupling Capcitors

8 Megx64
High Density DRAM DIMM

The EDI4G649EV is an industry standard 168-Pin 8-byte Dual In-Line Memory Module (DIMM) which is configured as an 8 Meg x 64. The module is well suited for applications requiring large memory arrays.
The on-DIMM buffering of selected input signals provides improved system performance. Both the DATA and RAS signals are not buffered, which preserves the DRAM access specification. The EDI4G649EV is assembled using (8) 8 Meg x 8 EDO DRAMs.

Pin Names

A0,B0,A1 - A11	Address Inputs (Buffered)
CAS 0-7	Column Address Strobe (Buffered)
$\overline{RAS0,2}$	Row Address Strobe
$\overline{W0}$, $\overline{W2}$	Read/Write Enable (Buffered)
DQ0-63	Data Input/Output
PD1-8	Presence Detect Pins (Buffered)
PDE	Presence Detect Enable
IDO-ID1	ID Bits
VCC	3.3V ±10%
VSS	Ground
NC	No Connection
$\overline{G0}$, $\overline{G2}$	Output Enable (Buffered)

Presence Detect

	70ns	60ns
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	1	1
PD8	1	1
ID0	0	0
ID1	0	0

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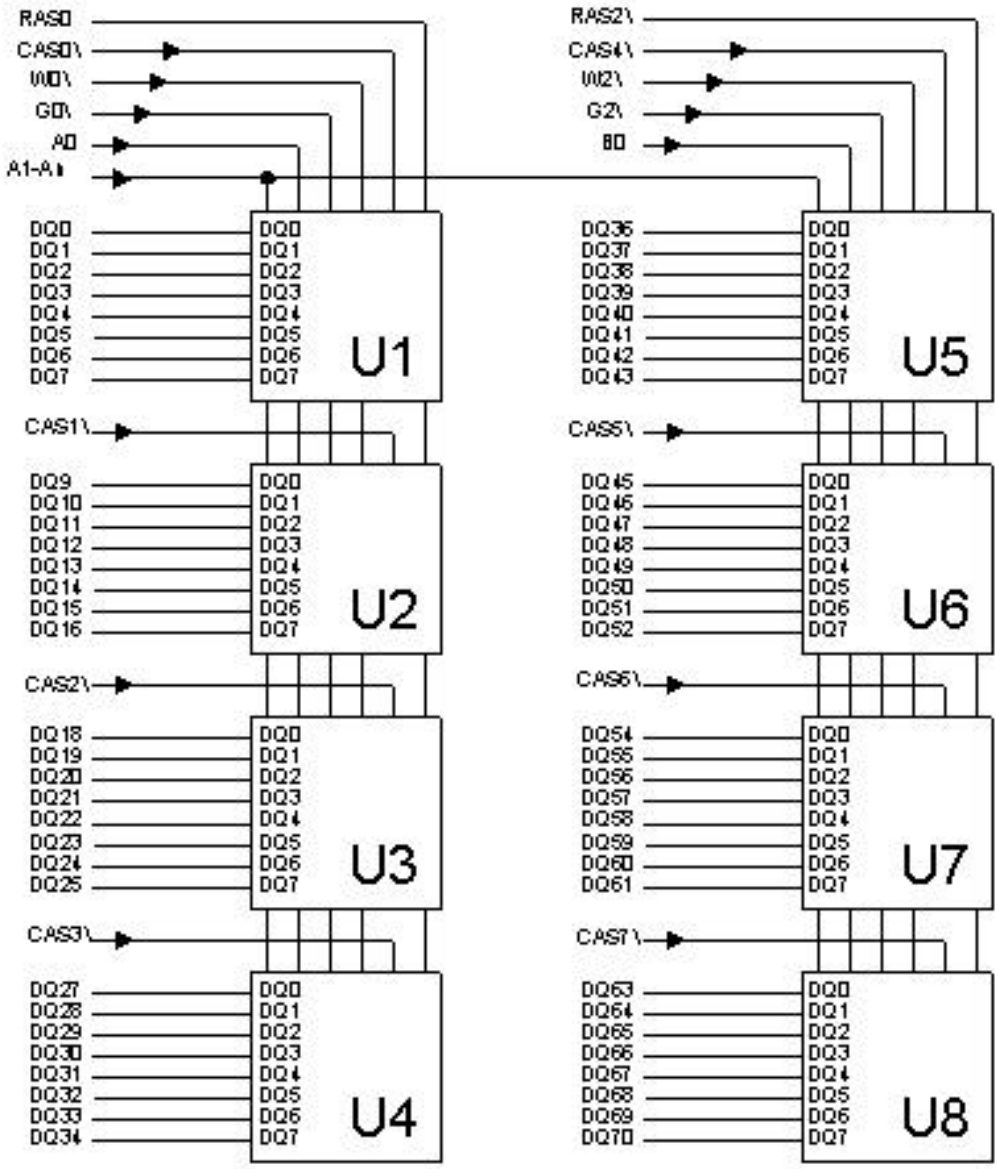
Pin Configurations

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	85	VSS	43	VSS	127	VSS
2	DQ0	86	DQ36	44	G2	128	NC
3	DQ1	87	DQ37	45	RAS2	129	NC
4	DQ2	88	DQ38	46	CAS4	130	CAS5
5	DQ3	89	DQ39	47	CAS6	131	CAS7
6	VCC	90	VCC	48	W2	132	PDE
7	DQ4	91	DQ40	49	VCC	133	VCC
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	NC	95	NC	53	DQ19	137	DQ55
12	VSS	96	VSS	54	VSS	138	VSS
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	VCC	143	VCC
18	VCC	102	VCC	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	NC	106	NC	64	NC	148	NC
23	VSS	107	VSS	65	DQ25	149	DQ61
24	NC	108	NC	66	NC	150	NC
25	NC	109	NC	67	DQ27	151	DQ63
26	VCC	110	VCC	68	VSS	152	VSS
27	W0	111	NC	69	DQ28	153	DQ64
28	CAS0	112	CAS1	70	DQ29	154	DQ65
29	CAS2	113	CAS3	71	DQ30	155	DQ66
30	RAS0	114	NC	72	DQ31	156	DQ67
31	G0	115	NC	73	VCC	157	VCC
32	VSS	116	VSS	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	NC	161	NC
36	A6	120	A7	78	VSS	162	VSS
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	VCC	124	VCC	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	VCC	168	VCC

Block Diagram



Absolute Maximum Ratings*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to VSS	VIN,VOUT	-0.5 to +4.6	V
Voltage on VCC supply relative to VSS	VCC	-0.5 to +4.6	V
Storage Temperature	TSTG	-40 to +125	°C
Power Dissipation	PD	4	W
Short Circuit Output Current	IOS	50	mA

*Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(Voltages referenced to VSS, TA = 0 to 70°C)

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Ground	VSS	0	0	0	V
Input High Voltage	VIH	2.4	-	VCC+0.3[1]	V
Input Low Voltage	VIL	-0.3[2]	-	0.8	V

Notes: 1. VCC +1.3V15ns(3.3V), Pulse width is measured at VCC.
2. -1.3V/15ns(3.3V), Pulse width is measured at VSS.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Typ	Unit
Input Capacitance (Address)	CA	13	pF
Input Capacitance (W)	CW	13	pF
Input Capacitance (RAS)	CR	40	pF
Input Capacitance (CAS)	CC	13	pF
Output Capacitance	CDQ	15	pF

DC and Operating Characteristics

(EDI4G649EV, 8 Meg x 64)
(Recommended operating conditions unless otherwise noted)

Parameter	Sym	Conditions		60ns/70ns Min	60ns/70ns Max	Units
Operating Current	ICC1*	RAS+CAS cycling @ tRC=min			1048	mA
Standby Current	ICC2	RAS=CAS=W=VIH			16	mA
RAS-Only Refresh Current	ICC3*	CAS=VIH, RAS cycling @ TRC=min			880	mA
Hyper Page Mode Current	ICC4*	RAS=VIL,CAS, Address cycling @ TPC=min		640		mA
Standby Current	ICC5	RAS=CAS=W=VCC-0.2V			8	mA
CAS-Before-RAS Refresh Current	ICC6*	RAS and CAS cycling @ TRC=min			960	mA
Input Leakage Current Address	IIL	Any input 0<VIN<VCC+0.3V all other pins not under test = 0 Volts		±10	±10	µA
Input Leakage Current RAS 0,2, CAS 0-7	IIL	Any input 0<VIN<VCC+0.3V all other pins not under test =0 Volts	CAS RAS	±10 ±40	±10 ±40	µA µA
Input Leakage Current W\	IIL	Any input 0<VIN<VCC+0.3V all other pins not under test = 0 Volts		±10	±10	µA
Output Leakage Current	IOL	Data out is disabled, 0V<VOUT<VCC		±10	±10	µA
Output High Voltage Level	VOH	IOH=-2mA		2.4		V
Output Low Voltage Level	VOL	IOL = 2mA			0.4	V

* Note: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1, ICC3, and ICC6, address can be changed maximum once while RAS=VIL. In ICC4, address can be changed maximum once within one fast page mode cycle time, TPC.

AC Characteristics

(0°C-TA-70°C, See note 1,2)
(Test condition: VCC=3.3V±10%, VIH/VIL=2.0/0.8V, VOH/VOL=2.4/0.4V)

	Symbol	60ns		70ns			
Parameter		**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Random read or write cycle time	TRC	104		124		ns	
Read-modify-write cycle time	TRWC	138		165		ns	
Access time from $\overline{RAS}$	TRAC		60		70	ns	3,4,9
Access time from $\overline{CAS}$	TCAC		15		20	ns	3,4,10
Access time from column address	TAA		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	TCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	TCEZ	3	13	3	15	ns	5
$\overline{OE}$ to output in Low-Z	TOLZ	3		3		ns	3
Transition time (rise and fall)	TT	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	TRP	40		50		ns	
$\overline{RAS}$ pulse width	TRAS	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	TRSH	15		20		ns	
$\overline{CAS}$ hold time	TCSH	45		50		ns	
$\overline{CAS}$ pulse width	TCAS	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	TRCD	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	TRAD	15	30	15	35	ns	8
$\overline{CAS}$ to $\overline{RAS}$ precharge time	TCRP	5		5		ns	
Row address set-up time	TASR	5		5		ns	
Row address hold time	TRAH	10		10		ns	
Column address set-up time	TASC	5		5		ns	
Column address hold time	TCAH	10		15		ns	
Column address to $\overline{RAS}$ lead time	TRAL	35		40		ns	
Read command set-up time	TRCS	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	TRCH	0		0		ns	7
Read command hold time referenced to$\overline{RAS}$	TRRH	0		0		ns	7
Write command hold time	TWCH	10		15		ns	
Write command pulse width	TWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	TRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	TCWL	15		20		ns	

See Notes on Page 6.

AC Characteristics

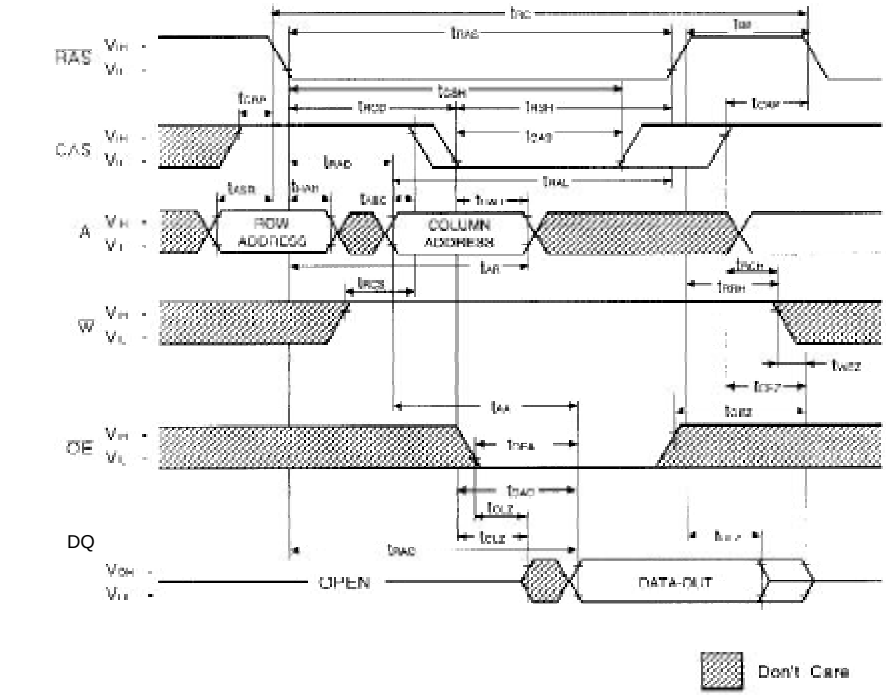
(0 ° C-TA-70 ° C, See note 1)
(Test condition (3V device): VCC=3.3V±10%, VIH/VIL=2.0/0.8V, VOH/VOL=2.4/0.4V)

Parameter	Symbol	60ns Min	60ns Max	70ns Min	70ns Max	Units	Notes
Data set-up time	TDS	0		0		ns	8
Data hold time	TDH	10		15		ns	8
Refresh period (4K/8K, Normal)	TREF		64		64	ms	
Write Command set-up time	TWCS	0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	TCWD	32		39		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	TRWD	77		89		ns	6
Column address to W delay time	TAWD	47		54		ns	6
$\overline{CAS}$ set-up time $\overline{CAS}$-before-$\overline{RAS}$ refresh	TCSR	10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	TCHR	10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	TRPC	5		5		ns	
Access time from $\overline{CAS}$ precharge	TCPA		35		40	ns	3
Hyper page cycle time	THPC	25		30		ns	
Hyper page read-modify-write cycle time	THPRWC	56		71		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	TCP	10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	TRASP	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	TRHCP	35		40		ns	
$\overline{OE}$ access time	TOEA		15		20		ns
$\overline{OE}$ to data delay	TOED	13		15		ns	
Output buffer turn off delay from $\overline{OE}$	TOEZ	0	13	0	15	ns	
$\overline{OE}$ command hold time	TOEH	15		20		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time (C-$\overline{B}$-$\overline{R}$ refresh)	TWRP	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-$\overline{B}$-$\overline{R}$ refresh)	TWRH	10		10		ns	
Output data hold time	TDOH	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	TREZ	3	15	3	20	ns	
Output buffer turn off delay from $\overline{W}$	TWEZ	3	15	3	20	ns	
$\overline{W}$ to data delay	TWED	15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	TOCH	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	TCHO	5		5		ns	
$\overline{OE}$ precharge time	TOEP	5		5		ns	
$\overline{W}$ pulse width (Hyper Page Mode)	TWPE	5		5		ns	

Notes:
1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load of equivalent to 2 TTL(5V device) loads and 100pF.
4. Operation within the TRCD(max) limit insures that TRAC(max) can be met. TRCD(max) is specified as a reference point only. If TRCD is greater than the specified TRCD(max) limit, then access time is controlled exclusively by TCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
6. TWCS, TRWD, TCWD, TAWD and TCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If TWCS≥TWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If TCWD≥TCWD(min), TRWD≥TRWD(min), TAWD≥TAWD(min) and TCPWD≥TCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either TRCH or TRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the TRAD(max) limit insures that TRAC(max) can be met. TRAD(max) is specified as a reference point only. If TRAD is greater than the specified TRAD (max) limit, then access time is controlled by TAA.
10. Assumes that TCRD≥TCRD (max).

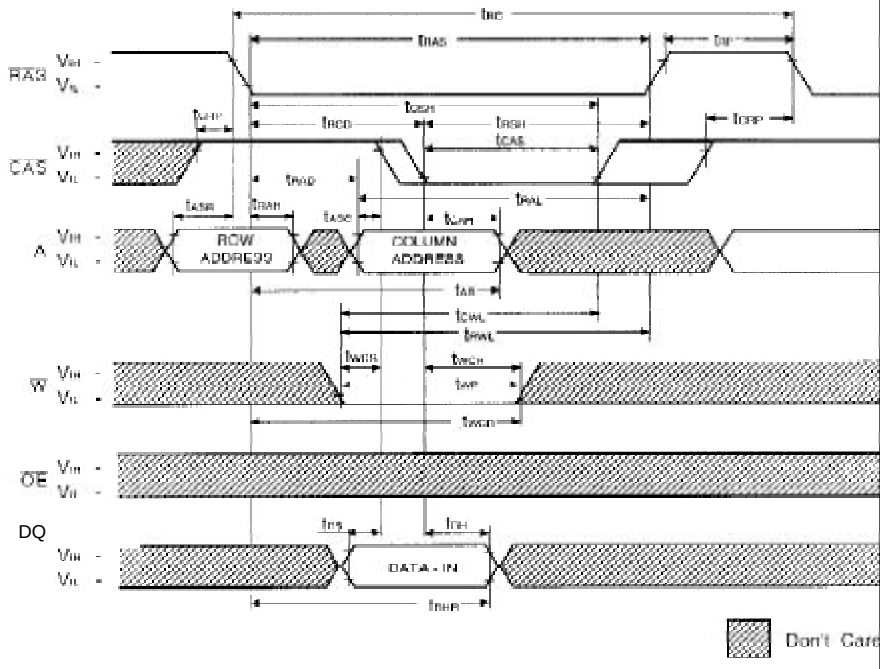
Timing Diagrams

READ CYCLE



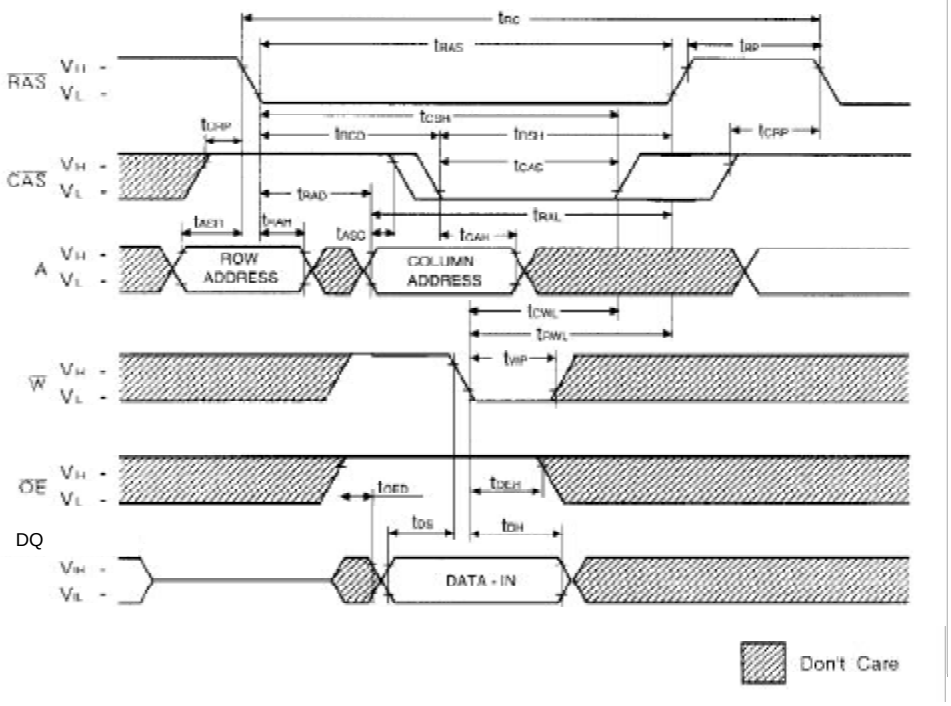
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN

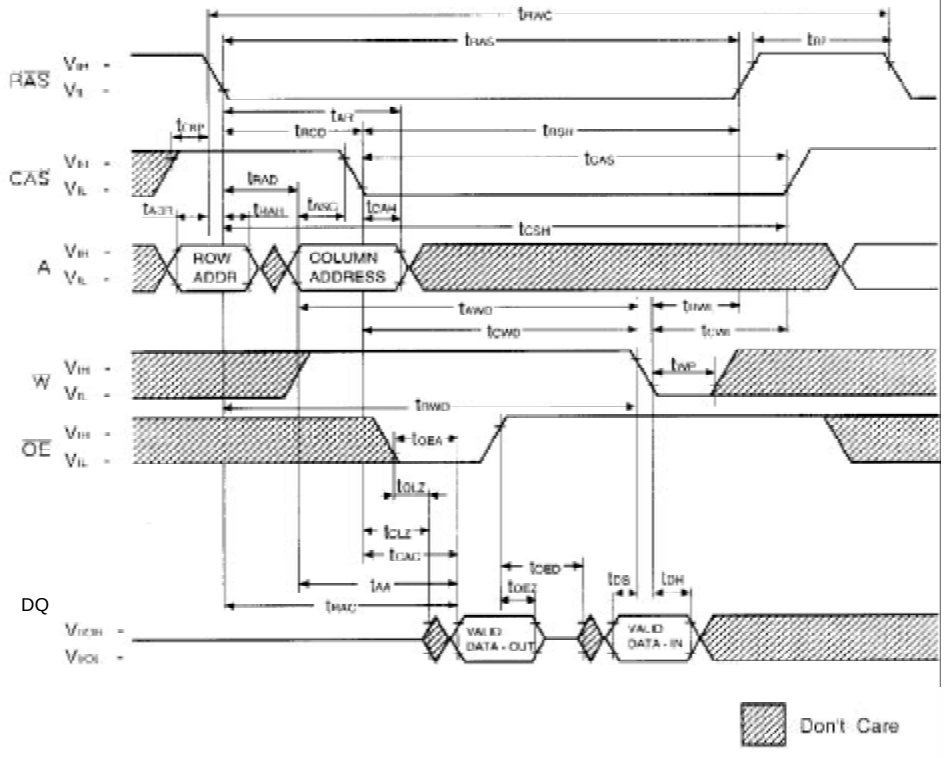


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

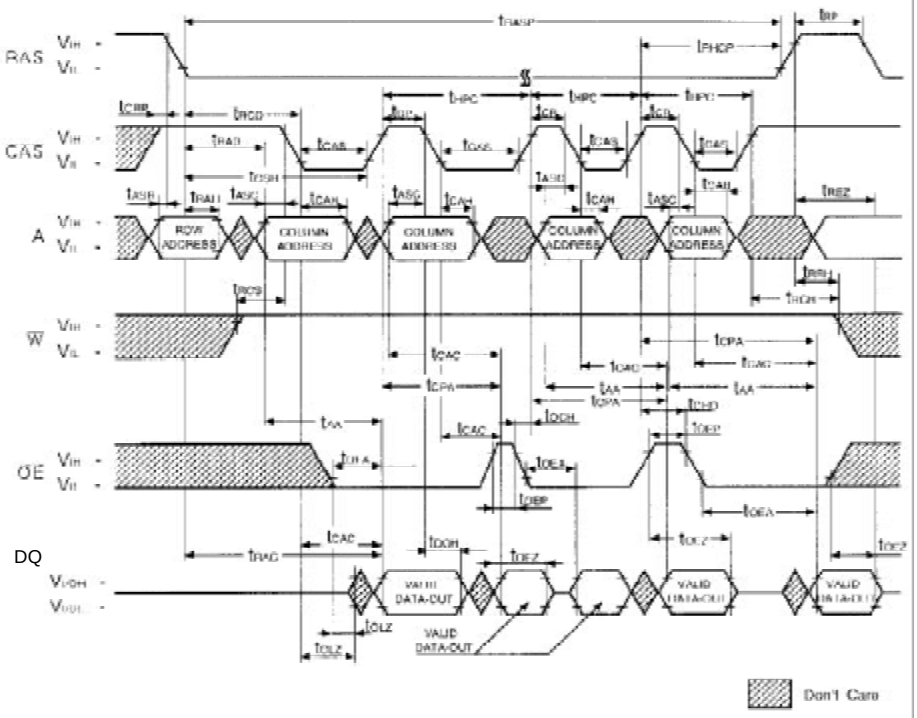
NOTE : D_{OUT} = OPEN



READ - MODIFY - WRITE CYCLE

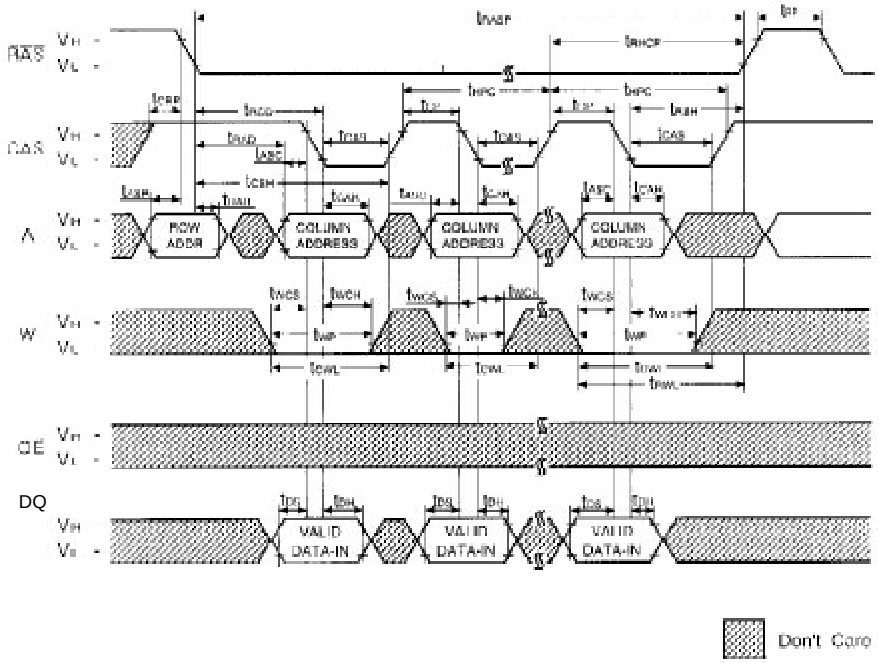


HYPER PAGE READ CYCLE

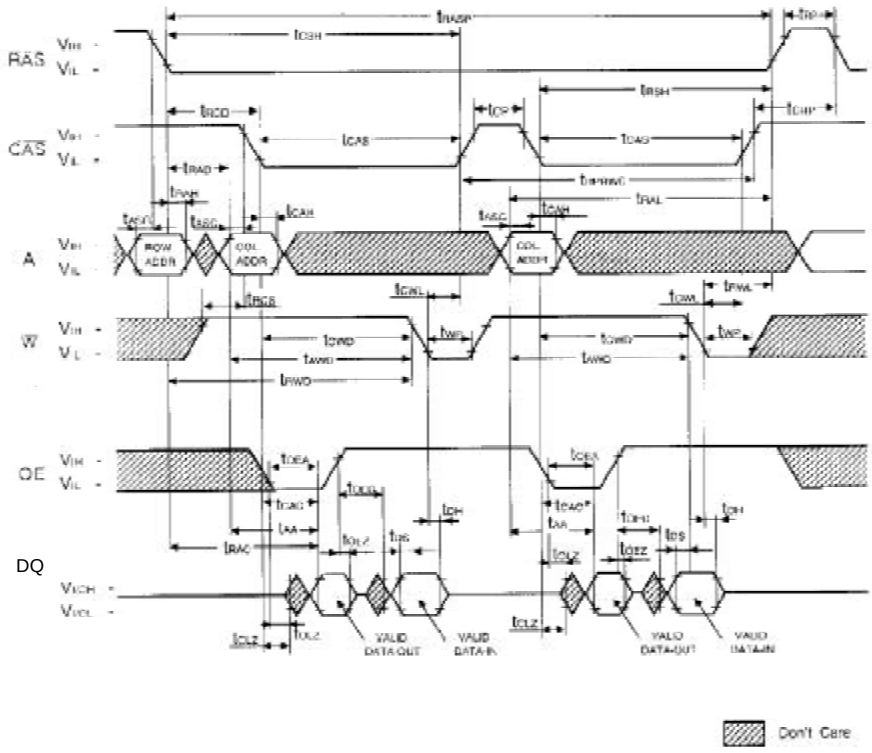


HYPER PAGE WRITE CYCLE (EARLY WRITE)

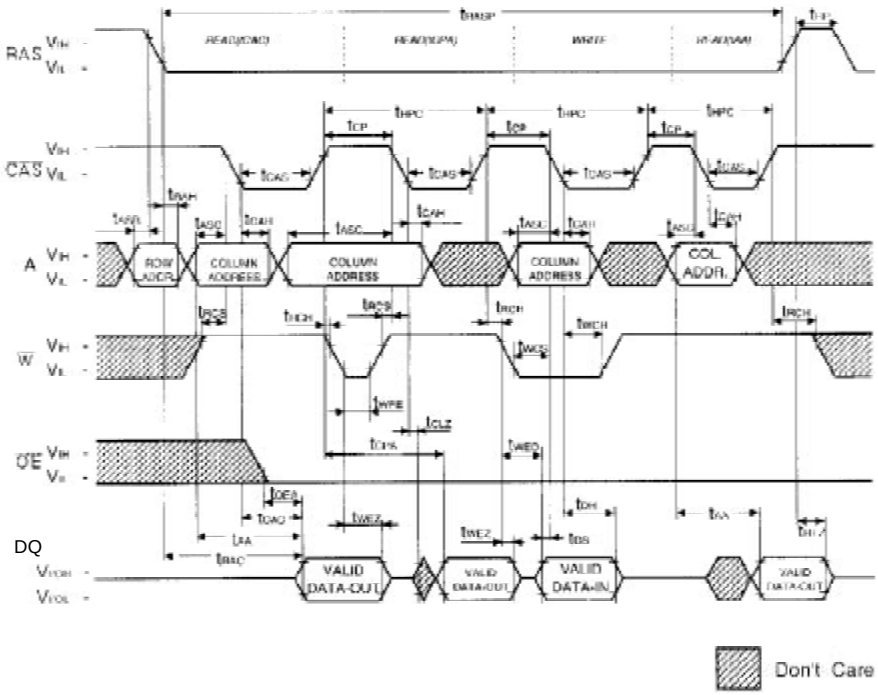
NOTE : Dout = Open



HYPER PAGE READ-MODIFY-WRITE CYCLE

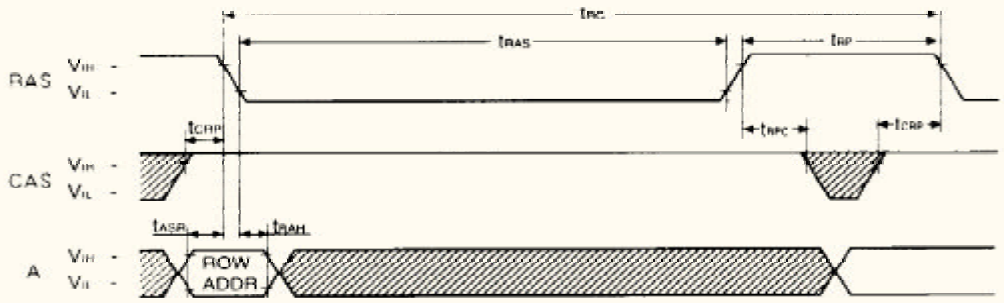


HYPER PAGE READ AND WRITE MIXED CYCLE



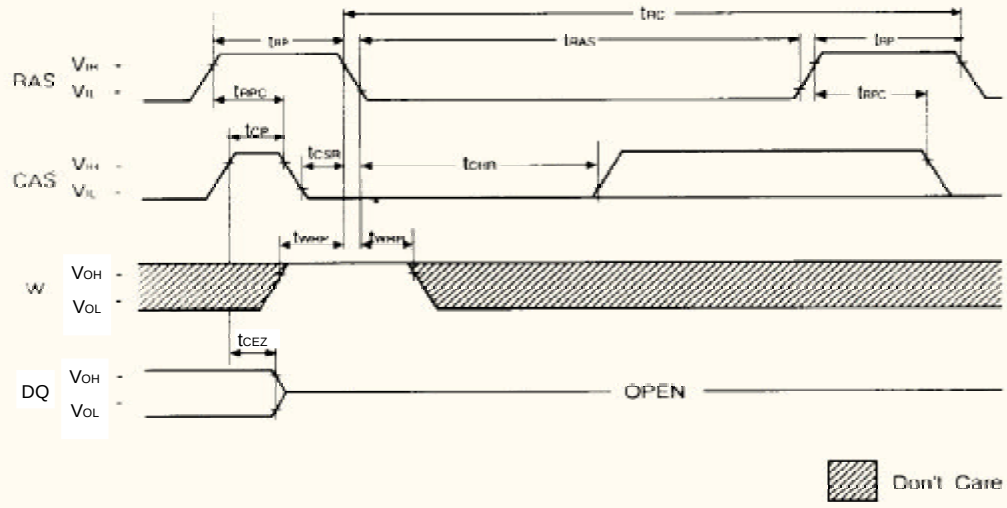
RAS-ONLY REFRESH CYCLE

NOTE : W D_{IN} = Don't care
D_{OUT} = Open

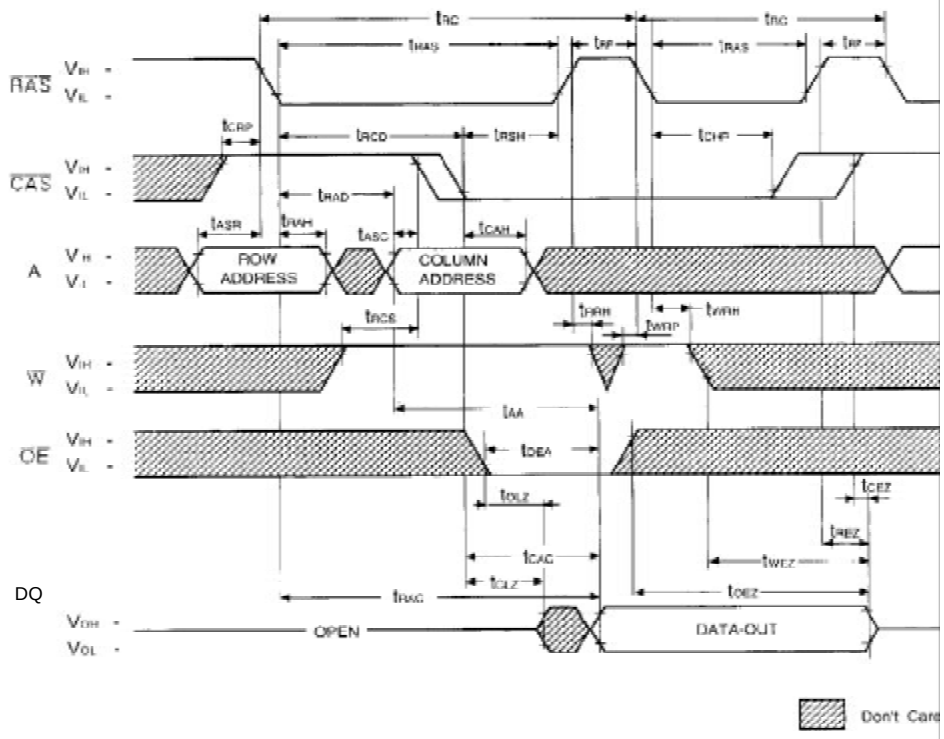


CAS-BEFORE-RAS REFRESH CYCLE

NOTE : A = Don't Care

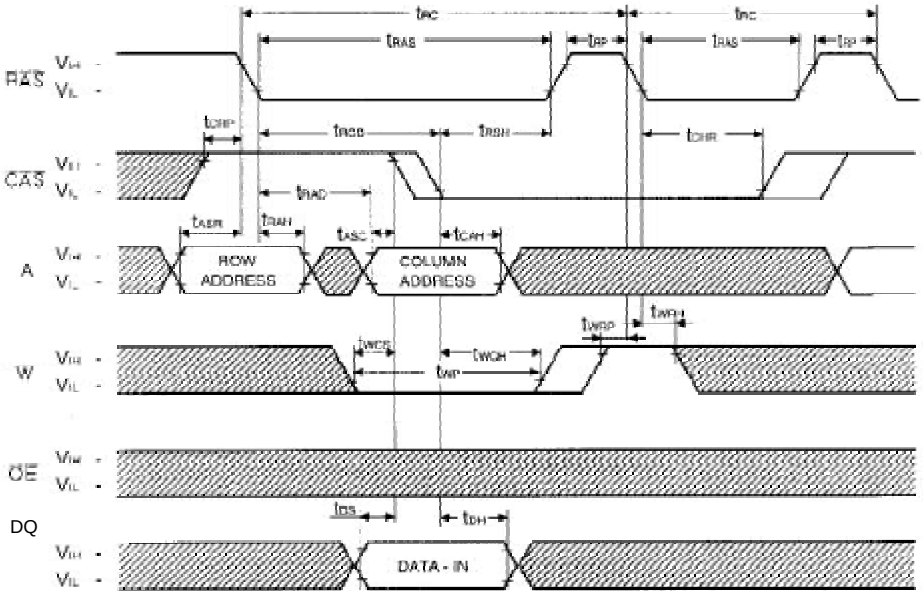


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Ordering Information

Part Number	Organization	Speed (ns)	Package No.
EDI4G649EV6D	8Meg x 64	60	429
EDI4G649EV7D	8Meg x 64	70	429

Package Description

Package No. 429