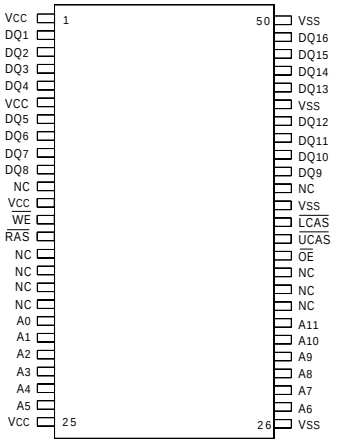
4Mx16 EDO (Extended Data Out) Dynamic RAM 3.3V

FEATURES

- Access Time: 50, 60 and 70ns
- 4 Meg x 16 bit CMOS Dynamic RAM
- Package:
  - 50 pin Plastic TSOP
- Extended Data Out Mode Operation
- Single +3.3V (±0.3V) Supply Operation
- 4096 Cycles Refresh
- $\overline{RAS}$ - Only, $\overline{CAS}$-before-$\overline{RAS}$, and HIDDEN refresh capability
- Low Operating Power Dissipation
- Low Standby Power
- Common I/O
- All Inputs/Outputs TTL Compatible
- Industrial (-40°C to +85°C) and Military (-55°C to +125°C) Temperature Ranges

PIN CONFIGURATION

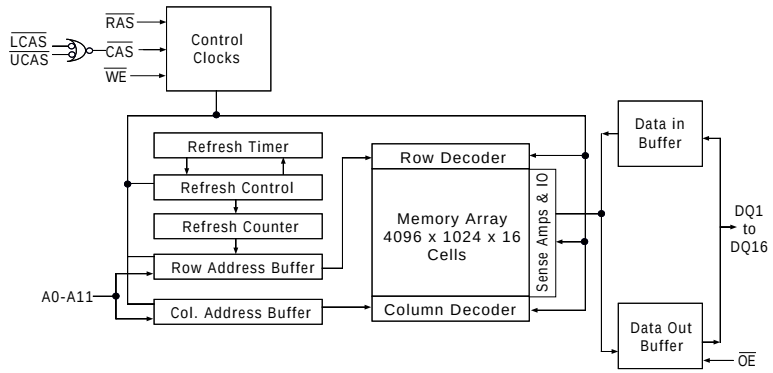
TOP VIEW



PIN DESCRIPTION

A0-11	Address Inputs
$\overline{LCAS}$ / $\overline{UCAS}$	Column Address Strobes
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable
DQ1-16	Data Inputs/Outputs
Vcc	Power (+3.3V±0.3V)
Vss	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature (Industrial)	-40°C to +85°C
Operating Temperature (Military)	-55°C to +125°C
Storage Temperature	-55°C to +150°C
Power Dissipation	1 Watt
Output Current	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(1)

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2	--	Vcc +0.3	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

NOTES:
1. All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Current	I_{CC1}	$\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @T_{RC} = min.			180	mA
Standby Current	I_{CC2}	$\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = $\overline{WE}$ = V_{IH}			4	mA
$\overline{RAS}$-only-Refresh Current	I_{CC3}	$\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}, $\overline{RAS}$, Addressing cycling @ T_{RC} = min			180	mA
EDO Mode Current	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$ Addressing cycling @ T_{RC} = min.			165	mA
Standby Current	I_{CC5}	$\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = $\overline{WE}$ = V_{CC} -0.2V			2	mA
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current	I_{CC6}	$\overline{RAS}$ and $\overline{UCAS}$ or $\overline{LCAS}$ cycling @ T_{RC}=min.			180	mA
Input Leakage Current	I_{IL}	0V ≤ V_{IN} ≤ Vcc +0.3V All Other Input Pins = 0V	-5		5	µA
Output Leakage Current	I_{OL}	0V ≤ V_{OUT} ≤ Vcc	-5		5	µA
Output High Voltage	V_{OH}	I_{OH} = -2.0mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	—	—	0.4	V

NOTES:

3. I_{CC1}(av), I_{CC3}(av), I_{CC4}(av), and I_{CC6} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. I_{CC1}(av) and I_{CC4}(av) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE

(f = 1.0MHz, T_A = 25°C, V_{CC} = 3.3V)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{IN1}	5	pF
Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{RAS}$)	C_{IN2}	7	pF
Output Capacitance (Q)	C_{DQ}	7	pF

TRUTH TABLE

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ1-8	DQ9-16	STATE
H	X	X	X	X	High Z	High Z	Standby
L	H	H	X	X	High Z	High Z	Refresh
L	L	H	H	L	DQ Out	High Z	Byte Read
L	H	L	H	L	High Z	DQ Out	Byte Read
L	L	L	H	L	DQ Out	DQ Out	Word Read
L	L	H	L	H	DQ In	—	Byte Write
L	H	L	L	H	—	DQ In	Byte Write
L	L	L	L	H	DQ In	DQ In	Word Write
L	L	L	H	H	High Z	High Z	—

TIMING REQUIREMENTS — READ, WRITE, READ-MODIFY-WRITE, REFRESH, AND PAGE MODE CYCLES

(V_{CC}=3.3V±0.3V) Notes 1, 2, 5

Parameter	Symbol	50ns Min	50ns Max	60ns Min	60ns Max	70ns Min	70ns Max	Unit	Notes
Random Read or Write Cycle Time	t_{RC}	90		110		130		ns	
Read-Modify-Write CycleTime	t_{RWC}	126		150		180		ns	
Access Time from $\overline{CAS}$	t_{CAC}		13		15		20	ns	3,4,5
Access Time from $\overline{RAS}$	t_{RAC}		50		60		70	ns	3,4,10
Access Time From Column Address	t_{AA}		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	6
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	ns	6,14
Transition Time	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	30		40		50		ns	
$\overline{RAS}$ Low Pulse Width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	t_{RSH}	13		15		20		ns	
$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	t_{CSH}	38		45		50		ns	
$\overline{CAS}$ Low Pulse Width	t_{CAS}	8	10,000	10	10,000	15	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	11	37	14	45	20	50	ns	4
Column Address Delay from $\overline{RAS}$ Low	t_{RAD}	9	25	12	30	15	35	ns	10
Delay $\overline{CAS}$ High to $\overline{RAS}$ Low	t_{CRP}	5		5		5		ns	
Row Address Set Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	9		10		10		ns	
Column Address Set Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	8		10		15		ns	
Column Address Hold Time Referenced $\overline{RAS}$	t_{AR}	40		45		55		ns	
Column Address to $\overline{RAS}$ Setup	t_{RAL}	25		30		35		ns	
Read Set Up Time before $\overline{CAS}$ Low	t_{RCS}	0		0		0		ns	
Read Hold Time after $\overline{CAS}$ High	t_{RCH}	0		0		0		ns	8
Read Hold Time after $\overline{RAS}$ High	t_{RRH}	0		0		0		ns	8
Write Hold Time after $\overline{CAS}$ Low	t_{WCH}	8		10		15		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	40		45		55		ns	
Write Pulse Width	t_{WP}	7		10		15		ns	
$\overline{RAS}$ Hold Time after Write Low	t_{RWL}	13		15		20		ns	
$\overline{CAS}$ Hold Time after Write Low	t_{CWL}	8		10		15		ns	
Data Set up Time	t_{DS}	0		0		0		ns	9
Data Hold Time after $\overline{CAS}$ Low	t_{DH}	8		10		15		ns	9
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	40		45		55		ns	
Refresh Cycle (Industrial)	t_{REF}		32		32		32	ms	
Refresh Cycle (Military)	t_{REF}		16		16		16	ms	
Write Setup Time before $\overline{CAS}$ Low	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ Low to $\overline{WE}$ Low Delay	t_{CWD}	30		35		45		ns	7
$\overline{RAS}$ Low to $\overline{WE}$ Low Delay	t_{RWD}	67		79		94		ns	7
Column Address Setup to $\overline{CAS}$ High	t_{ACH}	15		15		15		ns	
$\overline{OE}$ Low to Output Valid	t_{OE}		13		15		20	ns	13
$\overline{CAS}$ Low to DOUT	t_{COH}	3		3		3		ns	
$\overline{RAS}$ Low to $\overline{WE}$ Low	t_{WRH}	10		10		10		ns	
Write High to $\overline{RAS}$ Low	t_{WRP}	10		10		10		ns	
Address to $\overline{WE}$ Low Delay	t_{AWD}	48		55		65		ns	7

WRITE CYCLE, EARLY AND DELAYED WRITE

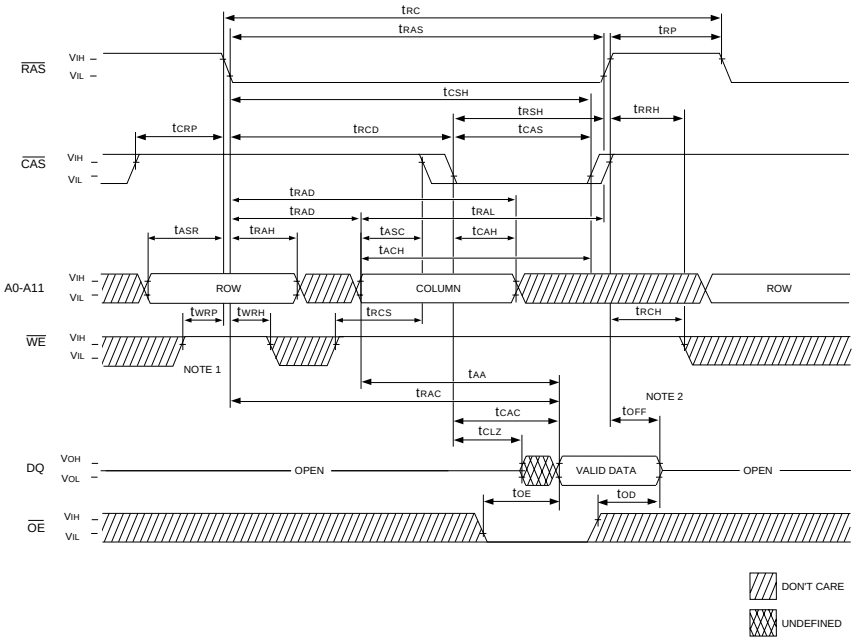
(VCC=3.3V±0.3V) Notes 1,2,5

Parameter	Symbol	50ns Min	50ns Max	60ns Min	60ns Max	70ns Min	70ns Max	Unit	Notes
$\overline{CAS}$ Setup for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CHR}	10		10		15		ns	
Precharge to $\overline{CAS}$ Active	t_{RPC}	5		5		5		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		28		35		40	ns	3
EDO Page Cycle Time	t_{PC}	20		25		30		ns	
EDO Page Read-Modify-Write Cycle Time	t_{PRWC}	47		56		71		ns	
$\overline{CAS}$ precharge time (EDO cycle)	t_{CP}	8		10		10		ns	
$\overline{RAS}$ pulse width (EDO Cycle)	t_{RASP}	50	125K	60	125K	70	125K	ns	
Output Disable Time after $\overline{OE}$ High	t_{OD}	0	13	0	15	0	20	ns	6
Write Low to Next $\overline{OE}$ Low	t_{OEH}	8		10		12		ns	
$\overline{OE}$ Low to $\overline{CAS}$ High Setup Time	t_{OES}	4		5		5		ns	
$\overline{OE}$ High Hold From $\overline{CAS}$ High	t_{OEHC}	5		10		10		ns	
$\overline{OE}$ High Pulse Width	t_{OEP}	7		10		10		ns	
$\overline{OE}$ Setup prior to $\overline{RAS}$ during Hidden Refresh Cycle	t_{ORD}	0		0		0		ns	
$\overline{OE}$ delay from $\overline{WE}$	t_{WHZ}	0	10	0	13	0	15	ns	
$\overline{WE}$ pulse to disable at $\overline{CAS}$ high	t_{WPZ}	10		10		10		ns	

NOTES:

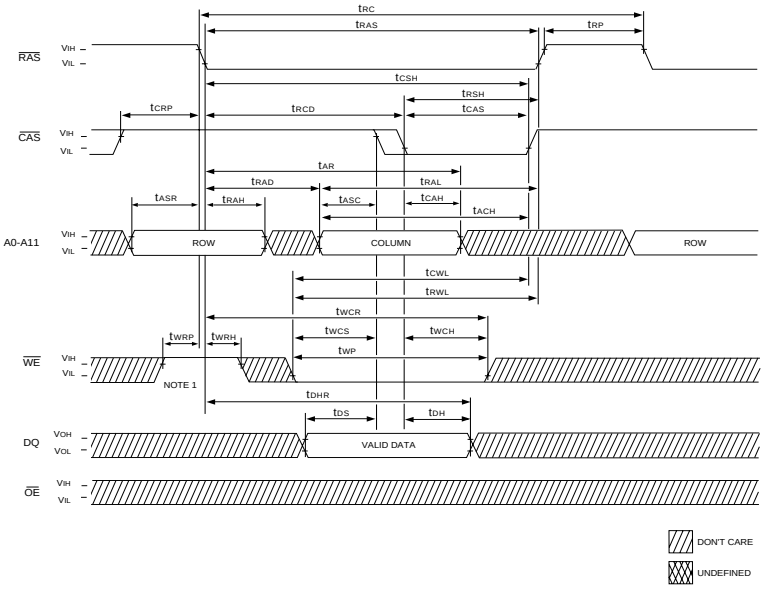
1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved, and must be repeated whenever t_{REF} is exceeded.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 3ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max)
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min) and $t_{AWD} > t_{AWD}$ (min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ falling edge in $\overline{OE}$ controlled write cycle and read-modify-write cycles.
10. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

READ CYCLE

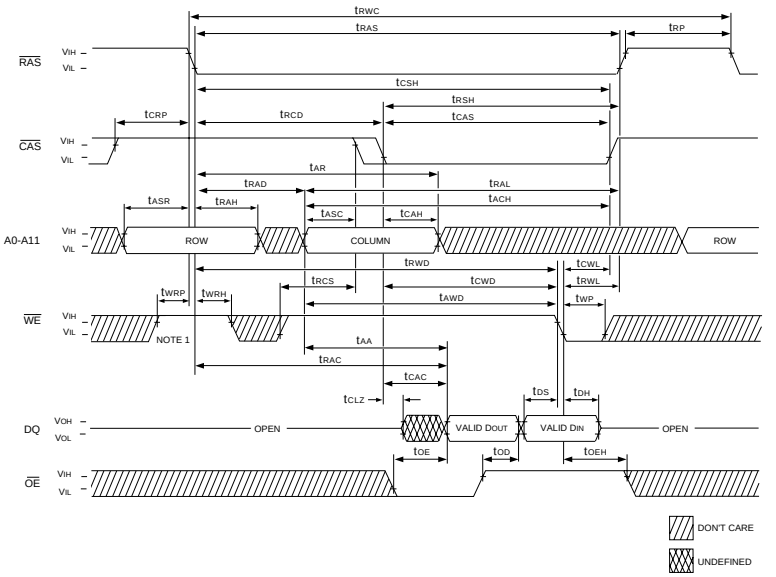


NOTES: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{WE}$ high for t_{WRP} and t_{WRH}.
2. t_{OFF} is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

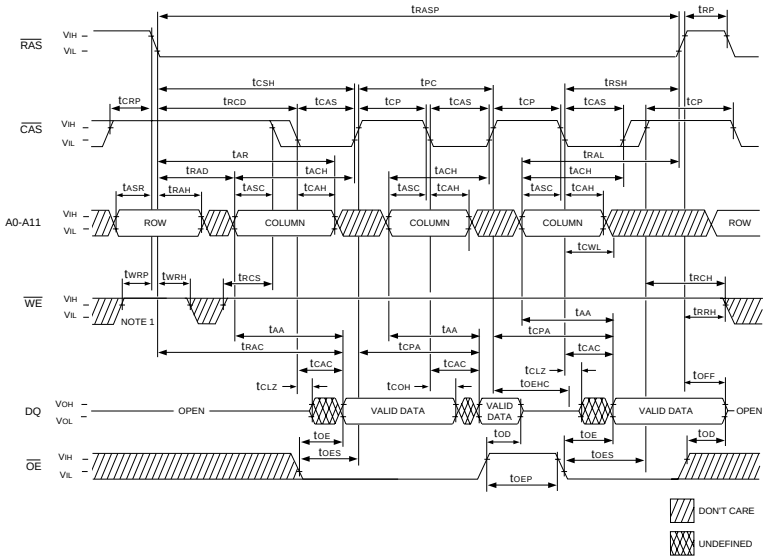
WRITE CYCLE, EARLY WRITE



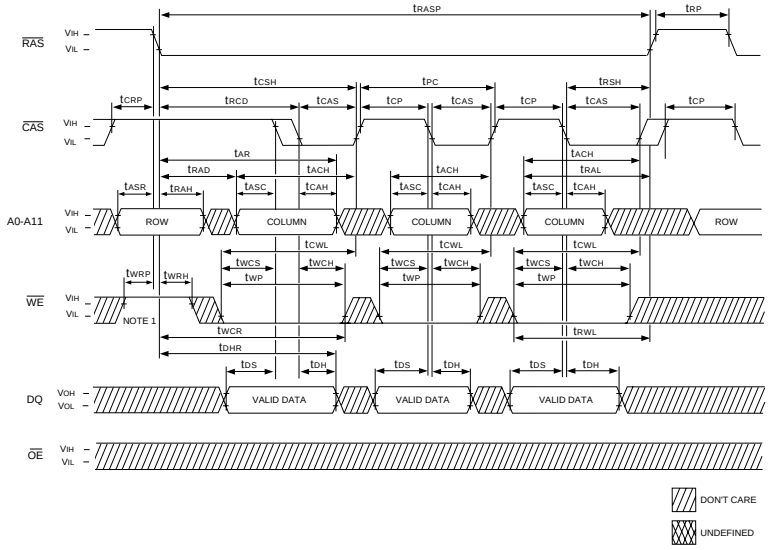
READ WRITE CYCLE
(Late Write and Read-Modify-Write Cycles)



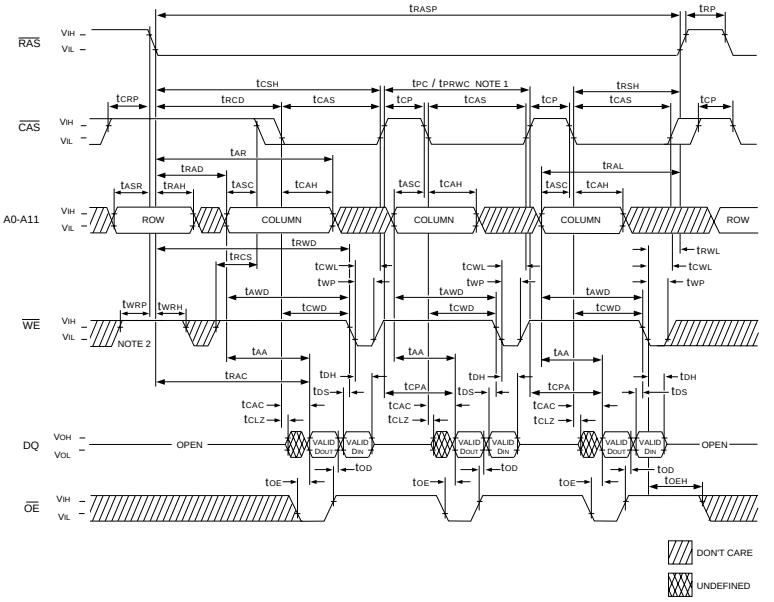
EDO-PAGE-MODE READ CYCLE



EDO-PAGE-MODE EARLY WRITE CYCLE

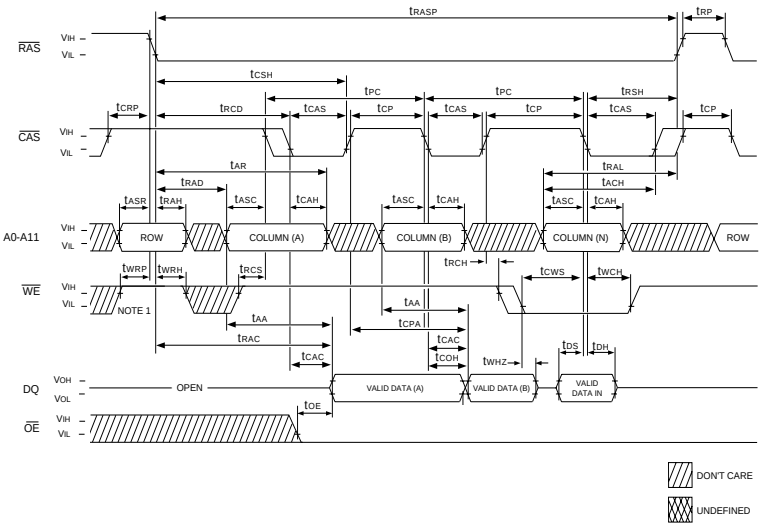


EDO-PAGE-MODE READ-WRITE CYCLE

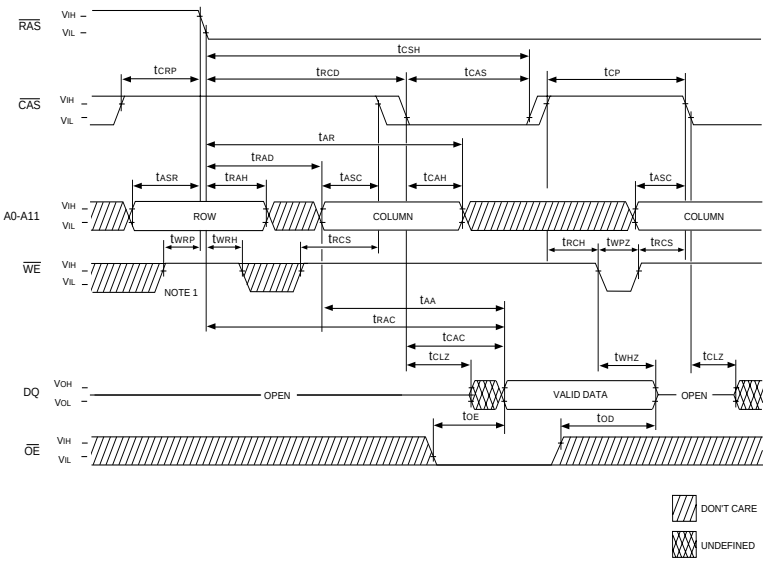


NOTE: 1. TPC is for Late Write Cycles Only

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE

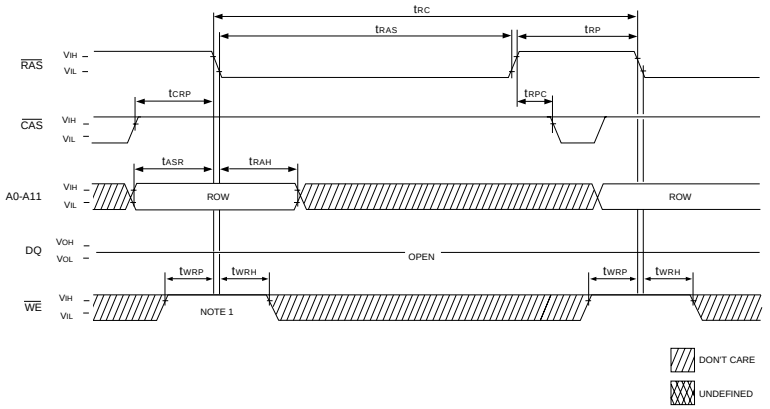


READ CYCLE WITH $\overline{WE}$ CONTROLLED DISABLE



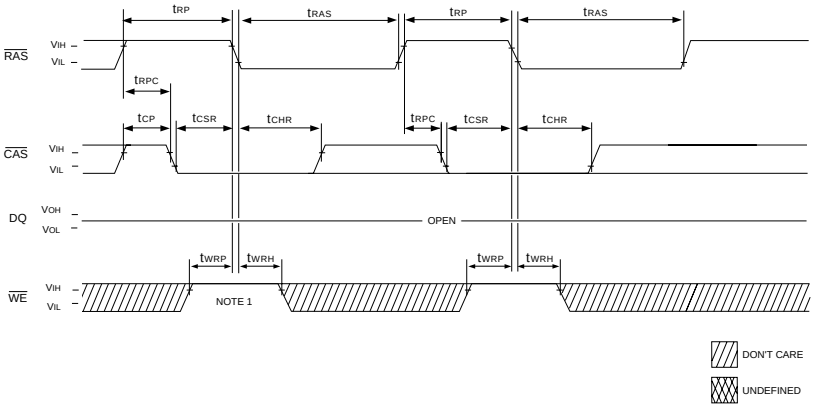
RAS - ONLY REFRESH CYCLE

($\overline{WE}$ and $\overline{OE}$=Don't Care)



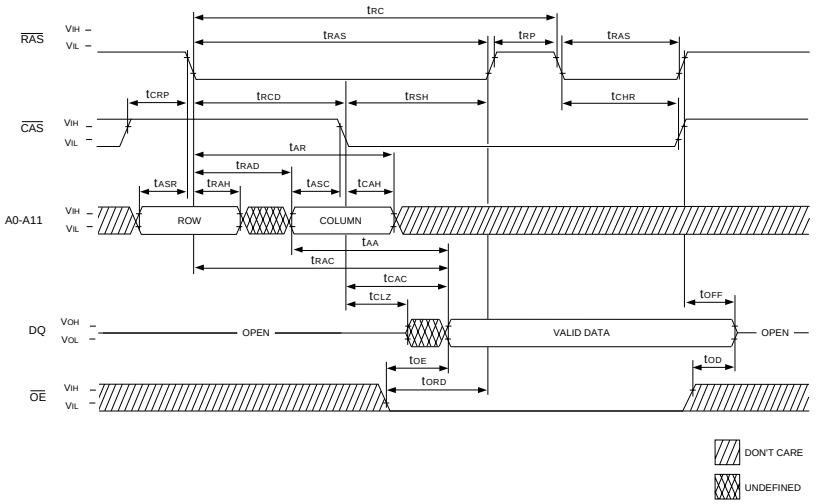
CBR REFRESH CYCLE

(A0-A11 and $\overline{OE}$=Don't Care)



HIDDEN REFRESH CYCLE

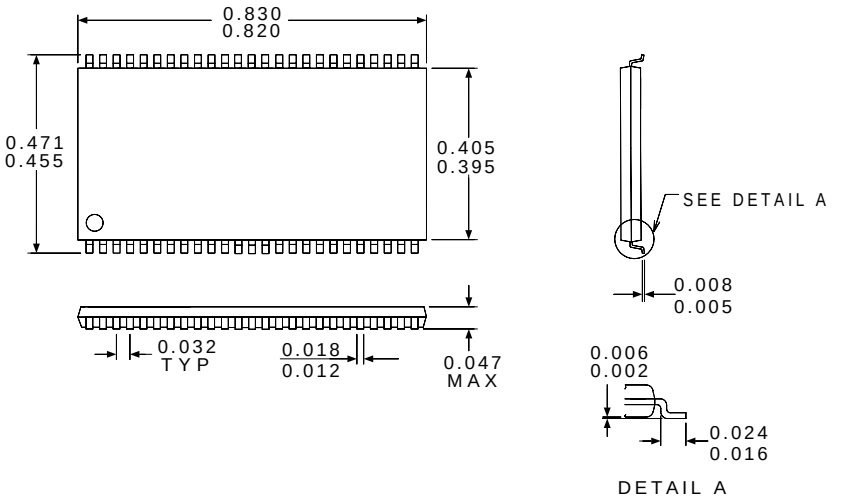
($\overline{WE}$=High, $\overline{OE}$=Low) NOTE 1



NOTE: 1. A hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{WE}$ = Low and $\overline{OE}$ = High

PACKAGE DESCRIPTION

50 PIN PLASTIC TSOP
PACKAGE NO. 372



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

MILITARY (-55 °C TO +125 °C)

Part No.	Speed (ns)	Package No.
EDI4164MEV50SM	50	372
EDI4164MEV60SM	60	372
EDI4164MEV70SM	70	372

INDUSTRIAL (-40 °C TO +85 °C)

Part No.	Speed (ns)	Package No.
EDI4164MEV50SI	50	372
EDI4164MEV60SI	60	372
EDI4164MEV70SI	70	372