

## Module Features

- 4x128Kx64 Synchronous
- Flow-Through Architecture
- Clock Controlled Registered Bank Enables (E1\, E2\, E3, E4\)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW\)
- Aysnchronous Output Enable (G\)
- Internally self-timed Write
- Module Sleep Mode enable (ZZ)
- Gold Lead Finish
- 3.3V  $\pm 10\%$  Operation
- Access Speed(s): TKHQV=9.5, 10, 11, 12, 15ns
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single total array Clock
- Multiple Vcc and Gnd

## 4x128Kx64, 3.3V

### Synchronous Flow-Through

The EDI2KG64128VxxD is a Synchronous SRAM, 60 position Card Edge DIMM (120 contacts) Module, organized as 4x128Kx64. The Module contains eight (8) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Synchronous Only, Flow-Through, Early Write Device. This module provides High Performance, Ultra Fast access times at a cost per bit benefit over BiCMOS Asynchronous SRAM based devices. As well as improved cost per bit, the use of Synchronous or Synchronous Burst devices or modules can ease the memory subsystem design by reducing or easing the memory controller requirement.

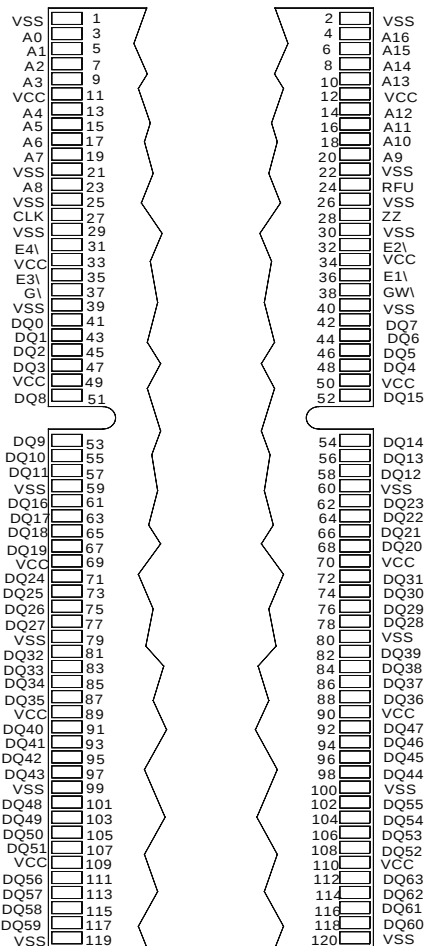
Synchronous operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. All read and write operations to this module are performed on Quad Words (64 bit operations).

Write cycles are internally self timed and are initiated by a rising clock edge. This feature relieves the designer the task of developing external write pulse width circuitry.

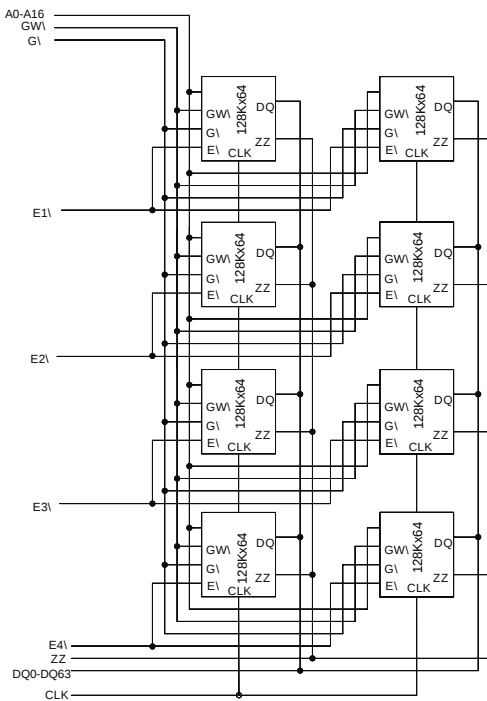
## Pin Names

|                    |                                 |
|--------------------|---------------------------------|
| DQ0-DQ63           | Input/Output Bus                |
| A0-A15             | Address Bus                     |
| E1\, E2\, E3\, E4\ | Synchronous Bank Enables        |
| Clk                | Array Clock                     |
| GW\                | Synchronous Global write Enable |
| G\                 | Asynchronous Output Enable      |
| ZZ                 | Module Sleep Enable             |
| Vcc                | 3.3V Power Supply               |
| Vss                | Gnd                             |

## Pin Configuration



## Functional Block Diagram



**EDI2KG464128V**  
**4 Megabyte Synchronous**  
**Card Edge DIMM**

### Pin Descriptions

| DIMM Pins                                                     | Symbol             | Type                  | Description                                                                                                                                                                                                           |
|---------------------------------------------------------------|--------------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3, 5, 7, 9, 15, 17,<br>19, 23, 20, 18, 16,<br>14, 10, 8, 6, 4 | A0-A16             | Input<br>Synchronous  | Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycle.   |
| 38                                                            | GW                 | Input<br>Synchronous  | Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE\ and BW\ lines and must meet the setup and hold times around the rising edge of CLK.                                   |
| 27                                                            | CLK                | Input<br>Synchronous  | Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.      |
| 36, 32,<br>—                                                  | E1\, E2\<br>35, 31 | Input<br>Synchronous  | Bank Enables: These active LOW inputs are used to enable each individual bank and to gate ADSP.                                                                                                                       |
| 37                                                            | G\                 | Input                 | Output Enable: This active LOW asynchronous input enables the data output drivers.                                                                                                                                    |
|                                                               | ZZ                 | Input<br>Asynchronous | Module Snooze: This active high signal places the memory module in sleep mode (low power consumption).                                                                                                                |
| Various                                                       | DQ0-63             | Input/Output          | Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is DQ40-47, seventh byte is DQ48-55 and the eighth byte is DQ56-64. |
| Various                                                       | Vcc                | Supply                | Core power supply: +3.3V -5%/+10%                                                                                                                                                                                     |
| Various                                                       | Vss                | Ground                | Ground                                                                                                                                                                                                                |

### Synchronous Only - Truth Table

| Operation                | E1\ | E2\ | E3\ | E4\ | GW\ | G\ | ZZ | CLK | DQ     |
|--------------------------|-----|-----|-----|-----|-----|----|----|-----|--------|
| Synchronous Write-Bank 1 | L   | H   | H   | H   | L   | H  | L  | ↑   | High-Z |
| Synchronous Read-Bank 1  | L   | H   | H   | H   | H   | L  | L  | ↑   |        |
| Synchronous Write-Bank 2 | H   | L   | H   | H   | L   | H  | L  | ↑   | High-Z |
| Synchronous Read-Bank 2  | H   | L   | H   | H   | H   | L  | L  | ↑   |        |
| Synchronous Write-Bank 3 | H   | H   | L   | H   | L   | H  | L  | ↑   | High-Z |
| Synchronous Read-Bank 3  | H   | H   | L   | H   | H   | L  | L  | ↑   |        |
| Synchronous Write-Bank 4 | H   | H   | H   | L   | L   | H  | L  | ↑   | High-Z |
| Synchronous Read-Bank 4  | H   | H   | H   | L   | H   | L  | L  | ↑   |        |
| Snooze Mode              | X   | X   | X   | X   | X   | X  | H  | X   | High-Z |

### Absolute Maximum Ratings\*

|                                    |                    |
|------------------------------------|--------------------|
| Voltage on Vcc Relative to Vss     | -0.5V to +4.6V     |
| Vin                                | -0.5V to Vcc +0.5V |
| Storage Temperature                | -55°C to +125°C    |
| Operating Temperature (Commercial) | 0°C to +70°C       |
| Operating Temperature (Industrial) | -40°C to +85°C     |
| Short Circuit Output Current       | 10 mA              |

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### AC Test Conditions

|                              |             |
|------------------------------|-------------|
| Input Pulse Levels           | Vss to 3.0V |
| Input and Output Timing Ref. | 1.25V       |
| Output Test equivalencies    |             |

### AC Test Load

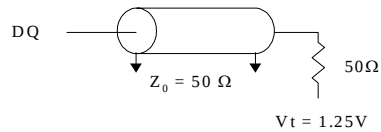


Fig. 1 Output Load Equivalent

### Recommended DC Operating Conditions

| Parameter      | Sym | Min  | Typ | Max     | Units   |
|----------------|-----|------|-----|---------|---------|
| Supply Voltage | VCC | 3.14 | 3.3 | 3.6     | V       |
| Supply Voltage | VSS | 0.0  | 0.0 | 0.0     | V       |
| Input High     | VIH | 1.1  | 3.0 | VCC+0.3 | V       |
| Input Low      | VIL | -0.3 | 0.0 | 0.3     | V       |
| Input Leakage  | ILi | -2   | 1   | 2       | $\mu A$ |
| Output Leakage | ILO | -2   | 1   | 2       | $\mu A$ |

### DC Electrical Characteristics - Read Cycle

| Description                   | SYM   | Typ  | Max |     |     |     |     | Units |
|-------------------------------|-------|------|-----|-----|-----|-----|-----|-------|
|                               |       |      | 9.5 | 10  | 11  | 12  | 15  |       |
| Power Supply Current          | lcc1  | 1.55 | 2.8 | 2.2 | 2.2 | 2.7 | 2.0 | A     |
| Power Supply Current          | lcc   | .750 | 1.8 | 1.5 | 1.3 | 1.3 | 1.0 | A     |
| Device Selected, No Operation |       |      |     |     |     |     |     |       |
| Snooze Mode                   | lccZZ | 200  | 300 | 300 | 300 | 300 | 300 | mA    |
| CMOS Standby                  | lcc3  | 400  | 500 | 500 | 500 | 500 | 500 | mA    |
| Clock Running-Deselect        | lccK  | 600  | 900 | 900 | 900 | 900 | 900 | mA    |

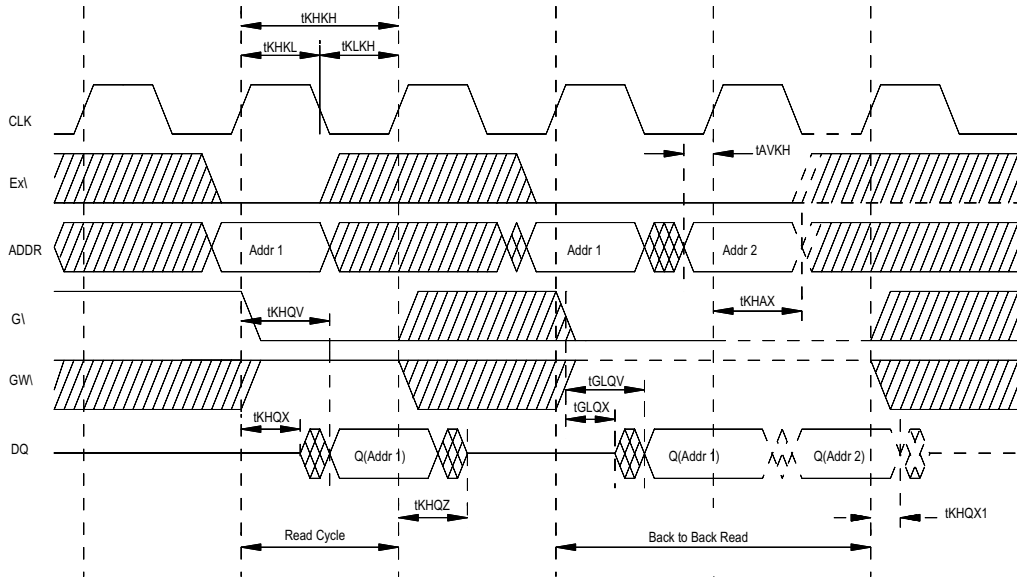
### Read Cycle Timing Parameters

| Description                    | Sym    | 9.5ns |     | 10ns |     | 11ns |     | 12ns |     | 15ns |     | Units |
|--------------------------------|--------|-------|-----|------|-----|------|-----|------|-----|------|-----|-------|
|                                |        | Min   | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |       |
| Clock Cycle Time               | tKhKh  | *     | *   | 12   |     | 13   |     | 15   |     | 20   |     | ns    |
| Clock High Time                | tKHKL  | *     | *   | 5    |     | 5    |     | 5    |     | 6    |     | ns    |
| Clock Low Time                 | tKLKH  | *     | *   | 5    |     | 5    |     | 5    |     | 6    |     | ns    |
| Clock to Output Valid          | tKHQV  | *     | *   |      | 10  |      | 11  |      | 12  |      | 15  | ns    |
| Clock to Output Invalid        | tKHQX1 | *     | *   | 3    |     | 3    |     | 3    |     | 3    |     | ns    |
| Clock to Output Low-Z          | tKHQX  | *     | *   | 2    |     | 2    |     | 2    |     | 2    |     | ns    |
| Output Enable to Output Valid  | tGLQV  | *     | *   |      | 4   |      | 5   |      | 5   |      | 6   | ns    |
| Output Enable to Output Low-Z  | tGLQX  | *     | *   | 0    |     | 0    |     | 0    |     | 0    |     | ns    |
| Output Enable to Output High-Z | tGHQZ  | *     | *   |      | 4   |      | 5   |      | 5   |      | 5   | ns    |
| Address Setup                  | tAVKH  | *     | *   | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | ns    |
| Bank Enable Setup              | tEVKH  | *     | *   | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | ns    |
| Address Hold                   | tKHAX  | *     | *   | 1.0  |     | 1.0  |     | 1.0  |     | 1.0  |     | ns    |
| Bank Enable Hold               | tKHEX  | *     | *   | 1.0  |     | 1.0  |     | 1.0  |     | 1.0  |     | ns    |

\*TBD

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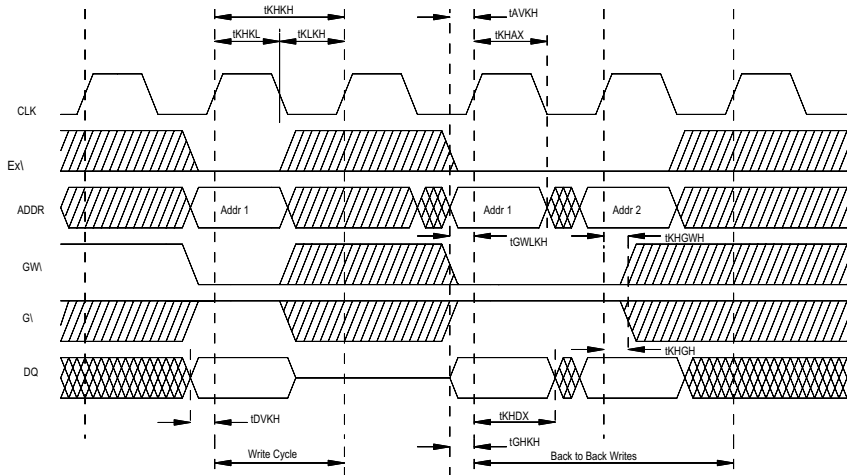
### Synchronous Read Cycle



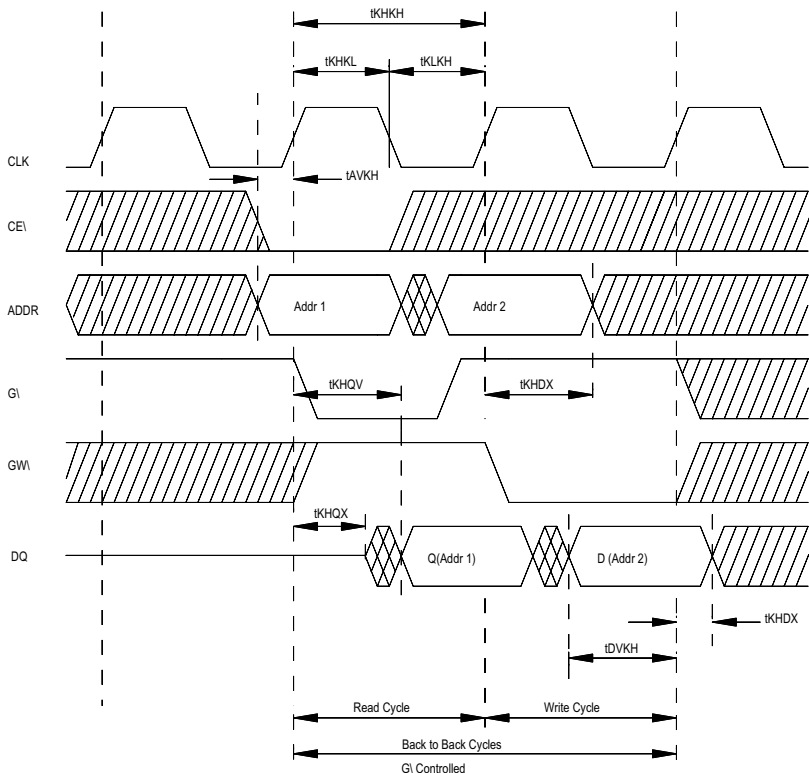
### Write Cycle Timing Parameters

| Description               | Sym   | 9.5ns |     | 10ns |     | 11ns |     | 12ns |     | 15ns |     | Units |
|---------------------------|-------|-------|-----|------|-----|------|-----|------|-----|------|-----|-------|
|                           |       | Min   | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |       |
| Clock Cycle Time          | tKHKH | *     | *   | 12   |     | 13   |     | 15   |     | 20   |     | ns    |
| Clock High Time           | tKHKL | *     | *   | 5    |     | 5    |     | 5    |     | 6    |     | ns    |
| Clock Low Time            | tKLKH | *     | *   | 5    |     | 5    |     | 5    |     | 6    |     | ns    |
| Address Setup             | tAVKH | *     | *   | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | ns    |
| Address Hold              | tKHAX | *     | *   | 1.0  |     | 1.0  |     | 1.0  |     | 1.0  |     | ns    |
| Bank Enable Setup         | tEVKH | *     | *   | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | ns    |
| Bank Enable Hold          | tKHEX | *     | *   | 1.0  |     | 1.0  |     | 1.0  |     | 1.0  |     | ns    |
| Global Write Enable Setup | tWVKH | *     | *   | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | ns    |
| Global Write Enable Hold  | tKHWX | *     | *   | 1.0  |     | 1.0  |     | 1.0  |     | 1.0  |     | ns    |
| Data Setup                | tDVKH | *     | *   | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | ns    |
| Data Hold                 | tKHDX | *     | *   | 1.0  |     | 1.0  |     | 1.0  |     | 1.0  |     | ns    |

## Sync Write Cycle



## Sync Read/Write Cycle



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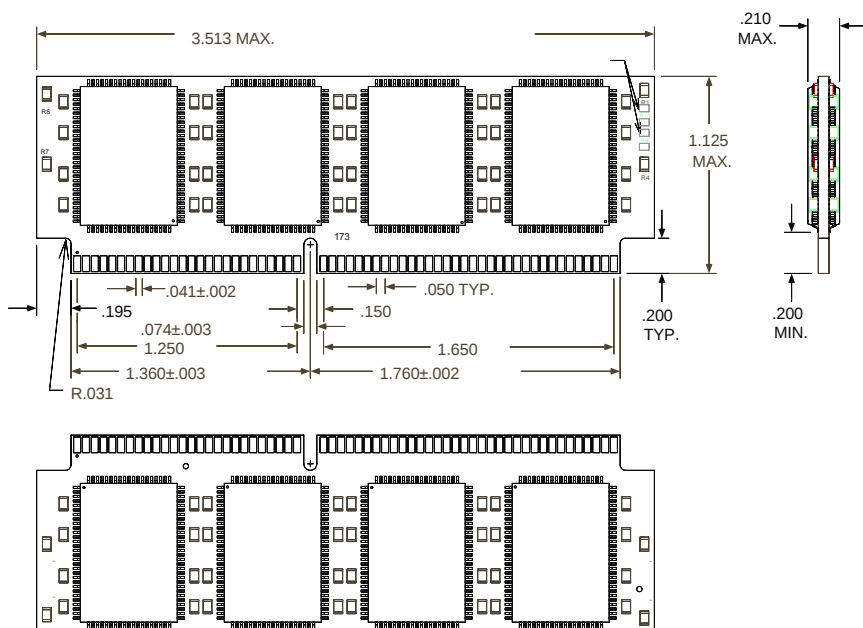
### Ordering Information

| Part Number       | Organization | Voltage | Speed (ns) | Package            |
|-------------------|--------------|---------|------------|--------------------|
| EDI2KG464128V95D* | 4x128Kx64    | 3.3     | 9.5        | 120 Card Edge DIMM |
| EDI2KG464128V10D* | 4x128Kx64    | 3.3     | 10         | 120 Card Edge DIMM |
| EDI2KG464128V11D  | 4x128Kx64    | 3.3     | 11         | 120 Card Edge DIMM |
| EDI2KG464128V12D  | 4x128Kx64    | 3.3     | 12         | 120 Card Edge DIMM |
| EDI2KG464128V15D* | 4x128Kx64    | 3.3     | 15         | 120 Card Edge DIMM |

\*Consult Factory for Availability

### Package Description

#### 120 Lead Card Edge DIMM



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