



## 2x128Kx72, 3.3V Sync/Sync Burst Flow-Through

### FEATURES

- 2x128Kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Linear and Sequential Burst Support via MODE pin
- Access Speed(s):  $T_{KHQV} = 8.5, 9, 12, 15\text{ns}$
- Clock Controlled Registered Bank Enables ( $\overline{E}_1, \overline{E}_2$ )
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write ( $\overline{GW}$ )
- Asynchronous Output Enable ( $\overline{G}$ )
- Internally Self-timed Write
- Individual Bank Sleep Mode Enables ( $ZZ_1, ZZ_2$ )
- Gold Lead Finish
- 3.3V  $\pm 10\%$  Operation
- Common Data I/O
- High Capacitance (30pF) Drive, at Rated Access Speed
- Single Total Array Clock
- Multiple Vcc and Gnd

The EDI2CG272128VxxD1 is a Synchronous/Synchronous Burst SRAM, 72 position DIMM (144 contacts) Module, small outline. The Module contains four (4) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sync Burst, Flow-Through, with support for either linear or sequential burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS asynchronous device architectures.

Synchronous Only operations are performed via strapping  $\overline{ADSC}$  Low, and  $\overline{ADSP} / \overline{ADV}$  High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined for Quad Word access in both read and write operations.



## PIN CONFIGURATION

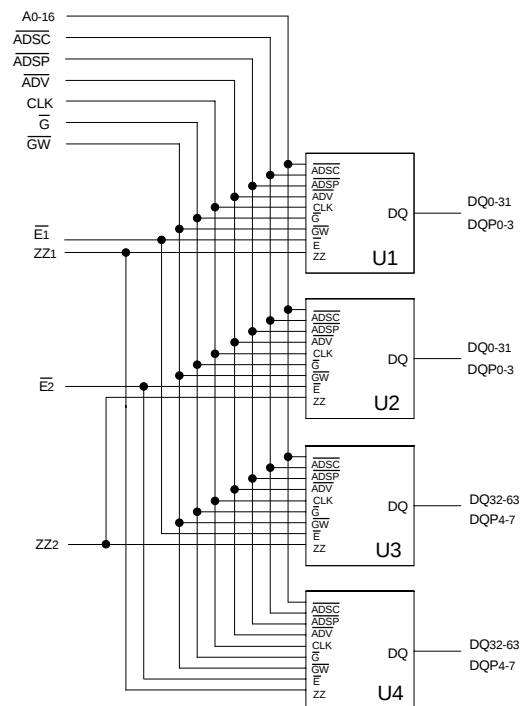
### PIN SYMBOLS

| PIN | FUNCTION     | PIN | FUNCTION   | PIN | FUNCTION | PIN | FUNCTION |
|-----|--------------|-----|------------|-----|----------|-----|----------|
| 1   | VSS          | 37  | DQ0        | 73  | VSS      | 109 | DQ41     |
| 2   | VSS          | 38  | DQ7        | 74  | VSS      | 110 | DQ46     |
| 3   | A0           | 39  | DQ1        | 75  | ZZ2      | 111 | DQ42     |
| 4   | RFU          | 40  | DQ6        | 76  | DQP3     | 112 | DQ45     |
| 5   | A16          | 41  | DQ2        | 77  | VCC      | 113 | DQ43     |
| 6   | A1           | 42  | DQ5        | 78  | VCC      | 114 | DQ44     |
| 7   | A2           | 43  | DQ3        | 79  | DQ24     | 115 | VSS      |
| 8   | A15          | 44  | DQ4        | 80  | DQ31     | 116 | VSS      |
| 9   | A14          | 45  | VSS        | 81  | DQ25     | 117 | RFU      |
| 10  | A3           | 46  | VSS        | 82  | DQ30     | 118 | DQP6     |
| 11  | A4           | 47  | ZZ1        | 83  | DQ26     | 119 | VCC      |
| 12  | A13          | 48  | DQP1       | 84  | DQ29     | 120 | VCC      |
| 13  | A12          | 49  | VCC        | 85  | DQ27     | 121 | DQ48     |
| 14  | A5           | 50  | VCC        | 86  | DQ28     | 122 | DQ55     |
| 15  | A6           | 51  | DQ8        | 87  | VSS      | 123 | DQ49     |
| 16  | A11          | 52  | DQ15       | 88  | VSS      | 124 | DQ54     |
| 17  | A10          | 53  | DQ9        | 89  | RFU      | 125 | DQ50     |
| 18  | A7           | 54  | DQ14       | 90  | DQP4     | 126 | DQ53     |
| 19  | A8           | 55  | DQ10       | 91  | VCC      | 127 | DQ51     |
| 20  | A9           | 56  | DQ13       | 92  | VCC      | 128 | DQ52     |
| 21  | VCC          | 57  | DQ11       | 93  | DQ32     | 129 | VSS      |
| 22  | VCC          | 58  | DQ12       | 94  | DQ39     | 130 | VSS      |
| 23  | $\bar{G}$    | 59  | VSS        | 95  | DQ33     | 131 | RFU      |
| 24  | RFU          | 60  | VSS        | 96  | DQ38     | 132 | DQP7     |
| 25  | $\bar{G}W$   | 61  | $\bar{E}2$ | 97  | DQ34     | 133 | VCC      |
| 26  | $\bar{A}DV$  | 62  | DQP2       | 98  | DQ37     | 134 | VCC      |
| 27  | $\bar{A}DSP$ | 63  | VCC        | 99  | DQ35     | 135 | DQ56     |
| 28  | $\bar{A}DSC$ | 64  | VCC        | 100 | DQ36     | 136 | DQ63     |
| 29  | MODE         | 65  | DQ16       | 101 | VSS      | 137 | DQ57     |
| 30  | CLK          | 66  | DQ23       | 102 | VSS      | 138 | DQ62     |
| 31  | VSS          | 67  | DQ17       | 103 | RFU      | 139 | DQ58     |
| 32  | VSS          | 68  | DQ22       | 104 | DQP5     | 140 | DQ61     |
| 33  | $\bar{E}1$   | 69  | DQ18       | 105 | VCC      | 141 | DQ59     |
| 34  | DQP0         | 70  | DQ21       | 106 | VCC      | 142 | DQ60     |
| 35  | VCC          | 71  | DQ19       | 107 | DQ40     | 143 | VSS      |
| 36  | VCC          | 72  | DQ20       | 108 | DQ47     | 144 | VSS      |

### PIN NAMES

|                      |                                 |
|----------------------|---------------------------------|
| DQ0-63               | Input/Output Bus                |
| DQP0-7               | Parity Bits                     |
| A0-16                | Address Bus                     |
| $\bar{E}1, \bar{E}2$ | Synchronous Bank Enables        |
| CLK                  | Array Clock                     |
| $\bar{G}W$           | Synchronous Global Write Enable |
| $\bar{G}$            | Asynchronous Output Enable      |
| ZZ1, ZZ2             | Blank Sleep Mode Enables        |
| Vcc                  | 3.3V Power Supply               |
| Vss                  | Ground                          |
| NC                   | No Connect                      |

FIG. 1 FUNCTIONAL BLOCK DIAGRAM




**PIN DESCRIPTIONS**

| DIMM Pins                                                    | Symbol                         | Type               | Description                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------------------------------------------------------------|--------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3, 6, 10, 11, 14, 15, 18, 19, 20, 17, 16, 13, 12, 9, 8, 3, 5 | A0-16                          | Input Synchronous  | Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycle.                                                                                                                                                                                                   |
| 25                                                           | $\overline{GW}$                | Input Synchronous  | Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWx}$ lines and must meet the setup and hold times around the rising edge of CLK.                                                                                                                                                                                                          |
| 30                                                           | CLK                            | Input Synchronous  | Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.                                                                                                                                                                                                      |
| 33, 61                                                       | $\overline{E1}, \overline{E2}$ | Input Synchronous  | Bank Enables: These active LOW inputs are used to enable each individual bank and to gate $\overline{ADSP}$                                                                                                                                                                                                                                                                                                           |
| 23                                                           | $\overline{G}$                 | Input              | Output Enable: This active LOW asynchronous input enables the data output drivers.                                                                                                                                                                                                                                                                                                                                    |
| 26                                                           | $\overline{ADV}$               | Input Synchronous  | Address Status Processor: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).                                                                                                                                                                                                                                                          |
| 27                                                           | $\overline{ADSP}$              | Input Synchronous  | Address Status Processor: This active LOW input, along with $\overline{EL}$ and $\overline{EH}$ being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.                                                                                                                                                                                                        |
| 28                                                           | $\overline{ADSC}$              | Input Synchronous  | Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.                                                                                                                                                                                                |
| 29                                                           | MODE                           | Input Static       | Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.                                                                                                                                                                                                                                                                              |
| 47, 75                                                       | ZZ1, ZZ2                       | Input Asynchronous | Snooze: These active HIGH inputs put the individual banks in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (no connect).                                                                                                                                                                                                                                            |
| Various                                                      | DQ0-63                         | Input/Output       | Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is DQ40-47, seventh byte is DQ48-55 and the eighth byte is DQ56-64.                                                                                                                                                                                                 |
| 34, 48, 62, 76, 90, 104, 118, 132                            | DQP0-7                         | Input/Output       | Parity Inputs/Outputs: DQP0 is parity bit for DQ0-7. DQP1 is parity bit for DQ8-15. DQP2 is parity bit for DQ16-23. DQP3 is parity bit for DQ24-31. DQP4 is parity bit for DQ32-39. DQP5 is parity bit for DQ40-47. DQP6 is parity bit for DQ48-55. DQP7 is parity bit for DQ56-64 and DQP7. In order to use the device configured as a 128K x 64, the parity bits need to be tied to Vss through a 10K ohm resistor. |
| Various                                                      | Vcc                            | Supply             | Core power supply: +3.3V -5%/+10%                                                                                                                                                                                                                                                                                                                                                                                     |
| Various                                                      | Vss                            | Ground             | Ground                                                                                                                                                                                                                                                                                                                                                                                                                |


**SYNCHRONOUS BURST - TRUTH TABLE**

| Operation                            | $\overline{E1}$ | $\overline{E2}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{GW}$ | $\overline{G}$ | CLK | DQ     | Addr. Used |
|--------------------------------------|-----------------|-----------------|-------------------|-------------------|------------------|-----------------|----------------|-----|--------|------------|
| Deselected Cycle, Power Down; Bank 1 | H               | X               | X                 | L                 | X                | X               | X              | L-H | High-Z | None       |
| Deselected Cycle, Power Down; Bank 2 | X               | H               | X                 | L                 | X                | X               | X              | L-H | High-Z | None       |
| Read Cycle, Begin Burst; Bank 1      | L               | H               | L                 | X                 | X                | X               | L              | L-H | Q      | External   |
| Read Cycle, Begin Burst; Bank 1      | L               | H               | L                 | X                 | X                | X               | H              | L-H | High-Z | External   |
| Read Cycle, Begin Burst; Bank 2      | H               | L               | L                 | X                 | X                | X               | L              | L-H | Q      | External   |
| Read Cycle, Begin Burst; Bank 2      | H               | L               | L                 | X                 | X                | X               | H              | L-H | High-Z | External   |
| Write Cycle, Begin Burst; Bank 1     | L               | H               | H                 | L                 | X                | L               | X              | L-H | D      | External   |
| Write Cycle, Begin Burst; Bank 2     | H               | L               | H                 | L                 | X                | L               | X              | L-H | D      | External   |
| Read Cycle, Begin Burst; Bank 1      | L               | H               | H                 | L                 | X                | H               | L              | L-H | Q      | External   |
| Read Cycle, Begin Burst; Bank 1      | L               | H               | H                 | L                 | X                | H               | H              | L-H | High-Z | External   |
| Read Cycle, Begin Burst; Bank 2      | H               | L               | H                 | L                 | X                | H               | L              | L-H | Q      | External   |
| Read Cycle, Begin Burst; Bank 2      | H               | L               | H                 | L                 | X                | H               | H              | L-H | High-Z | External   |
| Read Cycle, Continue Burst; Bank 1   | X               | H               | X                 | H                 | L                | H               | L              | L-H | Q      | Next       |
| Read Cycle, Continue Burst; Bank 1   | X               | H               | X                 | H                 | L                | H               | H              | L-H | High-Z | Next       |
| Read Cycle, Continue Burst; Bank 2   | H               | X               | X                 | H                 | L                | H               | L              | L-H | Q      | Next       |
| Read Cycle, Continue Burst; Bank 2   | H               | X               | X                 | H                 | L                | H               | H              | L-H | High-Z | Next       |
| Read Cycle, Continue Burst; Bank 1   | H               | H               | X                 | H                 | L                | H               | L              | L-H | Q      | Next       |
| Read Cycle, Continue Burst; Bank 1   | H               | H               | X                 | H                 | L                | H               | H              | L-H | High-Z | Next       |
| Read Cycle, Continue Burst; Bank 2   | H               | H               | X                 | H                 | L                | H               | L              | L-H | Q      | Next       |
| Read Cycle, Continue Burst; Bank 2   | H               | H               | X                 | H                 | L                | H               | H              | L-H | High-Z | Next       |
| Write Cycle, Continue Burst; Bank 1  | X               | H               | H                 | H                 | L                | L               | X              | L-H | D      | Next       |
| Write Cycle, Continue Burst; Bank 1  | H               | H               | X                 | H                 | L                | L               | X              | L-H | D      | Next       |
| Write Cycle, Continue Burst; Bank 2  | H               | X               | H                 | H                 | L                | L               | X              | L-H | D      | Next       |
| Write Cycle, Continue Burst; Bank 2  | H               | H               | X                 | H                 | L                | L               | X              | L-H | D      | Next       |
| Read Cycle, Suspend Burst; Bank 1    | X               | H               | H                 | H                 | H                | H               | L              | L-H | Q      | Current    |
| Read Cycle, Suspend Burst; Bank 1    | X               | H               | H                 | H                 | H                | H               | H              | L-H | High-Z | Current    |
| Read Cycle, Suspend Burst; Bank 2    | H               | X               | H                 | H                 | H                | H               | L              | L-H | Q      | Current    |
| Read Cycle, Suspend Burst; Bank 2    | H               | X               | H                 | H                 | H                | H               | H              | L-H | High-Z | Current    |
| Read Cycle, Suspend Burst; Bank 1    | H               | H               | X                 | H                 | H                | H               | L              | L-H | Q      | Current    |
| Read Cycle, Suspend Burst; Bank 1    | H               | H               | X                 | H                 | H                | H               | H              | L-H | High-Z | Current    |
| Read Cycle, Suspend Burst; Bank 2    | H               | H               | X                 | H                 | H                | H               | L              | L-H | Q      | Current    |
| Read Cycle, Suspend Burst; Bank 2    | H               | H               | X                 | H                 | H                | H               | H              | L-H | High-Z | Current    |
| Write Cycle, Suspend Burst; Bank 1   | X               | H               | H                 | H                 | H                | L               | X              | L-H | D      | Current    |
| Write Cycle, Suspend Burst; Bank 1   | H               | H               | X                 | H                 | H                | L               | X              | L-H | D      | Current    |
| Write Cycle, Suspend Burst; Bank 2   | H               | X               | H                 | H                 | H                | L               | X              | L-H | D      | Current    |
| Write Cycle, Suspend Burst; Bank 2   | H               | H               | X                 | H                 | H                | L               | X              | L-H | D      | Current    |



## SYNCHRONOUS ONLY - TRUTH TABLE

| Operation                | E1 | E2 | GW | G | ZZ | CLK | DQ     |
|--------------------------|----|----|----|---|----|-----|--------|
| Synchronous Write-Bank 1 | L  | H  | L  | H | L  | ↑   | High-Z |
| Synchronous Read-Bank 1  | L  | H  | H  | L | L  | ↑   |        |
| Synchronous Write-Bank 2 | H  | L  | L  | H | L  | ↑   | High-Z |
| Synchronous Read-Bank 2  | H  | L  | H  | L | L  | ↑   |        |
| Synchronous Write-Bank 3 | H  | H  | L  | H | L  | ↑   | High-Z |
| Synchronous Read-Bank 3  | H  | H  | H  | L | L  | ↑   |        |
| Synchronous Write-Bank 4 | H  | H  | L  | H | L  | ↑   | High-Z |
| Synchronous Read-Bank 4  | H  | H  | H  | L | L  | ↑   |        |
| Snooze Mode              | X  | X  | X  | X | H  | X   | High-Z |

## ABSOLUTE MAXIMUM RATINGS\*

|                                    |                    |
|------------------------------------|--------------------|
| Voltage on Vcc Relative to Vss     | -0.5V to +4.6V     |
| Vin                                | -0.5V to Vcc +0.5V |
| Storage Temperature                | -55°C to +125°C    |
| Operating Temperature (Commercial) | 0°C to +70°C       |
| Operating Temperature (Industrial) | -40°C to +85°C     |
| Short Circuit Output Current       | 10 mA              |

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

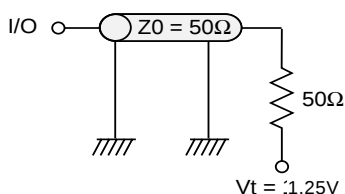
## RECOMMENDED DC OPERATING CONDITIONS

| Parameter      | Sym             | Min  | Typ | Max      | Units |
|----------------|-----------------|------|-----|----------|-------|
| Supply Voltage | Vcc             | 3.14 | 3.3 | 3.6      | V     |
| Supply Voltage | Vss             | 0.0  | 0.0 | 0.0      | V     |
| Input High     | V <sub>IH</sub> | 2.0  | 3.0 | Vcc +0.3 | V     |
| Input Low      | V <sub>IL</sub> | -0.3 | 0.0 | 0.8      | V     |
| Input Leakage  | I <sub>LI</sub> | -2   | 1   | 2        | μA    |
| Output Leakage | I <sub>LO</sub> | -2   | 1   | 2        | μA    |

## DC ELECTRICAL CHARACTERISTICS - READ CYCLE

| Description                                           | Symbol            | Typ  | Max |     |      |      | Units |
|-------------------------------------------------------|-------------------|------|-----|-----|------|------|-------|
|                                                       |                   |      | 8.5 | 9   | 12   | 15   |       |
| Power Supply Current                                  | I <sub>CC1</sub>  | 1.55 | 2.2 | 2.1 | 2.1  | 2.0  | A     |
| Power Supply Current<br>Device Selected, No Operation | I <sub>CC</sub>   | 750  | 1.5 | 1.5 | 1.0  | 1.0  | A     |
| Snooze Mode                                           | I <sub>CCZZ</sub> | 150  | 200 | 200 | 200  | 200  | mA    |
| CMOS Standby                                          | I <sub>CC3</sub>  | 400  | 600 | 600 | 600  | 600  | mA    |
| Clock Running-Deselect                                | I <sub>CCK</sub>  | 600  | 1.0 | 1.0 | 0.75 | 0.75 | A     |

## AC TEST CIRCUIT



## AC TEST CONDITIONS

| Parameter                      | I/O                 | Unit |
|--------------------------------|---------------------|------|
| Input Pulse Levels             | Vss to 3.0          | V    |
| Input and Output Timing Levels | 1.25                | V    |
| Output Test Equivalencies      | See figure, at left |      |

FIG. 2 AC OUTPUT LOAD EQUIVALENT



**BURST ADDRESS TABLE (MODE = NC/V<sub>CC</sub>)**

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| A..A00                   | A..A01                    | A..A10                   | A..A11                    |
| A..A01                   | A..A00                    | A..A11                   | A..A10                    |
| A..A10                   | A..A11                    | A..A00                   | A..A01                    |
| A..A11                   | A..A10                    | A..A01                   | A..A00                    |

**BURST ADDRESS TABLE (MODE = V<sub>SS</sub>)**

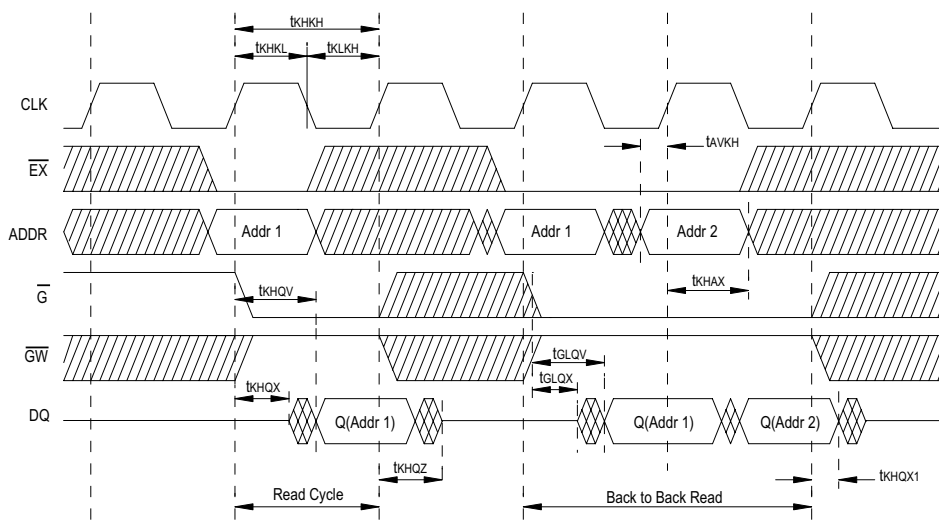
| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| A..A00                   | A..A01                    | A..A10                   | A..A11                    |
| A..A01                   | A..A10                    | A..A11                   | A..A00                    |
| A..A10                   | A..A11                    | A..A00                   | A..A01                    |
| A..A11                   | A..A00                    | A..A01                   | A..A10                    |

**READ CYCLE TIMING PARAMETERS**

| Description                    | Sym                | 8.5ns |     | 9ns |     | 12ns |     | 15ns |     | Units |
|--------------------------------|--------------------|-------|-----|-----|-----|------|-----|------|-----|-------|
|                                |                    | Min   | Max | Min | Max | Min  | Max | Min  | Max |       |
| Clock Cycle Time               | t <sub>KHKH</sub>  | *     | *   | 10  |     | 12   |     | 15   |     | ns    |
| Clock High Time                | t <sub>KHKL</sub>  | *     | *   | 4   |     | 5    |     | 5    |     | ns    |
| Clock Low Time                 | t <sub>KLKH</sub>  | *     | *   | 4   |     | 5    |     | 5    |     | ns    |
| Clock to Output Valid          | t <sub>KHQV</sub>  | *     | *   |     | 9   |      | 10  |      | 12  | ns    |
| Clock to Output Invalid        | t <sub>KHQX1</sub> | *     | *   | 3   |     | 3    |     | 3    |     | ns    |
| Clock to Output Low-Z          | t <sub>KHQX</sub>  | *     | *   | 2   |     | 2    |     | 2    |     | ns    |
| Output Enable to Output Valid  | t <sub>GLQV</sub>  | *     | *   |     | 4   |      | 4   |      | 5   | ns    |
| Output Enable to Output Low-Z  | t <sub>GLQX</sub>  | *     | *   | 0   |     | 0    |     | 0    |     | ns    |
| Output Enable to Output High-Z | t <sub>GHQZ</sub>  | *     | *   |     | 4   |      | 4   |      | 5   | ns    |
| Address Setup                  | t <sub>AVKH</sub>  | *     | *   | 2.5 |     | 2.5  |     | 2.5  |     | ns    |
| Bank Enable Setup              | t <sub>EVKH</sub>  | *     | *   | 2.5 |     | 2.5  |     | 2.5  |     | ns    |
| Address Hold                   | t <sub>KHAX</sub>  | *     | *   | 1.0 |     | 1.0  |     | 1.0  |     | ns    |
| Bank Enable Hold               | t <sub>KHEX</sub>  | *     | *   | 1.0 |     | 1.0  |     | 1.0  |     | ns    |

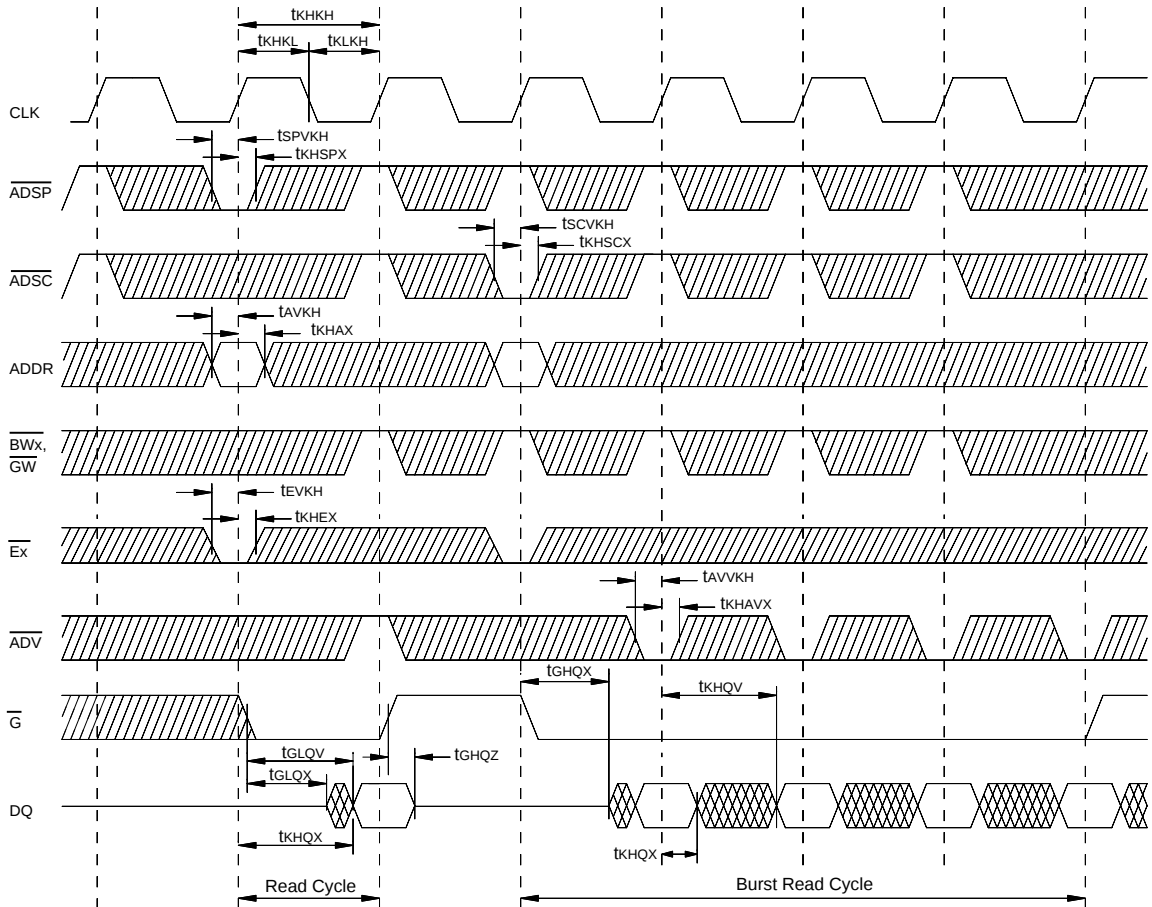
\*TBD

**FIG. 3 SYNCHRONOUS ONLY READ CYCLE**





**FIG. 4 SYNCHRONOUS-BURST READ CYCLE**

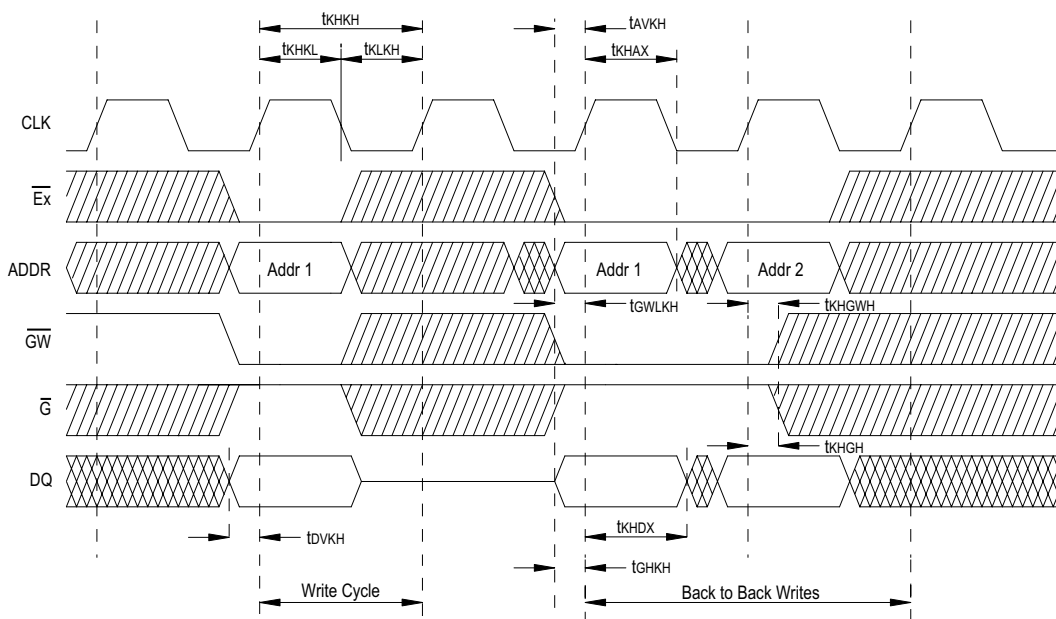




# WRITE CYCLE TIMING PARAMETERS

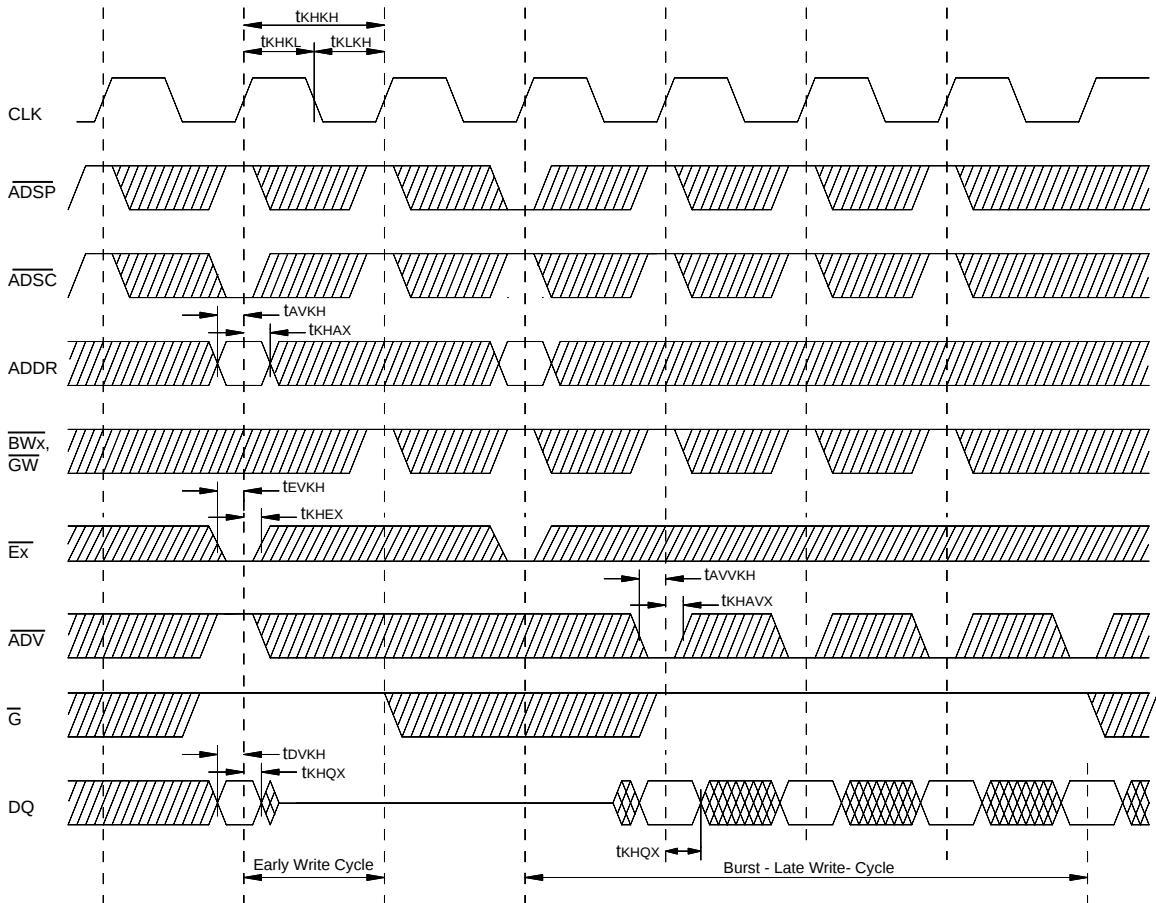
| Description               | Sym   | 8.5ns |     | 9ns |     | 12ns |     | 15ns |     | Units |
|---------------------------|-------|-------|-----|-----|-----|------|-----|------|-----|-------|
|                           |       | Min   | Max | Min | Max | Min  | Max | Min  | Max |       |
| Clock Cycle Time          | tkHKH |       |     | 9   |     | 12   |     | 15   |     | ns    |
| Clock High Time           | tkHKL |       |     | 4   |     | 5    |     | 5    |     | ns    |
| Clock Low Time            | tkLKH |       |     | 4   |     | 5    |     | 5    |     | ns    |
| Address Setup             | tAVKH |       |     | 2.5 |     | 2.5  |     | 2.5  |     | ns    |
| Address Hold              | tkHAX |       |     | 1.0 |     | 1.0  |     | 1.0  |     | ns    |
| Bank Enable Setup         | tEVKH |       |     | 2.5 |     | 2.5  |     | 2.5  |     | ns    |
| Bank Enable Hold          | tkHEX |       |     | 1.0 |     | 1.0  |     | 1.0  |     | ns    |
| Global Write Enable Setup | tWVKH |       |     | 2.5 |     | 2.5  |     | 2.5  |     | ns    |
| Global Write Enable Hold  | tkHWX |       |     | 1.0 |     | 1.0  |     | 1.0  |     | ns    |
| Data Setup                | tDVKH |       |     | 2.5 |     | 2.5  |     | 2.5  |     | ns    |
| Data Hold                 | tkHDX |       |     | 1.0 |     | 1.0  |     | 1.0  |     | ns    |

**FIG. 5 SYNCHRONOUS (NON-BURST) WRITE CYCLE**



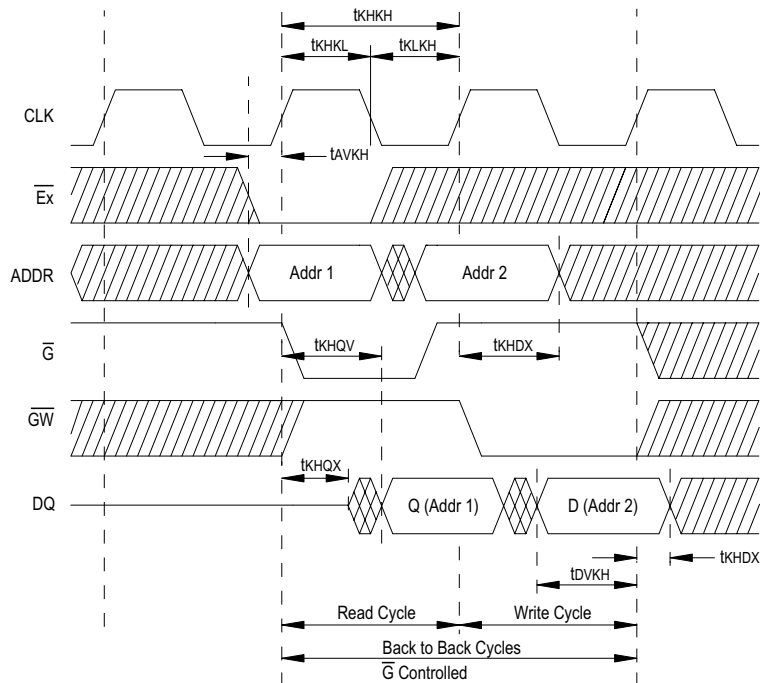


**FIG. 6 SYNCHRONOUS-BURST WRITE CYCLE**





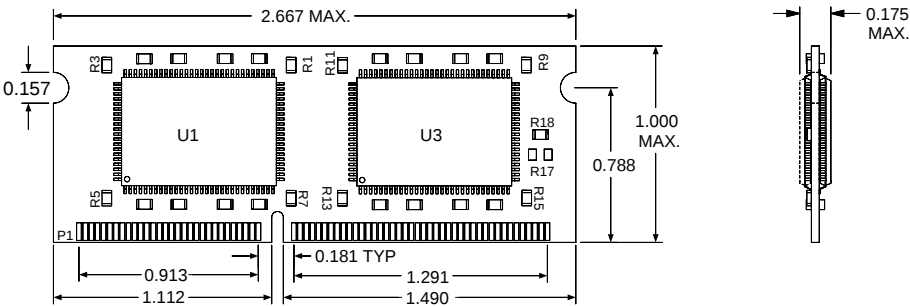
**FIG. 7 SYNCHRONOUS (NON-BURST) READ/WRITE CYCLE**





**PACKAGE DESCRIPTION: 144 LEAD SMALL OUTLINE DIMM**

*Package No. 409*



ALL DIMENSIONS ARE IN INCHES

**ORDERING INFORMATION**

| Part Number        | Organization | Voltage | Speed (ns) | Package                |
|--------------------|--------------|---------|------------|------------------------|
| EDI2CG272128V85D1* | 2x128Kx72    | 3.3     | 8.5        | 144 Small Outline DIMM |
| EDI2CG272128V9D1*  | 2x128Kx72    | 3.3     | 9          | 144 Small Outline DIMM |
| EDI2CG272128V12D1  | 2x128Kx72    | 3.3     | 12         | 144 Small Outline DIMM |
| EDI2CG272128V15D1  | 2x128Kx72    | 3.3     | 15         | 144 Small Outline DIMM |

*\*Consult Factory for Availability*