4Mx8 Bit NAND Flash
CMOS, Monolithic

Features

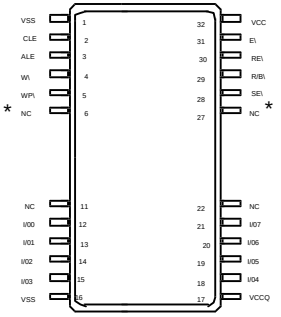
- Single 3.3 - Volt Supply
- Separate Output Buffer power supply (3.3V or 5V)
- Organization
  - Memory Cell array (4M+128K) bit x 8bit
  - Data Register (512 +16) bit x 8 bit
- Automatic Program and Erase
  - Page Program (512 +16) Byte
  - Block Erase (8K +256) Byte
  - Status Register
- 528 - Byte Page Read Operation
  - Random Access 10us
  - Sequential Page Cycle 50ns
  - Sequential Page Access 35ns
- Fast Write cycle Time
  - Program Time 250µs
  - Block Erase Time 5ms
- Command/Addresses/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance: 100K (min) Program/Erase cycles
- Data Retention: 10 years
- Command Register Operation
- 24/32 pin Ceramic Thinpack™ Flatpack No. 347
- 24/32 pin Ceramic Flatpack No. 348

The EDI784MSV is a 4M(4,194,304)x8 bit NAND Flash memory with a spare array of 128K(131,072)x8 bit. Its NAND cell provides the most cost-effective solution for high density nonvolatile memory applications. A program operation programs the 528-byte page in typically 250µs and an erase operation can be performed in typically 5ms on a 8K-byte block. Data in the page can be read out at a 50ns cycle time per byte, with a 35ns access. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase system functions, as well as internal verify and cell margin verify. Each block can be programmed and erased a minimum of one hundred thousand cycles. Write-intensive systems can take advantage of the EDI784MSV's extended reliability up to 1,000,000 program/erase cycles by providing either ECC(Error Checking and Correction) or real time mapping-out algorithm. The spare 16 bytes of a page combined with the 512 bytes of the main array, can be utilized by system-level ECC.

The EDI784MSV is an optimum solution for large nonvolatile storage application such as solid state storage, data/voice recorder, digital maps and other applications requiring ruggedized nonvolatility.

Pin Names

I/OØ-I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{E}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
$\overline{SE}$	Spare area Enable
R/$\overline{B}$	Read/Busy Output
VCC	Power (3.3V)
VCCQ	Output Buffer Power (3.3V/5.0V)
VSS	Ground
NC	No Connection



* Pins 6 & 27 which are no connects on the 4Megx8, become $\overline{RST}$ and $\overline{E2}$ respectively, on the 8Megx8.

Block Diagram

Figure 1. FUNCTIONAL BLOCK DIAGRAM

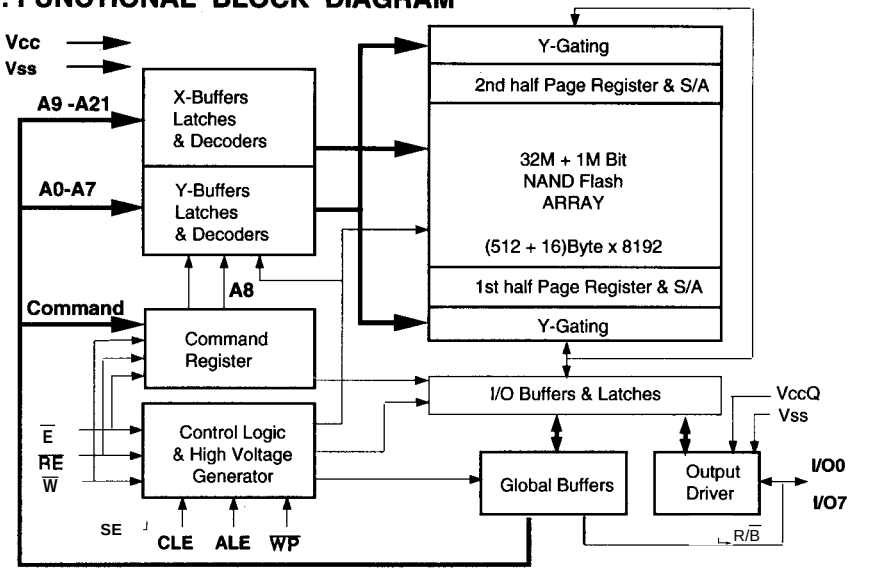
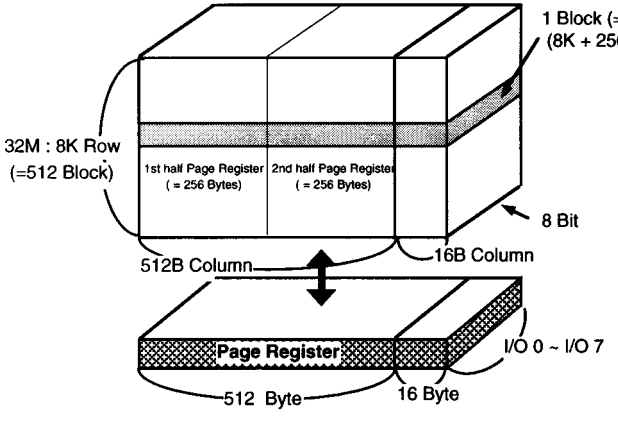


Figure 2. ARRAY ORGANIZATION



1 Page = 528 Byte
1 Block = 528B x 16 Pages
= (8K+256) Bytes
1 Device = 528B x 16Pages x 512 Blocks
= 33 MBits

Product Introduction

The EDI784MSV is a 33Mbit(34,603,008 bit) memory organized as 8192 rows by 528 columns. A spare sixteen columns are located from column address 512 to 527. A 528-byte data register is connected to the memory cell array accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells reside in a different page. A block consists of the 16 pages formed by one NAND structures, totaling 528 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 512 separately erasable 8K-byte blocks.

The EDI784MSV has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows system upgrades to future higher densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{W}$ low while E is low. Data is latched on the rising edge of $\overline{W}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: a cycle for erase-setup and another for erase-execution after block address loading. The 4 Megabyte physical space requires 22 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase, however, only the two row address cycles are used.

Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the EDI784MSV.

Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command During Busy State
Sequential Data Input	80h	--	NO
Read 1	00h/01h(1)	--	NO
Read 2	50h(2)	--	NO
Read ID	90h	--	NO
Reset	FFh	--	YES
Page Program	10h	--	NO
Block Erase	60h	D0h	NO
Erase Suspend	B0h	--	YES
Erase Resume	D0h	--	NO
Read Status	70h	--	YES
Read Register	E0h	--	NO

Notes: 1. The 00h Command defines starting Address on the 1st half of Registers.
The 01h Command defines starting Address on the 2nd half of Registers
After data access on the 2nd half of register by the 01h command , the status pointer is automatically moved to the 1st half register (00H) on the next cycle.
2. The 50H command is valid only when the SE (pin 28) is low.

Pin Description

Command Latch Enable (CLE)- The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{W}$ signal.

Address Latch Enable (ALE)- The ALE input controls the path activation for address and input data to the internal address/data registers. Addresses are latched on the rising edge of $\overline{W}$ with ALE high, and input data is latched when ALE is low.

Chip Enable ($\overline{E}$) - The $\overline{E}$ input is the device selection control. When $\overline{E}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{E}$ high is ignored, and does not return the device to standby mode.

Write Enable ($\overline{W}$) - The $\overline{W}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{W}$ pulse.

Read Enable ($\overline{RE}$) - The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid TREA after the falling edge of $\overline{RE}$, which also increments the internal column address counter by one.

Spare Area Enable ($\overline{SE}$)- The $\overline{SE}$ input is the spare array control, when high it deselects the spare array during Read 1, Sequential data input and Page program.

I/O Port: I/O 0-I/O 7 - the I/O Pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or the outputs are disabled.

Write Protected ($\overline{WP}$) - The $\overline{WP}$ pin provides inadvertent write/erase protection. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready/Busy (R/$\overline{B}$) - The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or outputs are disabled.

Mode Selection

CLE	ALE	$\overline{E}$	$\overline{W}$	$\overline{RE}$	$\overline{SE}$	$\overline{WP}$	Mode	I/O	Power
H	L	L	↑	H	X	X	Command Input	DIN	Active
L	H	L	↑	H	X	X	Address Input (3clock)	DIN	Active
L	H	L	H	↓	X	X	Address Output (3 Clock)	DOUT	Active
L	L	L	↑	H	L/H(3)	X	Data Input	DIN	Active
L	L	L	H	↓	L/H(3)	X	Sequential Read & Data Output	DOUT	Active
X	X	X	X	X	L/H(3)	H	During program (Busy)	High-Z	Active
X	X	X	X	X	X	H	During Erase (Busy)	High-Z	Active
X	X(1)	X	X	X	X	L	Write Protect	High-Z	Active
X	X	H	X	X	OV/VCC(2)	OV/VCC(2)	Stand-by	High-Z	Stand-by

Notes: 1. X can be VIL or VIH
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby
3. When $\overline{SE}$ is high, spare area is deselected

Absolute Maximum Ratings*

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	VIN	-0.6 to +5.5	V
Operating Temperature TA (Ambient)			
Commercial		0 to + 70	°C
Industrial		-40°C to +85	°C
Military		-55°C to +125	°C
Storage Temperature	TSTG	-65° to + 150	°C
Short Circuit Output Current	IOS	5	mA

Notes: Minimum DC voltage is -0.3V an input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is VCC+0.5V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

Ta=-55 to +125C, VCC=3.3V±10%, unless otherwise noted

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.0		5.5	V
Input Low Voltage	VIL	-0.3		0.8	V

AC Test Condition

Ta=-55 to +125C, VCC=3.3V±10%, unless otherwise noted

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and CL=100pf

DC and Operating Characteristics

Parameter		Sym	Conditions	Min	Typ	Max	Units
Operating Current	Sequential	ICC1	tcycle = 50ns $\overline{E}$=VIL,Iout=0mA	-	10	20	mA
	Read	ICC2	tcycle = 1us $\overline{E}$=VIL,Iout=0mA	-	2	5	mA
	Command Address Input	ICC3	tcycle = 50ns		10	20	mA
	Data Input	ICC4	--	-	10	20	mA
	Register Read	ICC5	tcycle = 50ns Iout = 0mA	-	10	20	mA
	Program	ICC6	--	-	10	20	mA
	Erase	ICC7	--	-	10	20	mA
Stand-by Current (TTL)		ISB1	$\overline{E}$=VIH,$\overline{WP}$=$\overline{SE}$=0V/VCC	-	-	1	mA
Standby Current (CMOS)		ISB2	$\overline{E}$=VCC-0.2, $\overline{WP}$=$\overline{SE}$=OV/VCC	-	5	50	µA
Input Leakage Current		ILI	VIN=0 to 3.6V	-	-	±10	µA
Output Leakage Current		ILO	VOUT=0 to 3.6V	-	-	±10	µA
Input High Voltage, All Inputs		VIH	-	2.0	-	VCC+0.5	V
Input Low Voltage, All inputs		VIL	-	-0.3	-	0.8	V
Output High Voltage Level		VOH	IOH=-400µA	2.4	-	-	V
Output Low Voltage Level		VOL	IOL=2.1 mA	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		IOL(R/$\overline{B}$)	VOL=0.4V	8	10	-	mA

Capacitance

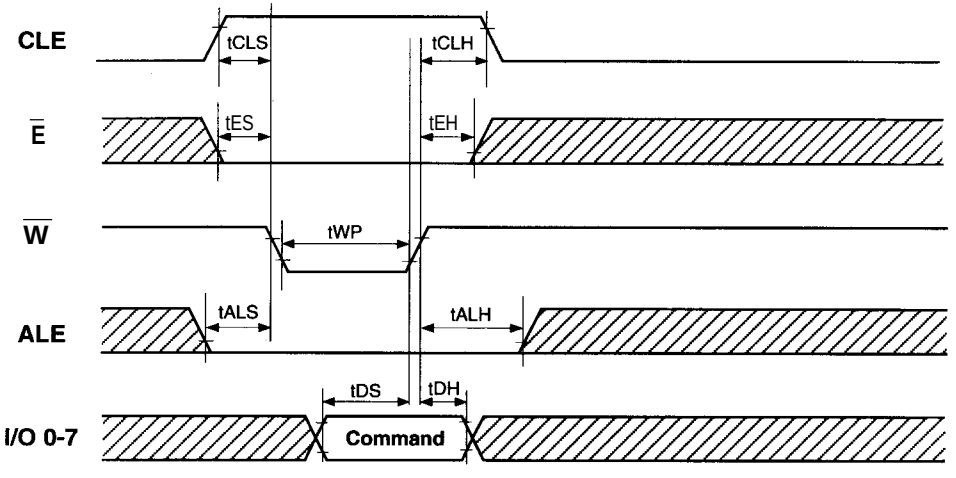
Ta=-55 to +125C, VCC=3.3V±10%, unless otherwise noted, guaranteed, but not tested.

Item	Symbol	Condition	Min	Max	Unit
Input/Output Capacitance	CI/O	VIL = 0V	-	10	pF
Input Capacitance	CIN	VIN = 0V	-	10	pF

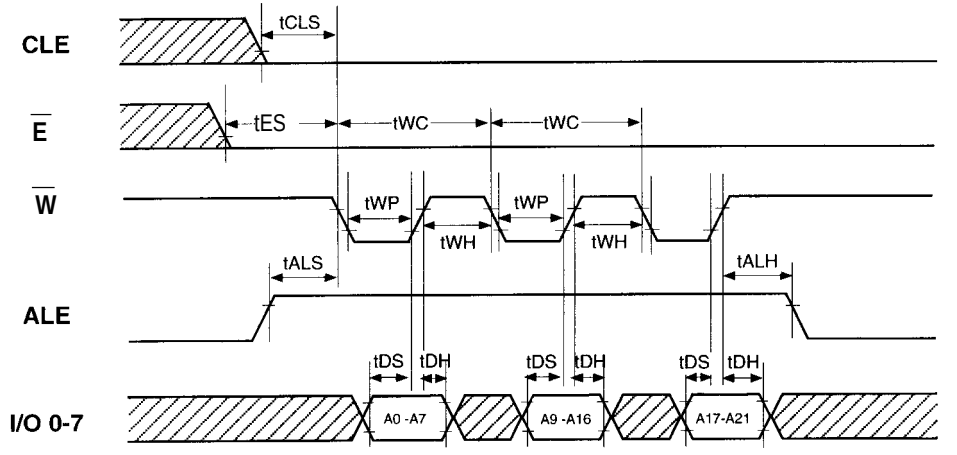
AC Characteristics for Command/Address/Data Input

Parameter	Sym	Min	Max	Unit
CLE Set-up Time	TCLS	0	-	ns
CLE Hold Time	TCLH	10	-	ns
$\overline{E}$ Setup Time	TES	0	-	ns
$\overline{E}$ Hold time	TEH	10	-	ns
$\overline{W}$ Pulse Width	TWP	25	-	ns
ALE Set-up Time	TALS	0	-	ns
ALE Hold Time	TALH	10	-	ns
Data Set-up Time	TDS	20	-	ns
Data Hold Time	TDH	10	-	ns
Write cycle Time	TWC	50	-	ns
$\overline{W}$ High Hold time	TWH	10	-	ns

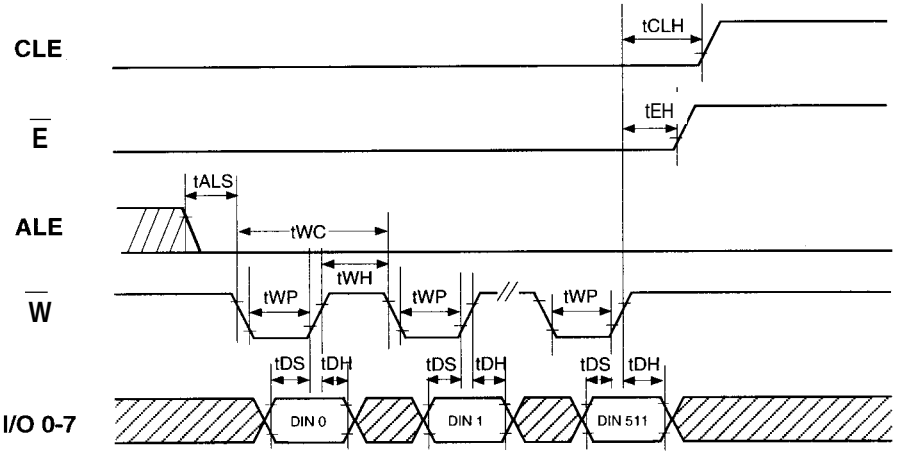
Command Latch Cycle



Address Latch Cycle



Input Data Latch Cycle



AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	TR	-	10	µs
ALE to $\overline{RE}$ Delay (Read register, Read ID)	TAR1	150	-	ns
ALE to $\overline{RE}$ Delay (Read Cycle)	TAR2	50	-	ns
$\overline{E}$ to $\overline{RE}$ Delay (Address register read, ID Read)	TCR	100	-	ns
Ready to $\overline{RE}$ Low	TRR	20	-	ns
$\overline{W}$ High to Busy	TWB	-	100	ns
Read Cycle Time	TRC	50	-	ns
$\overline{RE}$ Access Time	TREA	-	35	ns
$\overline{RE}$ High to Output Hi-Z	TRHZ	15	30	ns
$\overline{E}$ High to Output Hi-Z	TEHZ	-	20	ns
$\overline{RE}$ High Hold Time	TREH	10	-	ns
Output Hi-Z to $\overline{RE}$ Low	TIR	0	-	ns
Last $\overline{RE}$ High to Busy (at sequential read)	TRB	-	100	ns
$\overline{E}$ High to ready (in case of interception by CE at read)	TEHRY	-	50+tr($R/\overline{B}$)	ns
$\overline{E}$ High Hold Time (at the last serial read)	TEH	100	-	ns
ALE Setup Time (Register Read)	TALS1	10	-	ns
$\overline{RE}$ Low to Status Output	TRSTO	-	35	ns
$\overline{E}$ Low to Status Output	TESTO	-	45	ns
$\overline{RE}$ High to W Low	TRHW	0	-	ns
$\overline{W}$ High to $\overline{E}$ Low	TWHEL	30	-	ns
$\overline{W}$ High to $\overline{RE}$ Low	TWHR	60	-	ns
$\overline{W}$ High to $\overline{RE}$ Low (Register Read)	TWHR1	200	-	ns
Erase Suspend Input to Ready	TSR	-	500	µs
$\overline{RE}$ access time (Read ID)	TREADID	-	35	ns
Device Resetting Time (Read/Program/Erase/after erase suspend)	TRST	-	5/10/500/5	µs

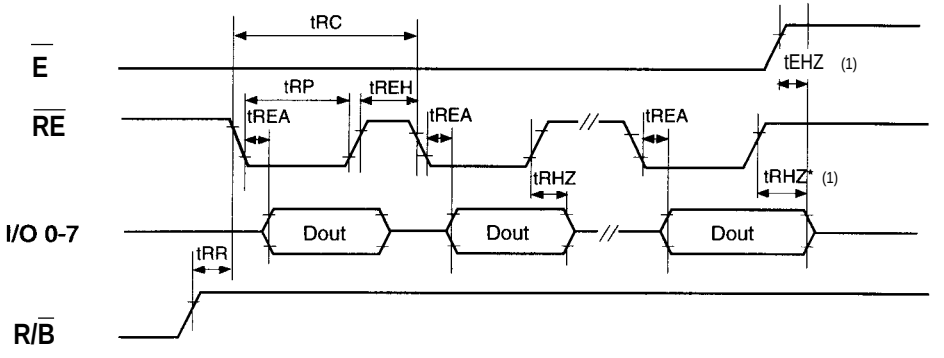
Notes: 1. If $\overline{E}$ goes high within 30ns after the rising edge of the last $\overline{RE}$, $R/\overline{B}$ will not transition to VOL.
2. The time to Ready depends on the value of the pull-up resistor tied to $R/\overline{B}$ pin.
3. To break the sequential ready cycle, $\overline{E}$ must be held high for longer than TEH.

Program/Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	tPROG	-	0.25	1.5	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	10	cycles
Block Erase Time	tBERS	-	5	30	ms

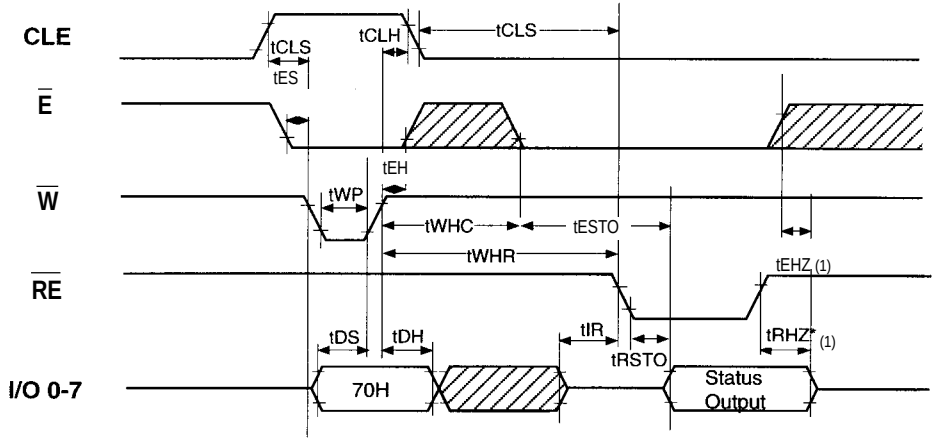
Sequential Out Cycle after Read

(CLE=L,WE=H,ALE=L)



Note: 1. Transition is measured ±200mv from steady voltage with load.
This parameter is sampled and not 100% tested.

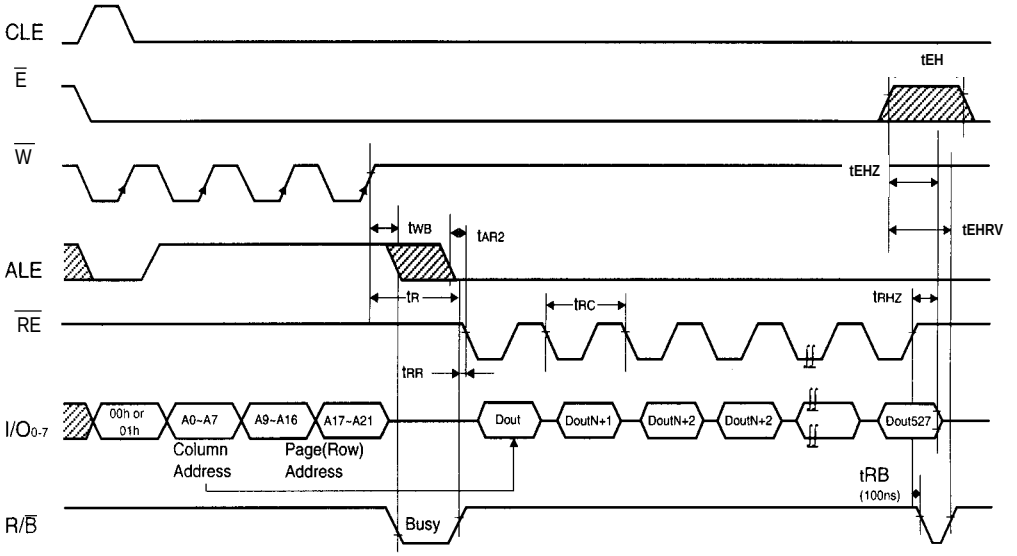
Status Read Cycle



Note: 1.Transition is measured ±200mv from steady voltage with load.
This parameter is sampled and not 100% tested.

Read 1 Operation

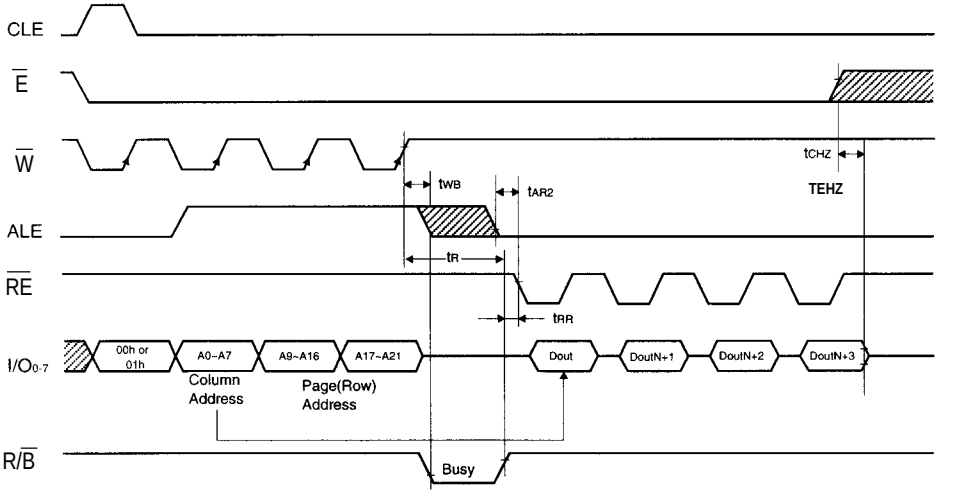
(Read One Page)



Note: 1.Transition is measured ±200mv from steady voltage with load.
This parameter is sampled and not 100% tested.

Read 1 Operation

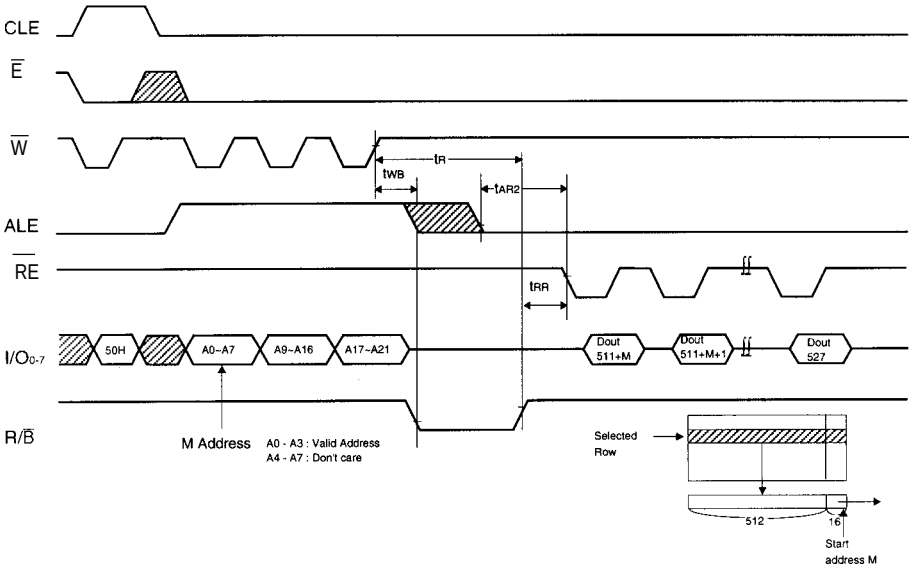
(Intercepted by $\overline{E}$)



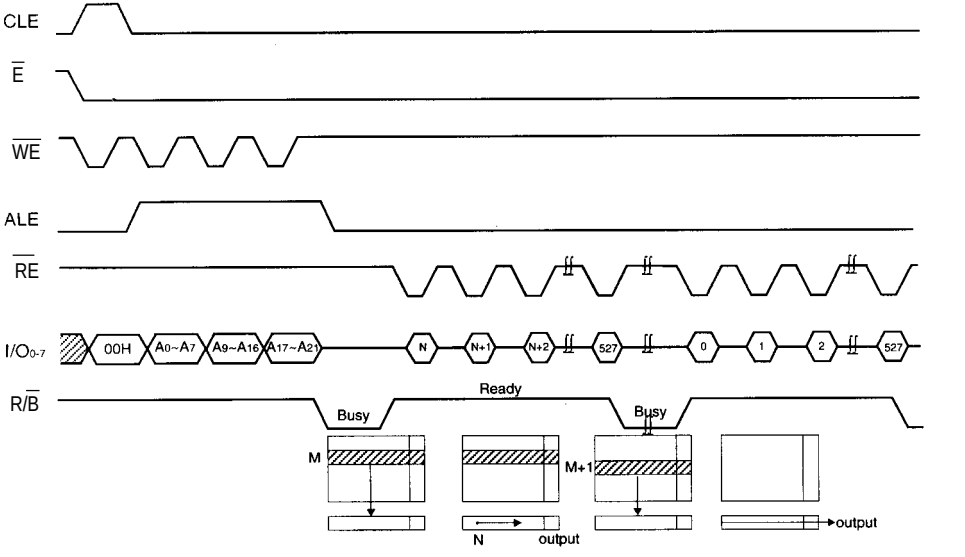
Note: 1.Transition is measured ±200mv from steady voltage with load.
This parameter is sampled and not 100% tested.

Read 2 Operation

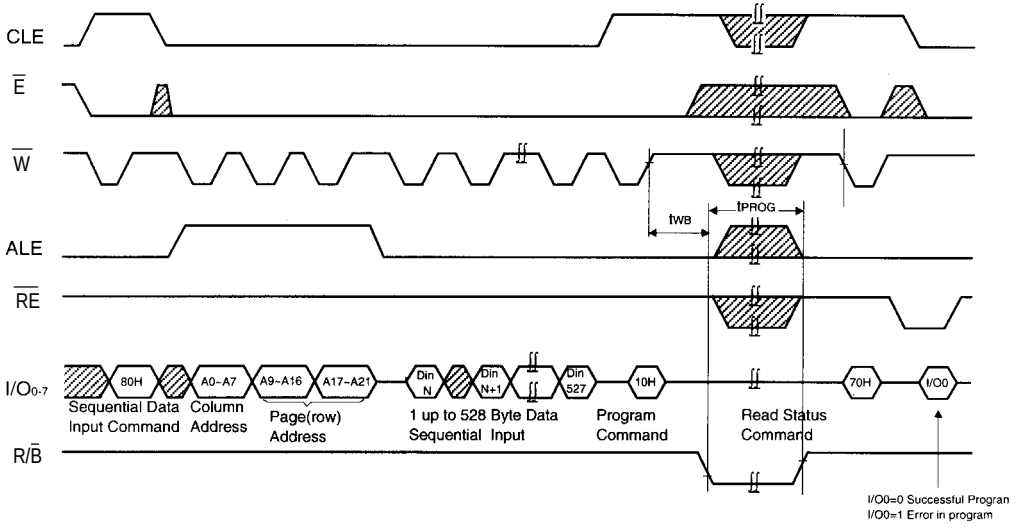
(Read One Page)



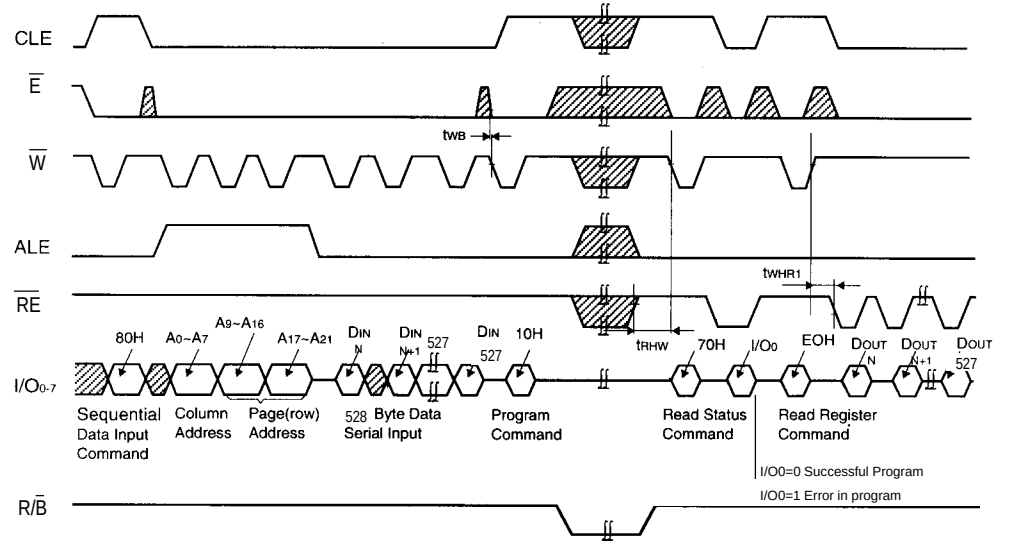
Sequential Row Read Operation



Page Program Operation

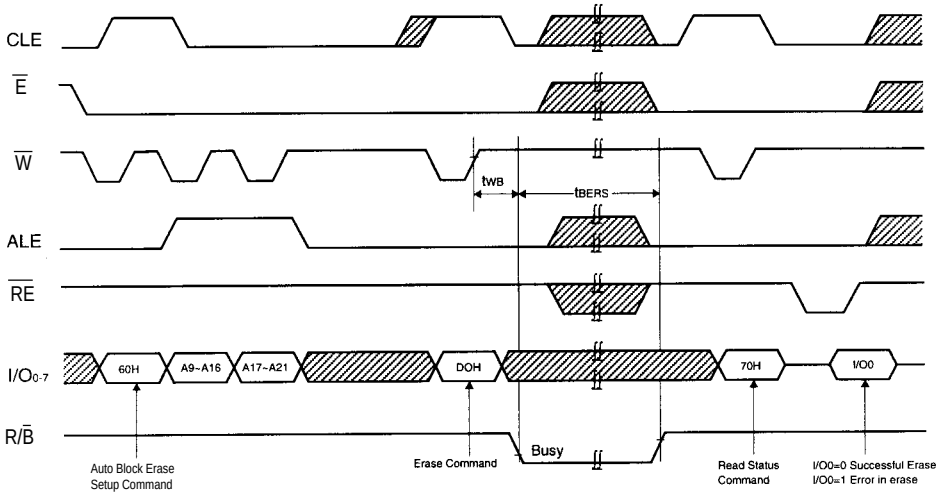


Page Program & Read Data Registration Operation

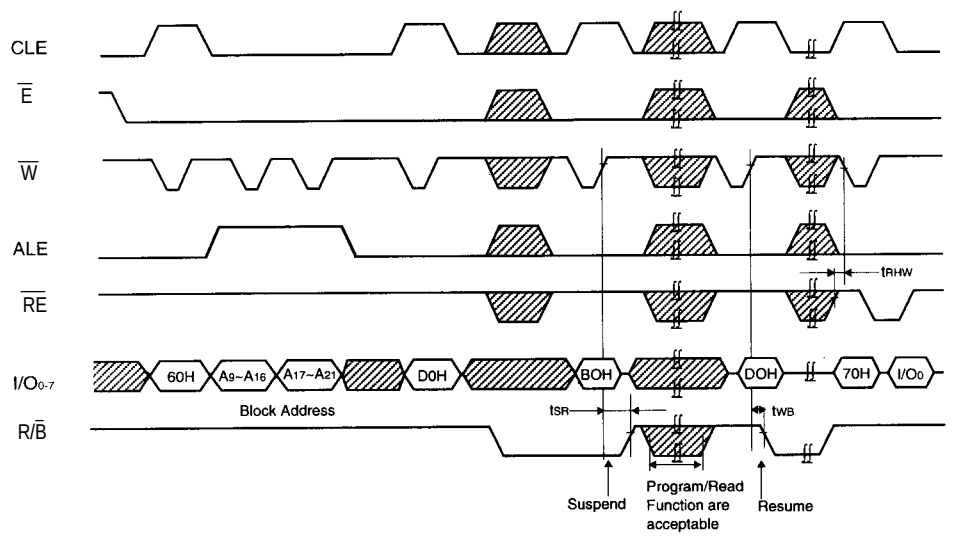


Block Erase Operation

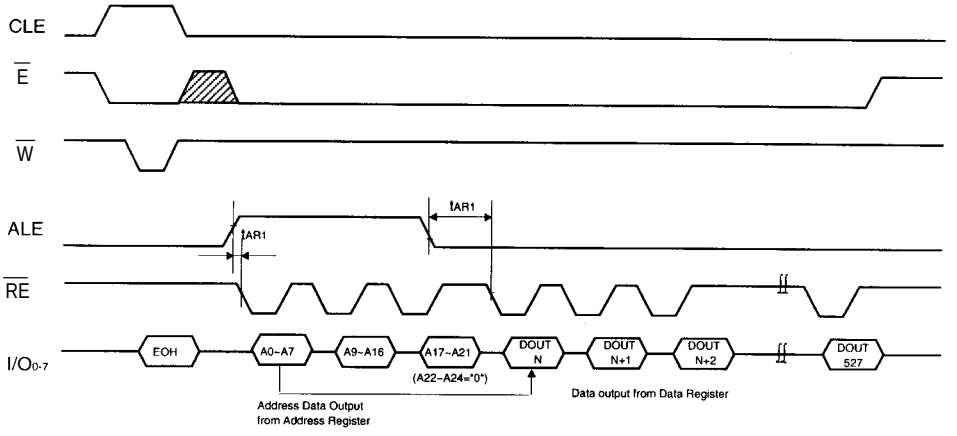
(Erase One Block)



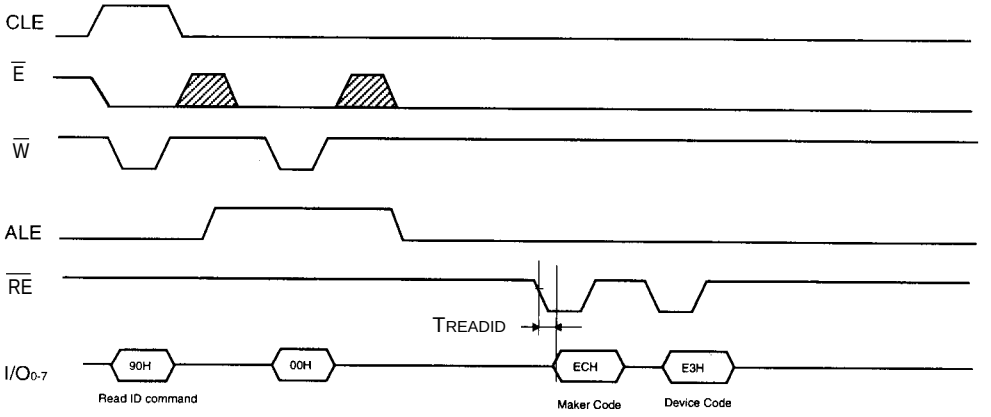
Suspend & Resume Operation During Block Erase



Read Register Operation



Manufacturer & Device ID Read Operation



Device Operation

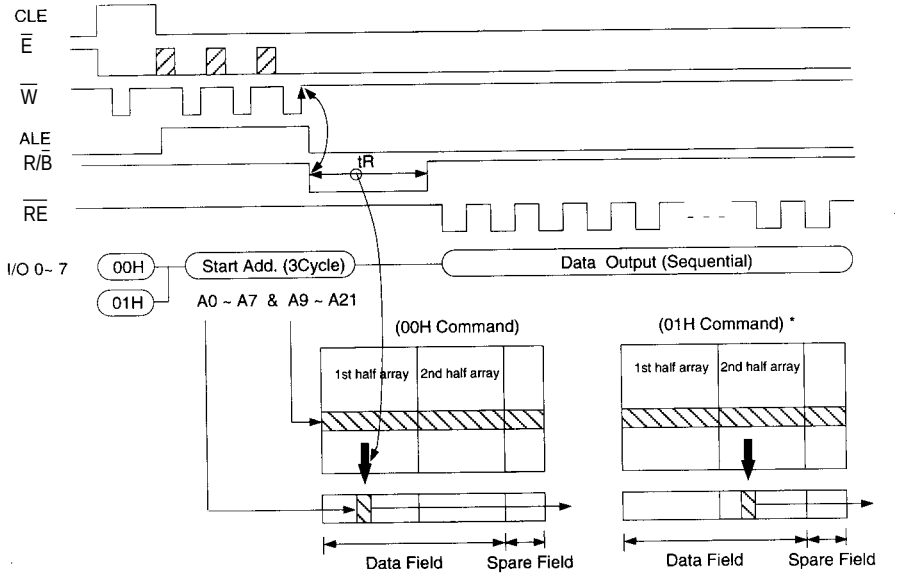
Page Read

The EDI784MSV defaults to Read 1 mode after device power-up. Entering Read 1 mode is also initiated by writing 00H or 01H to the command register, followed by three address cycles. Once the command is latched, it does not need to be written for additional page read operations. Three types of READ 1 accesses may occur: random read, serial page read and sequential read.

The random read occurs when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less the 10us (TR). The CPU can detect the completion of this data transfer(TR) by analyzing the output of Ready/Busy pin. Once the page of data is loaded into the page register, the data may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$ while $\overline{E}$ low. Data is output (serial page read) starting from the selected column address up to the last column address of the page (column 511 or 527 depending on state of $\overline{SE}$ pin). After the data of last column address is clocked out, the next sequential page is automatically selected for serial page read. Waiting 10us again allows for register loading of the selected page. The sequential read operation is terminated by bringing $\overline{E}$ high.

The Read 1 and Read 2 commands act as a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read 2 command with $\overline{SE}$ pin low level. Address A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential read as in Read 1 operation and spare sixteen bytes of each page may be sequentially read. The Read 1 command (00H) is needed to move the pointer back to the main area. Figures 3 thru 6 show typical sequence and timings for each read operation.

Figure 3. Read 1 Operation



* After data access on 2nd half array by 01H command, the start pointer is automatically moved to 1st half array (OOH) at next cycle

Figure 4. Read 2 Operation

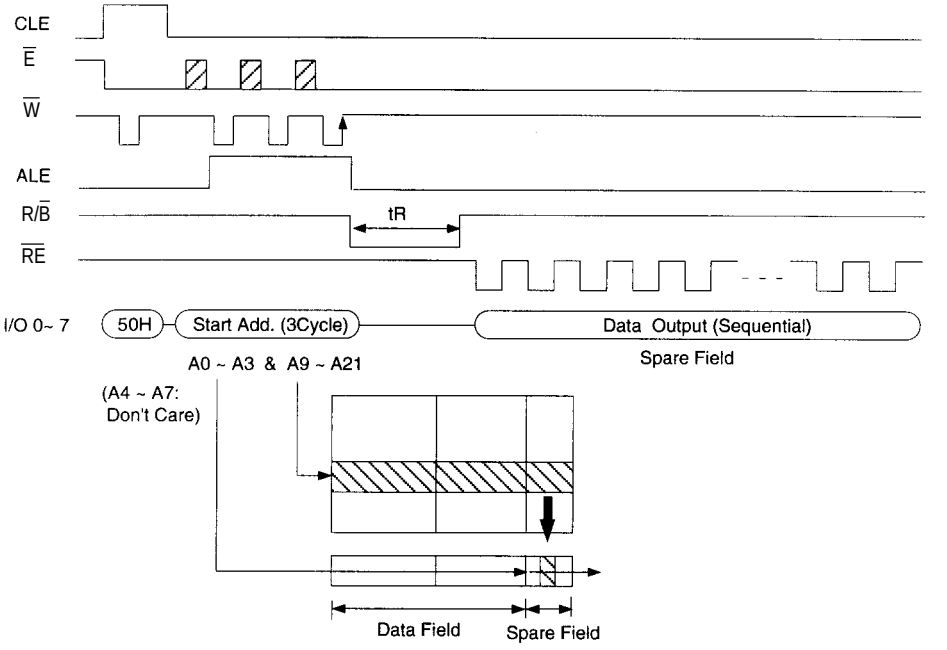


Figure 5. Sequential Read 1 Operation

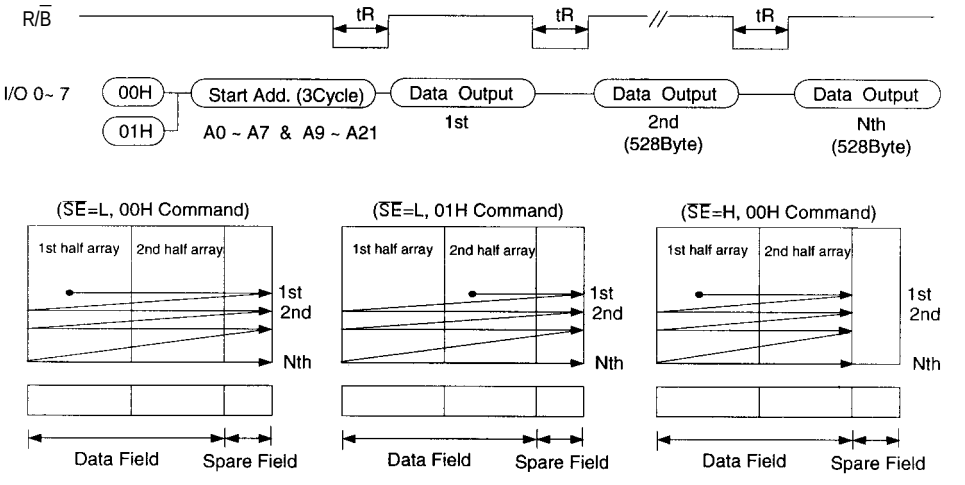
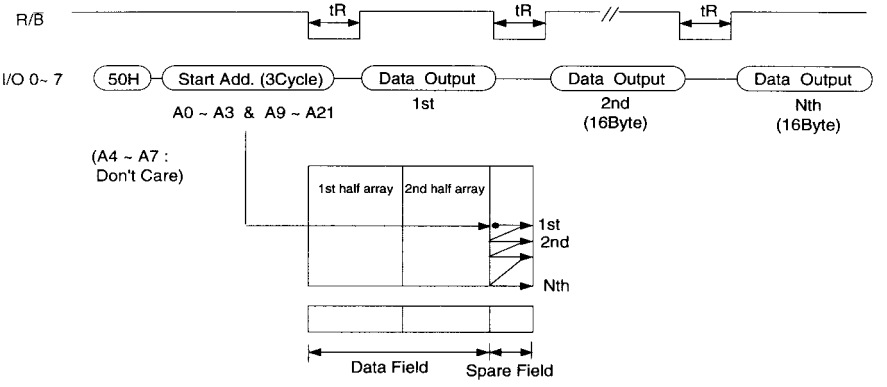


Figure 6. Sequential Read 2 Operation

(SE = fixed low)



Page Program

The EDI784MSV device is programmed on a page (528 byte) basis. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a nonvolatile programming period where the loaded data is programmed into the appropriate cells. The serial data loading period begins by inputting the Serial Data Input command (80H) followed by the three cycle address input. The data to be programmed is then loaded serially into the page register. $\overline{W}$ clocks in each byte of data to be programmed. The bytes other than those to be programmed do not need to be loaded. The Page Program confirm command (10H) initiates the programming process. Writing (10H) alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{E}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the Ready/Busy output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked (Figure 7). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. The data register may be read by writing the Read Register command (EOH) to determine the column address at which the error has been detected. The registers in error will have "1"s while the registers of successfully programmed bits will have "0"s (Figure 8).

The EDI784MSV does allow partial page programming: a byte or consecutive bytes within a page may be updated (Programmed) without erasing the contents of the page. The number of consecutive partial page programming operations within the same page without an intervening erase operation must not exceed ten. Note: When updating data, only cells containing "1" may be updated to "0". A cell containing a "0" can not be updated to a "1", this requires an erase operation.

Figure 7. Program & Read Status Operation

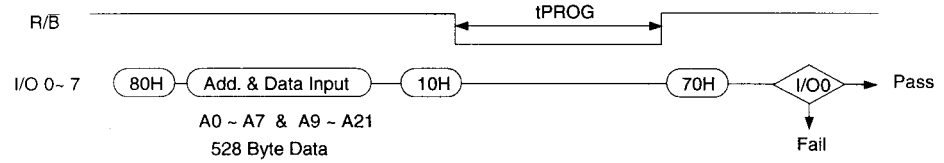
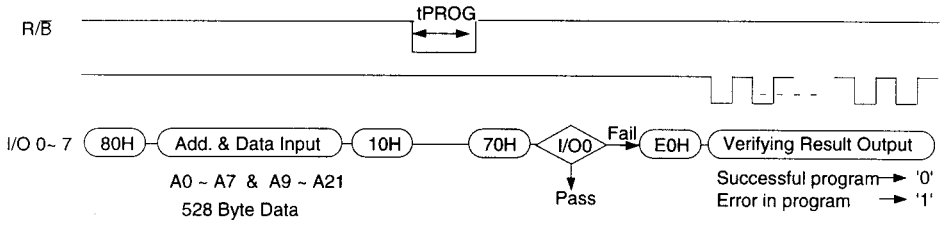


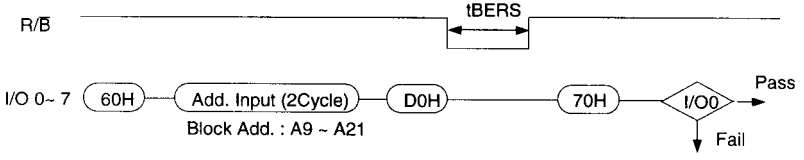
Figure 8. Program & Read Data Register Operation



Block Erase

The Erase operation erases data on a block (8K Byte) basis. Block address loading is accomplished in two cycles initiate by an Erase Setup command (60H). Only address A13 to A21 is valid while A9 to A12 is ignored. The Erase Confirm command (DOH) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased due to external noise

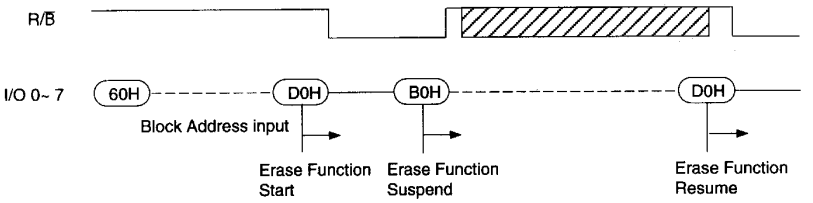
Figure 9. Block Erase Operation



Erase Suspend/Erase Resume

The Erase Suspend allows interruption during any erase operation in order to read or program data to or from another block of memory. Once an erase process begins, writing the Erase Suspend command (BOH) to the command register suspends the internal erase process, and the Ready/Busy signal return to "1". Erase Suspend Status bit will be also set to "1" when the Status Register is read. At this time, blocks other than the suspended block can be read or programmed. The Status Register and Ready/Busy operation will function as usual. After the Erase Resume command DOH, the Erase Suspend Status bit and Ready/Busy will return to "0". Refer to Figure 11 for operation sequence.

Figure 10. Erase Suspend & Erase Resume Operation



Read Status

The EDI784MSV contains a Status Register which can be read to find out whether program or erase operation is complete, and whether the program or erase operation completed successfully. After writing 70H command to the command register, a read cycle outputs the contents of the Status Register to the I/O pins on the falling edge of $\overline{E}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{E}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the Status Register is read during a random read cycle, the required Read Command (00H or 50H) should be input before serial page read cycle.

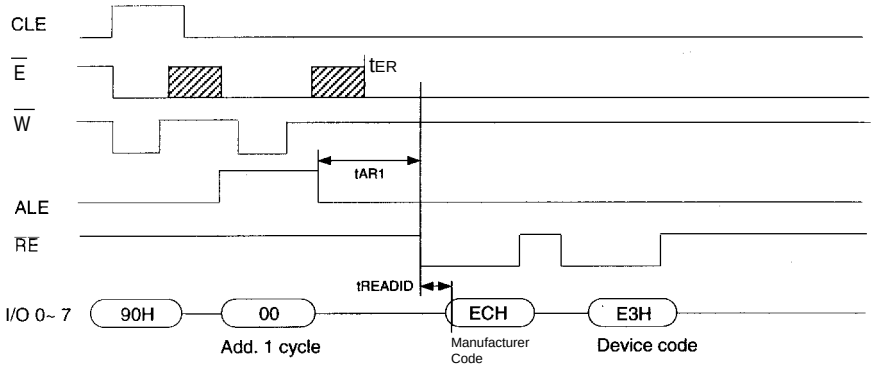
Table 2. Status Register Definition

SR	Status	Definition
I/O 0	Program/Erase–	"0": Successful Program /Erase "1" Error in Program Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5	Erase Suspend	"0" : Erase in Progress/Completed "1": Suspended
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1": Not Protected

Read ID

The EDI784MSV contains a product identification mode, initiated by writing 90H to the command register, followed by an address input of 00H. Two read cycles sequentially outputs the manufacturer code (ECH), and the device code (E3H) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 12 shows the operation sequence.

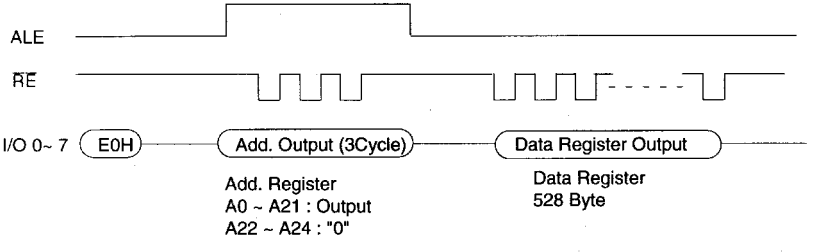
Figure 11. Read ID Operation



Read Register

The EDI784MSV has 528 data registers and 3 address registers which may be read by writing E0H to the command register. Toggling $\overline{RE}$ with ALE high will output the contents of the address registers. Toggling $\overline{RE}$ with ALE low drives the the contents of the data registers sequentially beginning with column address. The Read Register mode can be used in conjunction with the Page Program operation to identify the bits in programming error by reading the data registers. Figure 13 shows the flow chart.

Figure 12. Read Address and Data Register Operation



Reset

The EDI784MSV offers a reset feature, executed by writing FFH to the command register. When the device is in Busy state during random read, program erase modes, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. Internal address registers are cleared to "0"s and data registers to "1"s. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0H when $\overline{WP}$ is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted to by the command register. The Ready/Busy pin transitions to low for tRST after the Reset command is written Reset command is not necessarily for normal operation. Refer to figure 14 below.

Figure 13. Reset Operation

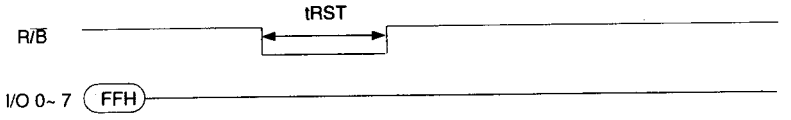
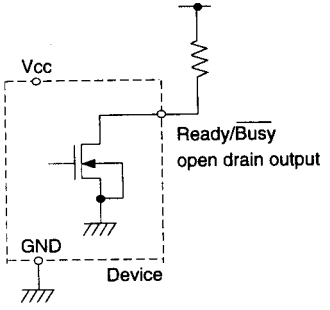


Table 3. Device Status

	After Power-up	After Reset
Address Register	All "0"	All "0"
Data Register	All "1"	All "1"
Operation Mode	Read 1	Waiting for next command

Ready/Busy

The EDI784MSV has a Ready/Busy output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read begins after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more Ready/Busy outputs to be Or-tied. An appropriate pull-up resistor is required for proper operation and the value may be calculated by following equation:



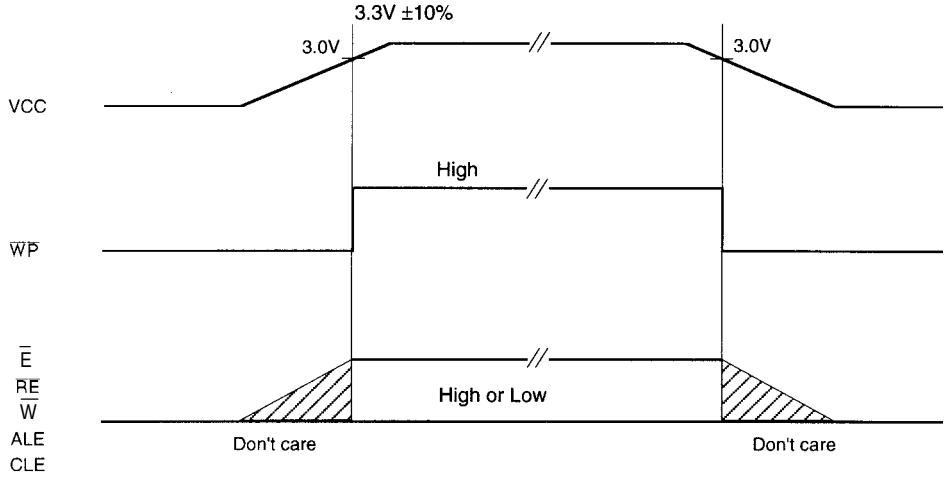
$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

Data Protection

The EDI784MSV has a write protect pin ($\overline{WP}$) that should be used to provide protection from any accidental write operation. During device power up, the $\overline{WP}$ should be at VIL until VCC reaches approximately 3.0V, during power down $\overline{WP}$ should be at VIL when VCC falls below 3.0V. Refer to Figure 25 below.

Figure 14. AC Waveforms for Power Transitions



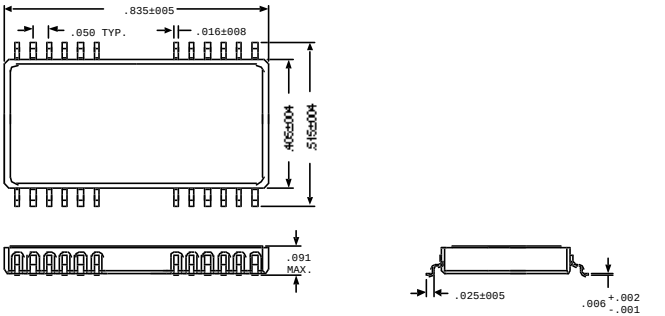
Ordering Information

Part No.	Speed (ns)	Package No.
EDI784MSV50BB	50	348
EDI784MSV50FB	50	349

For Commercial, Industrial or Military grade product use C,I or M, respectively, to replace B in the suffix of the part number, e.g. EDI784MSV50BB becomes EDI784MSV50BC (Commercial Temp Range) or EDI784MSV50BI (Industrial Temp Range).

Package Description

Package No. 348
24/32 Pin
Ceramic
Thinpack



Package No. 349
24/32 Pin
Ceramic
Flatpack