

4x512Kx16 Static RAM

CMOS, Module

Features

4x512Kx16 bit CMOS Static

Random Access Memory

- Access Times 70 thru 100ns
- Data Retention Function (EDI9F416512LP)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

High Density Packaging

- 80 Pin SIMM, No. 372

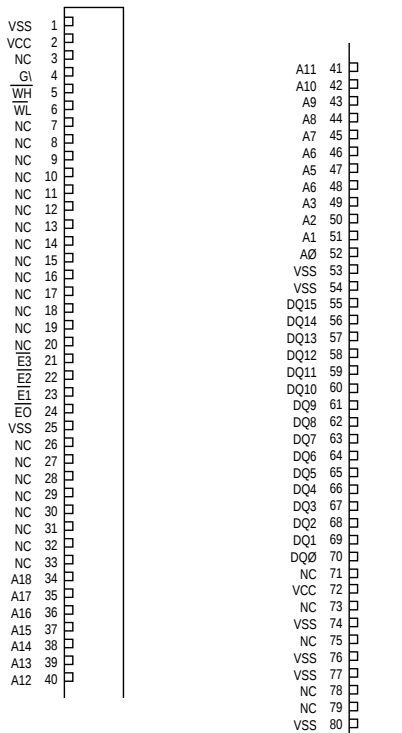
Single +5V ($\pm 10\%$) Supply Operation

The EDI9F416512C is a 32Megabit CMOS Static RAM based on eight 512Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR-4) substrate.

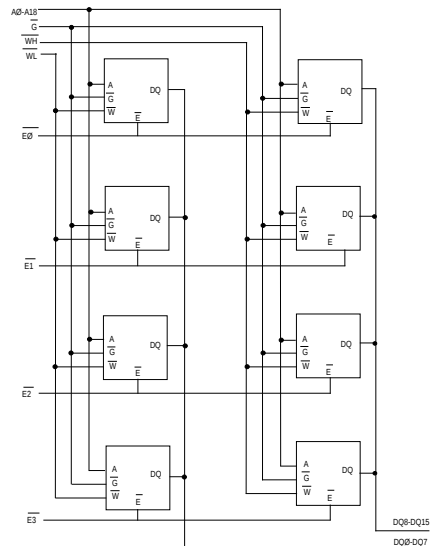
A low power version with data retention (EDI9F416512LP) is also available.

All inputs and outputs are TTL compatible and operate from a single +5V supply. Fully asynchronous, the EDI9F416512C requires no clocks or refreshing for operation.

Pin Configurations and Block Diagram



A0-A18	Address Inputs
E0-E3	Chip Enable
G	Output Enables
WH-WL	Write Enables
DQ0-DQ15	Data Input/Output
VCC	Supply 5 Volts
VSS	Ground
NC	No Connect



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	1 Watt
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V				
Input Rise and Fall Times	5ns				
Input and Output Timing Levels	1.5V				
Output Load	70ns	1TTL = 30pF			
	85-120ns	1TTL, CL = 100pF			

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power	ICC1	W, E = VIL, I/O = 0mA,	--	100	158	mA
Supply Current		Min Cycle				
Standby (TTL) Power	ICC2	E ≥ VIH, VIN ≤ VIL	--	5	35	mA
Supply Current		VIN ≥ VIH				
Full Standby Power	ICC3	E ≥ VCC-0.2V	C	--	25	mA
Supply Current		VIN ≥ VCC-0.2V or	LP	--	150	μA
CMOS		VIN ≤ 0.2V				
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±10	μA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10	μA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

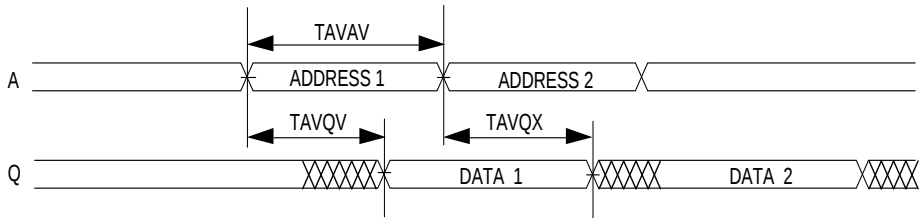
(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	60	pF
Data Lines	CD/Q	50	pF
Chip Enable Line	CC	25	pF
Write and Output Enable Lines CW		60	pF

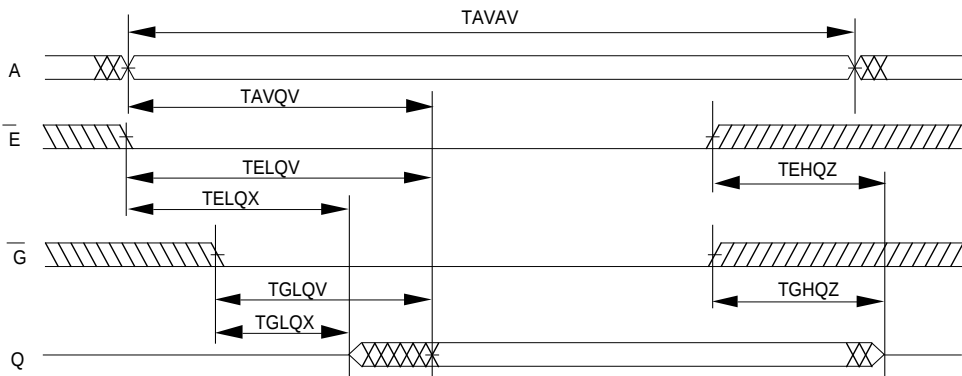
AC Characteristics Read Cycle

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	70		85		100		ns
Address Access Time	TAVQV	TAA		70		85		100	ns
Chip Enable Access Time	TELQV	TACS		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		30		35		40	ns

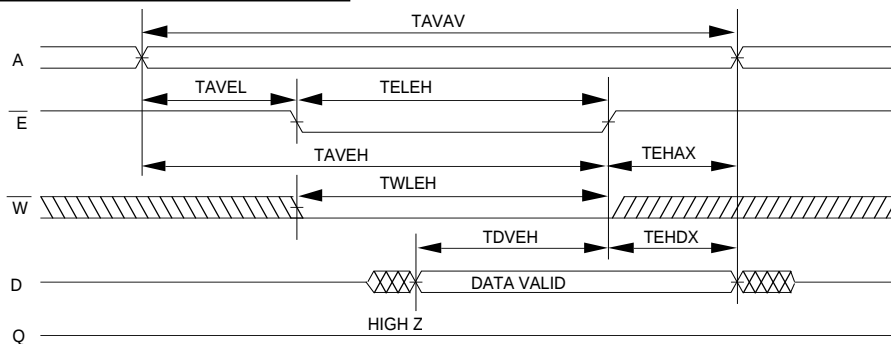
Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High



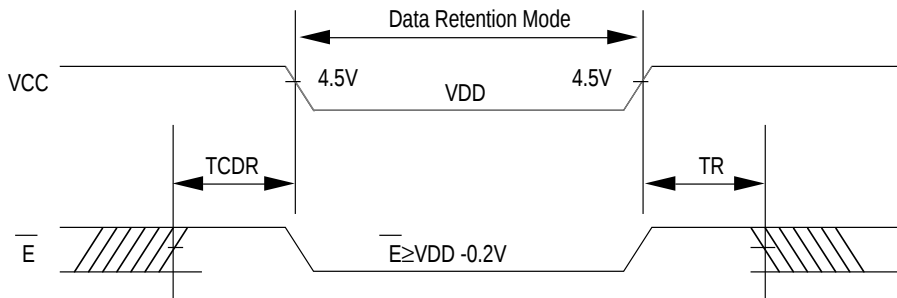
Write Cycle 2 - $\bar{E}$ Controlled



Data Retention Characteristics

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 0.2V		2	--		V
Data Retention Quiescent Current	ICCDR	E ≥ VDD - 0.2V VIN ≥ VDD - 0.2V or VIN ≤ 0.2V	3V	--	8	100	μA
Chip Disable to Data Retention Time(1)	TCDR			0	--	--	ns
Operation Recovery Time (1)	TR			5	--	--	ms

Data Retention - $\bar{E}$ Controlled



Ordering Information

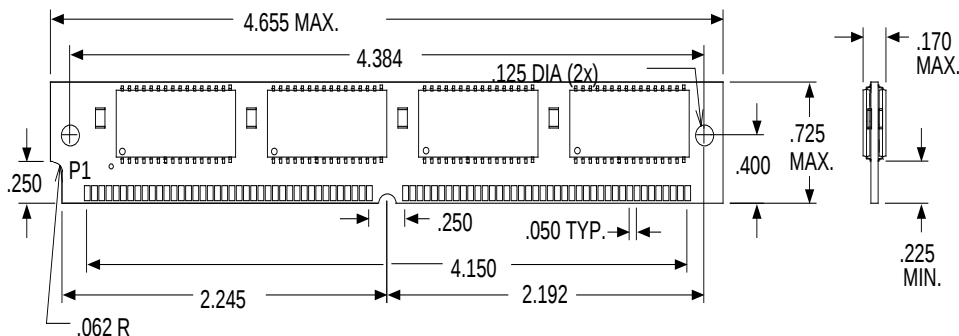
Part Number	Speed (ns)	Package No.
Standard Power		
EDI9F416512C70BNC	70	372
EDI9F416512C85BNC	85	372
EDI9F416512C100BNC	100	372
Low Power		
EDI9F416512LP70BNC	70	372
EDI9F416512LP85BNC	85	372
EDI9F416512LP100BNC	100	372

Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI9F416512C70BNC becomes EDI9F416512C70BNI.

Package Description

Package No. 372

80 Lead SIMM Angled



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