Features

512Kx8 bit CMOS Static
Random Access Memory

- Access Times 20 thru 35ns
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

High Density Packaging

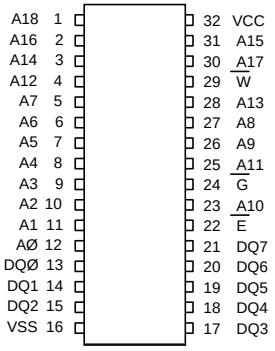
- 32 Pin DIP, JEDEC Pinout, No. 415

Single +5V (±10%) Supply Operation

512Kx8 Static RAM
CMOS, Module

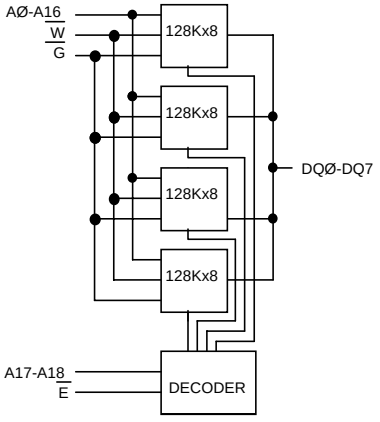
The EDI8F8513C is a 4096K bit CMOS Static RAM based on four 128Kx8 or Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.
Functional equivalence to the monolithic four megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address(es) to select one of the128Kx8 RAMs.
The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device, to ensure compatibility with future monolithics.
All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8F8513C requires no clocks or refreshing for operation.

Pin Configurations and Block Diagram



Pin Names

AØ-A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load 20-35ns	1TTL = 30pF
70-100ns	1TTL, CL =100pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max		Units
				-35	20-25	35	ns
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	225	570	390	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL	--	90	130	130	mA
		VIN $\geq$ VIH	--	--	--	--	mA
Full Standby Power Supply Current (CMOS)	ICC3	$\overline{E} \geq$ VCC-0.2V	--	5	40	40	mA
		VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V	--	--	--	--	µA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±10	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10	±10	µA
Output High Voltage	VOH	IOH =-4.0	2.4	--	--	--	V
Output Low Voltage	VOL	IOL =8.0mA	--	--	0.4	0.4	V

*Typical: TA=25°C, VCC=5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	43	pF
Chip Enable Line	CC	10	pF
Write and Output Enable Lines	CW	32	pF

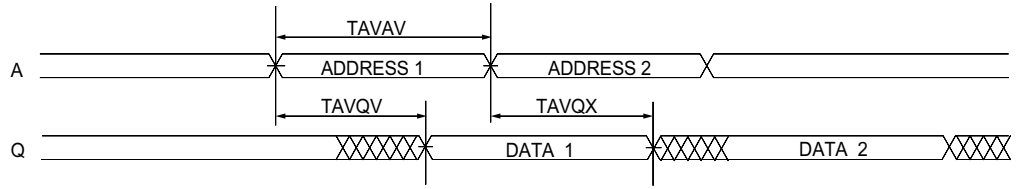
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

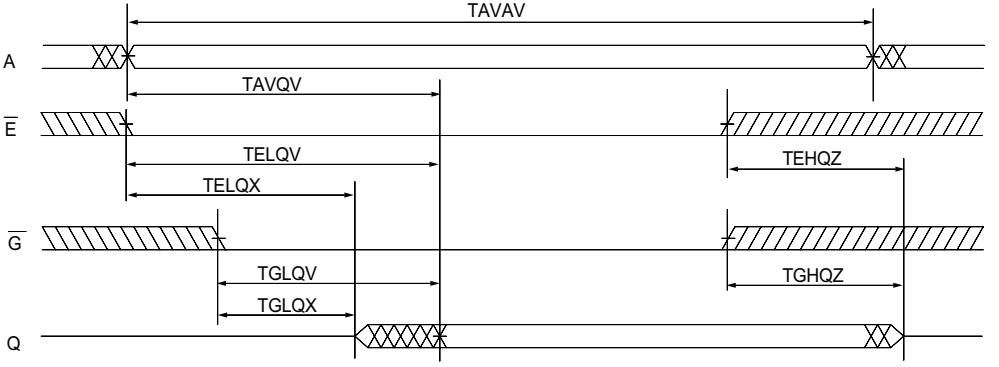
Parameter	Symbol JEDEC	Symbol Alt.	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Read Cycle Time	TAVAV	TRC	20		25		35		ns
Address Access Time	TAVQV	TAA		20		25		35	ns
Chip Enable Access Time	TELQV	TACS		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		15	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		13		15		20	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		8		10		12	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

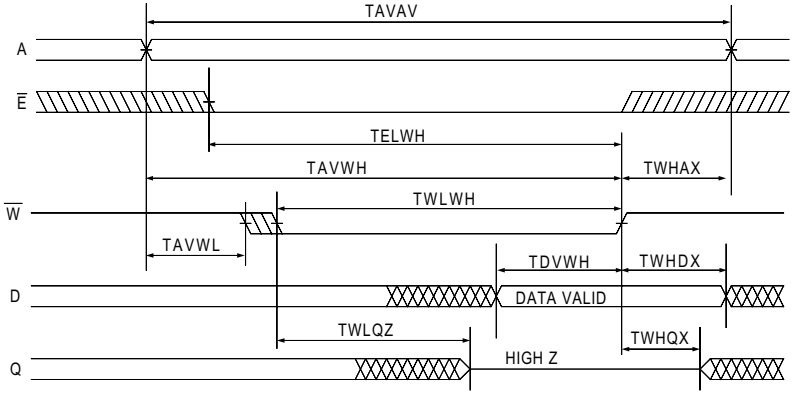


AC Characteristics Write Cycle

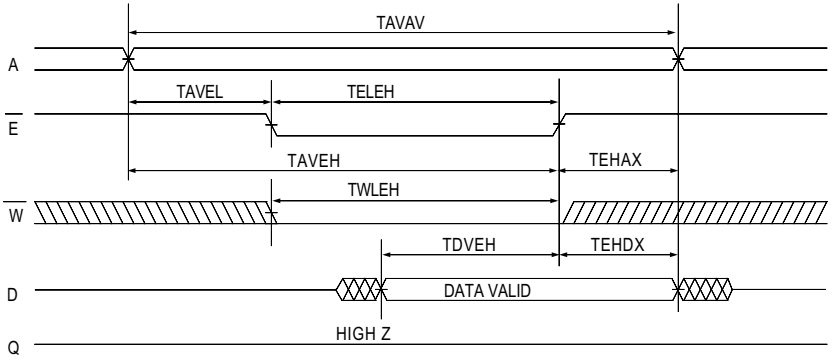
Write Cycle	Symbol		20ns		25ns		35ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	20		25		35		ns
Chip Enable to End of Write	TELWH	TCW	15		20		30		ns
	TELEH	TCW	15		20		30		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	15		20		30		ns
	TAVEH	TAW	15		20		30		ns
Write Pulse Width	TWLWH	TWP	15		20		25		ns
	TWLEH	TWP	15		20		25		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TDH	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	12	0	15	ns
Data to Write Time	TDVWH	TDW	12		15		20		ns
	TDVEH	TDW	12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - E Controlled

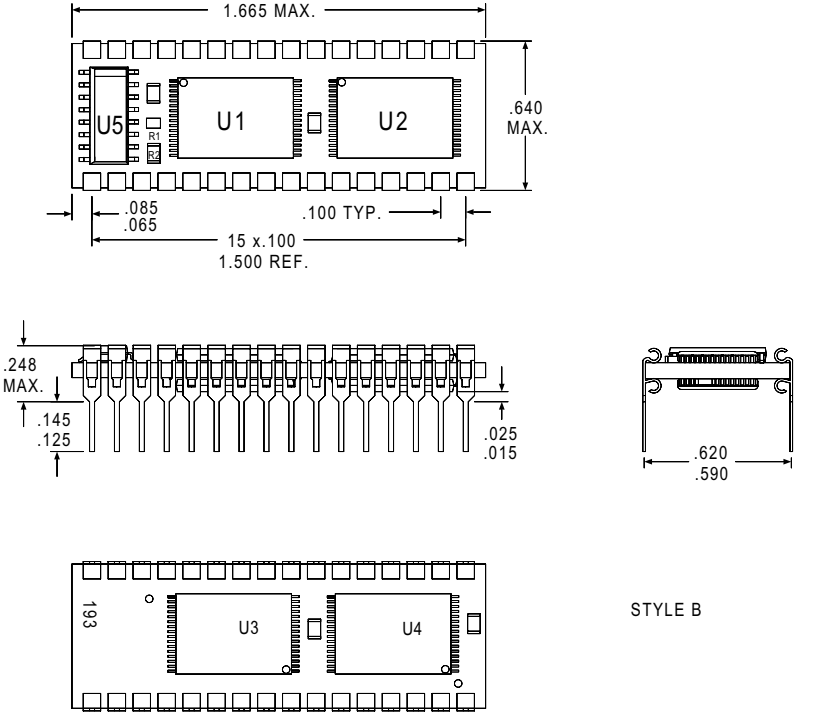


Ordering Information

Standard Power	Speed (ns)	Package No.
EDI8F8513B20M6C	20	415
EDI8F8513B25M6C	25	415
EDI8F8513B35M6C	35	415

Package Description

Package No. 415
32 Pin Dual-in-line Package



STYLE B