Features

128Kx24 bit CMOS Static
Random Access Memory

- Access Times 20, 25, and 35ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Package

- 60 Pin ZIP, No. 158
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

128Kx24 Static RAM
CMOS, High Speed Module

The EDI8F24128C is a high speed 3 megabit Static RAM module organized as 128K words by 24 bits. This module is constructed from three 128Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.
Three chip selects (EØ-E2) are used to independently enable the three bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.
The EDI8F24128C is offered in 60 pin ZIP package, which enable three megabits of memory to be placed in less than 0.75 square inches of board space.
All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

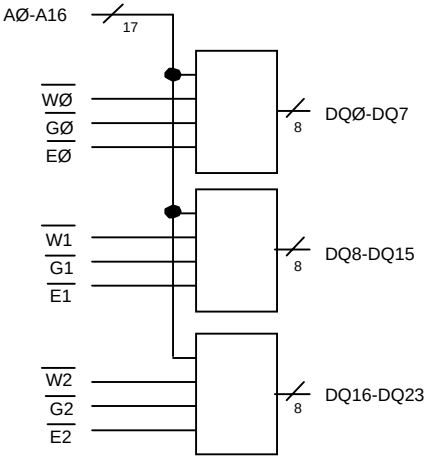
Pin Configurations and Block Diagram

128Kx24 ZIP
Module Pinout

VCC	1	2	GØ
EØ	3	4	WØ
DQØ	5	6	DQ1
DQ2	7	8	DQ3
VSS	9	10	DQ4
DQ5	11	12	DQ6
DQ7	13	14	VSS
A16	15	16	A15
A14	17	18	A13
A12	19	20	A11
G1	21	22	E1
W1	23	24	VSS
DQ8	25	26	DQ9
DQ10	27	28	DQ11
VSS	29	30	DQ12
DQ13	31	32	DQ14
DQ15	33	34	VSS
A10	35	36	A9
A8	37	38	A7
A6	39	40	VSS
A5	41	42	A4
A3	43	44	A2
A1	45	46	AØ
VSS	47	48	DQ16
DQ17	49	50	DQ18
DQ19	51	52	VSS
DQ20	53	54	DQ21
DQ22	55	56	DQ23
G2	57	58	E2
W2	59	60	VCC

Pin Names

AØ-A16	Address Inputs
EØ-E2	Chip Enables
WØ-W2	Write Enables
GØ-G2	Output Enables
DQØ-DQ23	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial.	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	4.0 Watts
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	-	450	680	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ • VIH, VIN - VIL VIN • VIH	--	25	100	mA
Full Standby Power Supply Current CMOS	ICC3	$\overline{E}$ • VCC-0.2V VIN • VCC-0.2V VIN - 0.2V	-	10	40	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±15	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2/ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Deselect Output	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Pins	CI	30	pF
Data Pins	CD/Q	15	pF
Control Pins ($\overline{E}$, $\overline{W}$, $\overline{G}$)	CC	15	pF

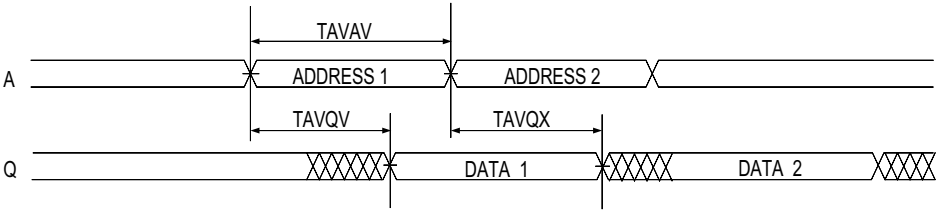
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

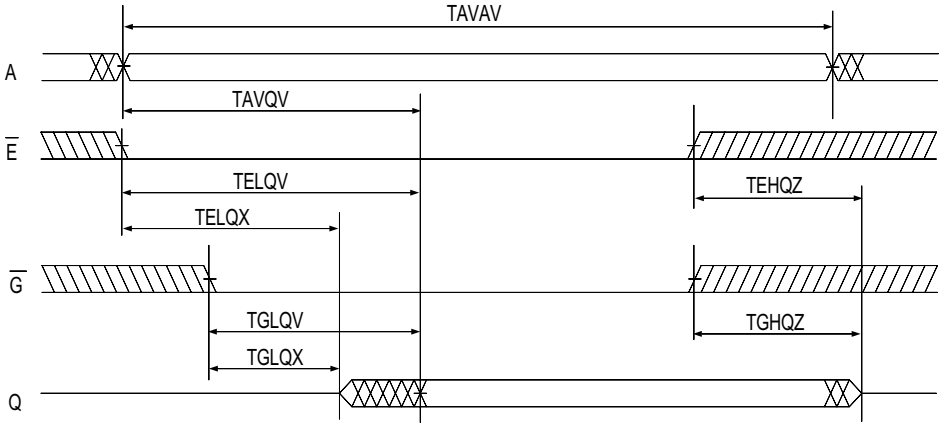
	Symbol		20ns		25ns		35ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	20		25		35		ns
Address Access Time	TAVQV	TAA		20		25		35	ns
Chip Enable Access	TELQV	TACS		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		15	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		13		15		20	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		8		10		12	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

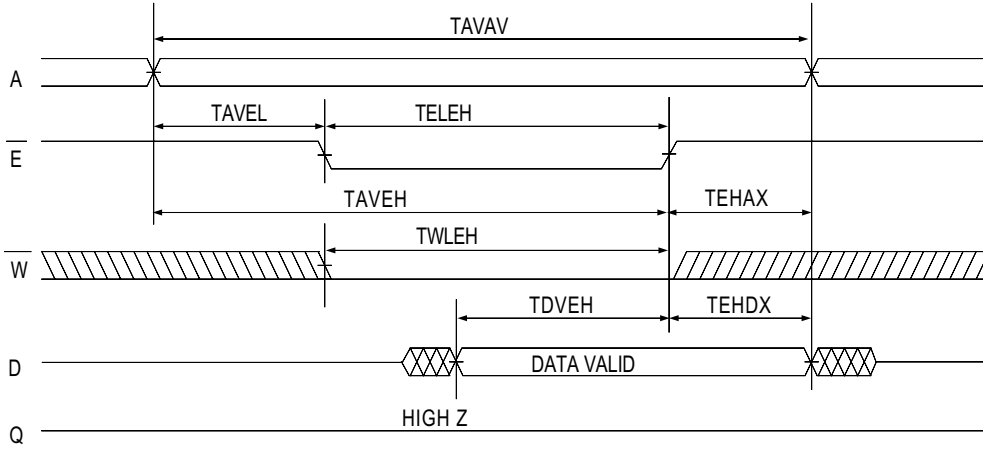


AC Characteristics Write Cycle

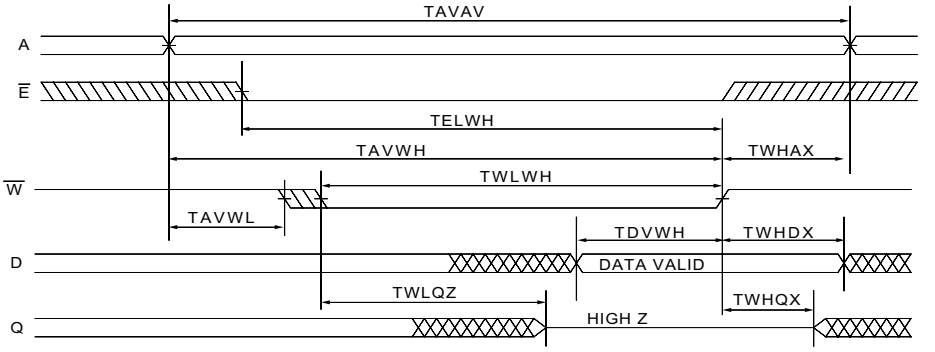
	Symbol		20ns		25ns		35ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	20		25		35		ns
Chip Enable to	TELWH	TCW	15		20		30		ns
End of Write	TWLEH	TCW	15		20		30		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to	TAVWH	TAW	15		20		30		ns
End of Write	TAVEH	TAW	15		20		30		ns
Write Pulse Width	TWLW	H TWP	15		20		25		ns
	TELEH	TWP	15		20		25		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TDH	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	12	0	15	ns
Data to Write Time	TDVWH	TDW	12		15		20		ns
	TDVEH	TDW	12		15		20		ns
Output Active from End of Write(1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled

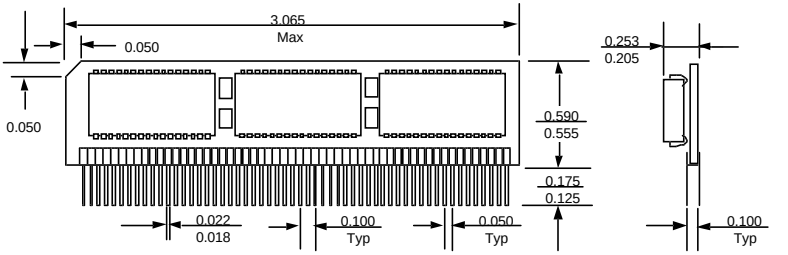


Ordering Information

Part Number	Speed (ns)	Package No.
EDI8F24128C20MZC	20	158
EDI8F24128C25MZC	25	158
EDI8F24128C35MZC	35	158

Package Description

Package No. 158
60 lead ZIP



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