Features

64Kx24 bit CMOS Static
Random Access Memory

- Access Times 15, 20, and 25ns
- Output Enable Function
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Packaging

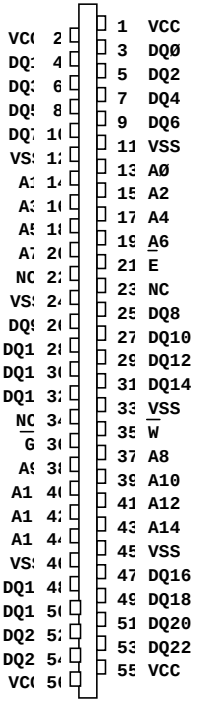
- 56 Pin ZIP, No.160
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

64Kx24 Static RAM
CMOS, High Speed Module

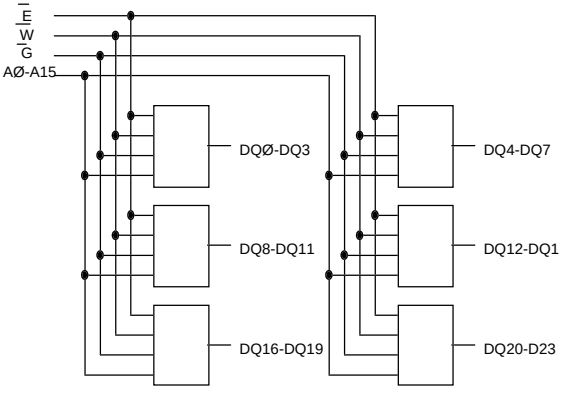
The EDI8F2464C is a high speed 1.5 megabit Static RAM module organized as 64Kx24. This module is constructed from six 64Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.
The EDI8F2464C is offered in a high density 56 lead ZIP.
All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

Pin Configurations and Block Diagram



Pin Names

A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ23	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	5.0 Watt
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL =30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{G}$, $\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	685	900	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ • VIH, VIN - VIL VIN • VIH	--	150	210	mA
Full Standby Power Supply Current CMOS	ICC3	$\overline{E}$ • VCC-0.2V VIN • VCC-0.2V or VIN - 0.2V	--	110	150	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10	µA
Output High Voltage	VOH	IOH =-4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	50	pF
Data Lines	CD/Q	20	pF
Control Lines	CC	50	pF

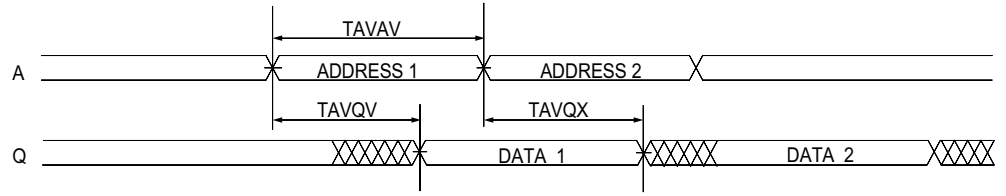
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

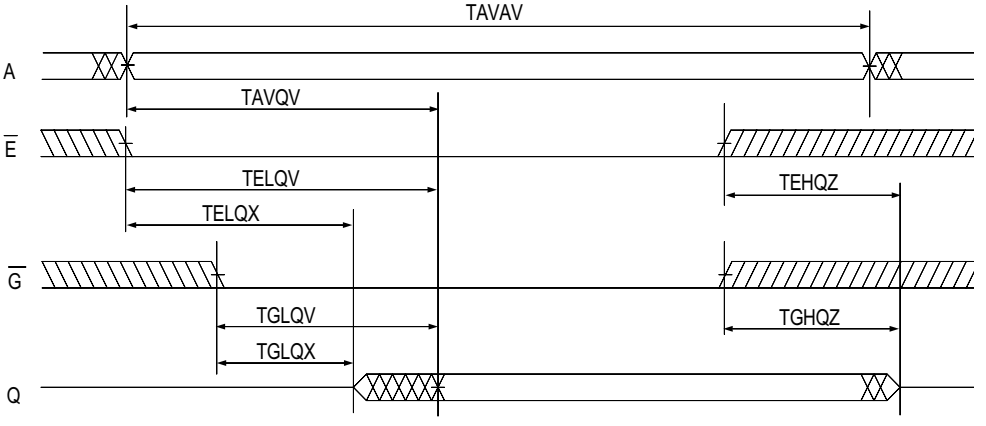
	Symbol		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	15		20		25		ns
Address Access Time	TAVQV	TAA		15		20		25	ns
Chip Enable Access Time	TELQV	TACS		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	10	0	12	0	13	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		10		12		15	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	10	0	12	0	13	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle - 2 $\overline{W}$ High

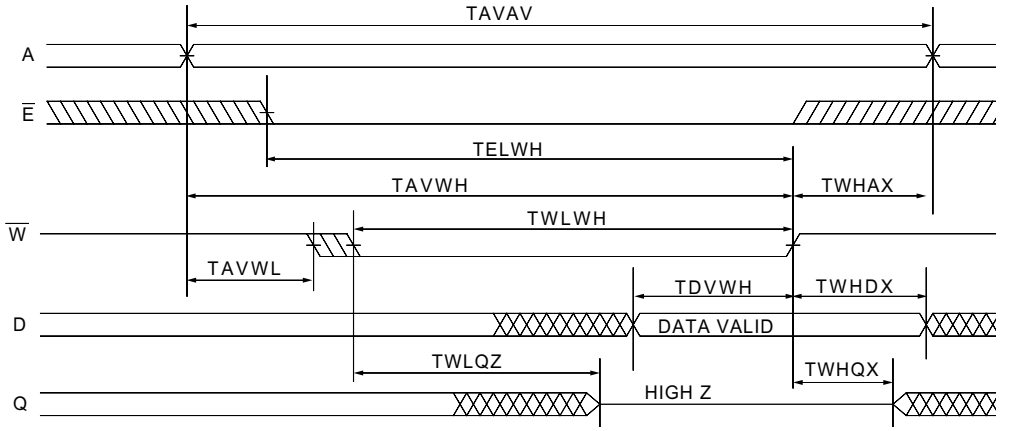


AC Characteristics Write Cycle

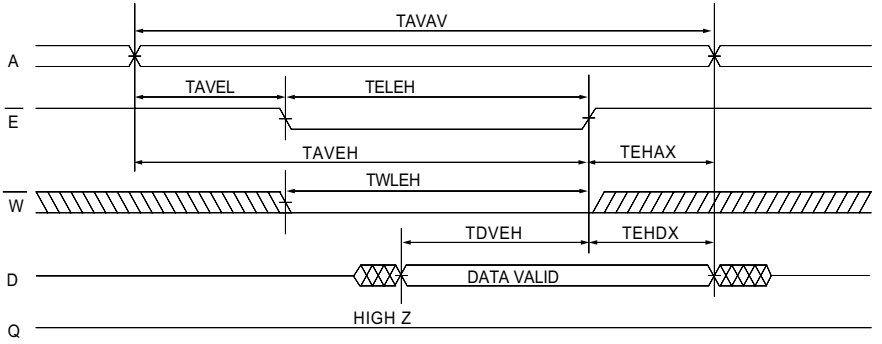
	Symbol		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	15		20		25		ns
Chip Enable to	TELWH	TCW	10		13		20		ns
End of Write	TELEH	TCW	10		13		20		ns
Address Setup Time	TAVWL	TAS	0		3		5		ns
	TAVEL	TAS	0		3		5		ns
Address Valid to	TAVWH	TAW	10		13		20		ns
End of Write	TAVEH	TAW	10		13		20		ns
Write Pulse Width	TWLWH	TWP	10		13		20		ns
	TWLEH	TWP	10		13		20		ns
Write Recovery Time	TWHAX	TWR	3		4		5		ns
	TEHAX	TWR	3		4		5		ns
Data Hold Time	TWHDX	TDH	5		5		5		ns
	TEHDX	TDH	5		5		5		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	13	0	15	0	15	ns
Data to Write Time	TDVWH	TDW	10		13		15		ns
	TDVEH	TDW	10		13		15		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled

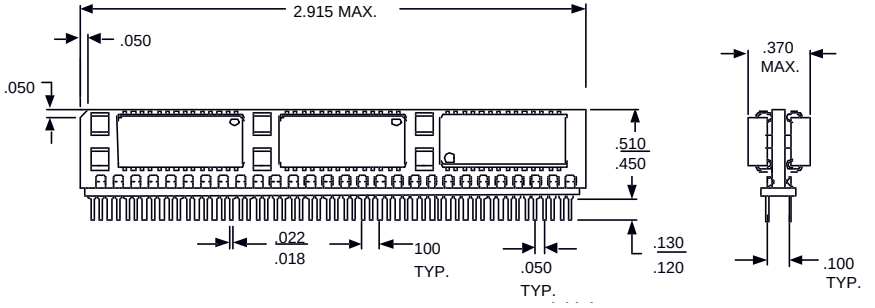


Ordering Information

Part Number	Speed (ns)	Package No.
EDI8F2464C15MZC	15	160
EDI8F2464C20MZC	20	160
EDI8F2464C25MZC	25	160

Package Description

Package No.160
56 Pin ZIP Module



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