Features

128Kx32 bit CMOS Static
Random Access Memory Array

- Fast Access Times: 15, 17, and 20
- Individual Byte Enables
- User Configurable Organization with Minimal Additional Logic
- Master Output Enable and Write Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Surface Mount Package

- 68 Lead PLCC, No. 99 (JEDEC MO-47AE)
- Small Footprint, 0.990 Sq. In.
- Multiple Ground Pins for Maximum Noise Immunity

Single +5V (±5%) Supply Operation

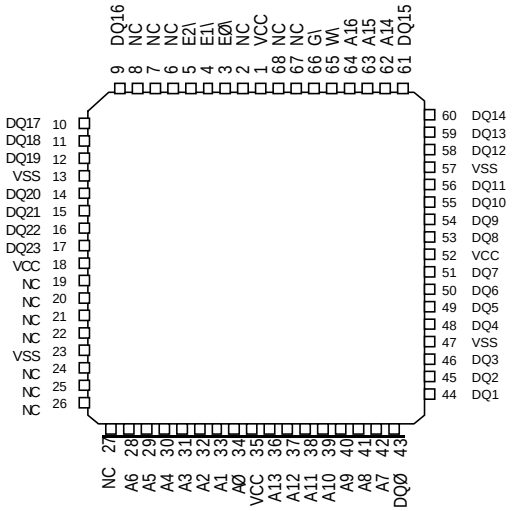
* Advance Information

128Kx24 CMOS High Speed Static RAM

The EDI8L24128C is a high speed, high performance, three megabit density Static RAM organized as a 128Kx24 bit array.
Three Chip Enables, Write Control, and Output Enable provide the user with a flexible memory solution. The user may independently enable each of the three bytes.
Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.
The EDI8L24128C, allows 3 megabits of memory to be placed in less than 0.990 square inches of board space.

Note: Solder Reflow temperature should not exceed 260°C for 10 seconds

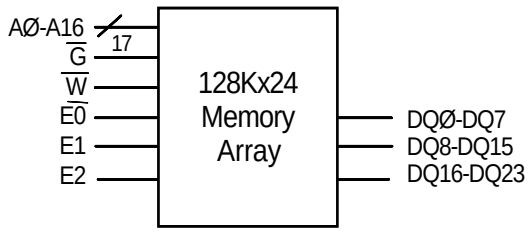
Pin Configurations and Block Diagram



Note: Pin 2 & 67 on the 64Kx24 (EDI8L2465C) and the 256Kx24 (EDI8L24256C) are word select pins.

Pin Names

AØ-A16	Address Inputs
EØ-E2	Chip Enables (One per Byte)
W	Master Write Enable
G	Master Output Enable
DQØ-DQ23	Common Data Input/Output
VCC	Power (+5V±5%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	3 Watts
Output Current.	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.75	5.0	5.25	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

Figure 1

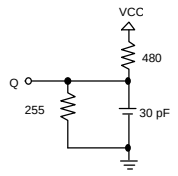
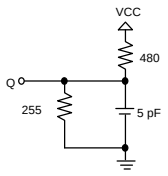


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions	Max 15	Max 17	Max 20/25	Units
Operating Power Supply Current	ICC1	$\overline{W}$= VIL, II/O = 0mA, Min Cycle	510	480	450	mA
Standby (TTL) Supply Current	ICC2	$\overline{E}$ ³ VIH, VIN£ VIL or VIN ³ VIH, f=ØMHz	120	120	120	mA
Full Standby CMOS Supply Current	ICC3	$\overline{E}$ ³VCC-0.2V VIN ³VCC-0.2V or VIN £ 0.2V	15	15	15	mA
Input Leakage Current	ILI	VIN = 0V to VCC		±10		µA
Output Leakage Current	ILO	V I/O = 0V to VCC		±10		µA
Output High Volltage	VOH	IOH = -4.0mA 2.4				V
Output Low Voltage	VOL	IOL = 8.0mA		0.4		V

* Advanced
Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2,ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CA	40	pF
Data Lines	CD/Q	10	pF
Write&OutputEnableLines	$\overline{W}$, $\overline{G}$	40	pF
Chip Enable Lines	$\overline{E}$Ø-$\overline{E}$2	8	pF

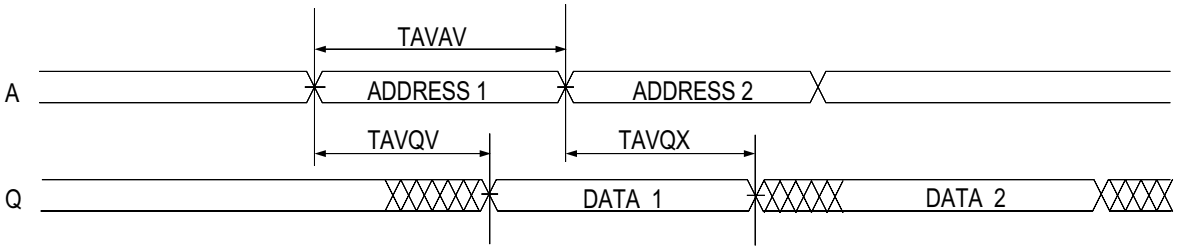
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

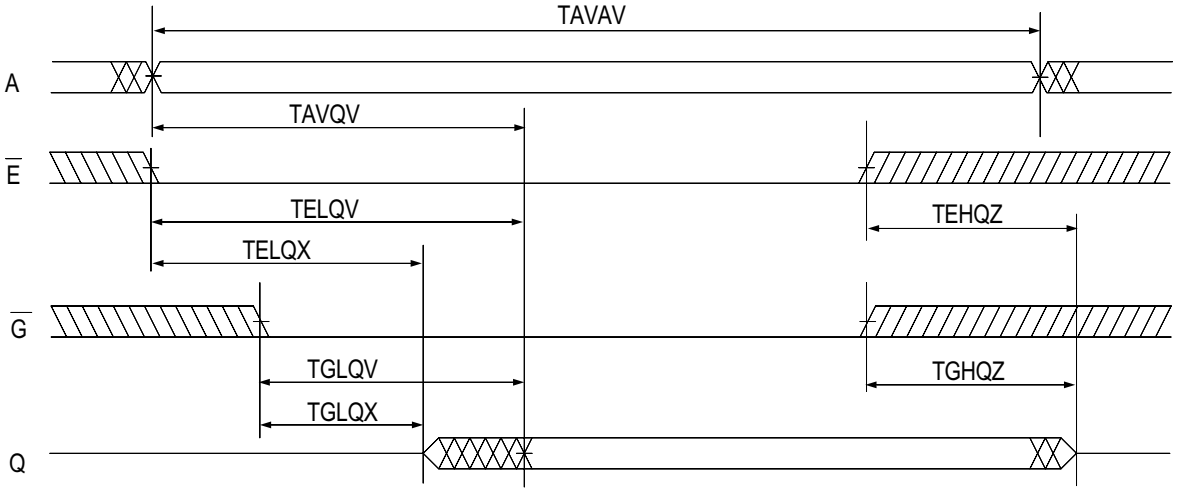
	Symbol		15ns		17ns		20ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	15		17		20		ns
Address Access Time	TAVQV	TAA		15		17		20	ns
Chip Enable Access Time	TELQV	TACS		10		17		20	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		8		8		10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		6		8		8	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	2		2		2	0	ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		5		6		8	ns

Note 1: Parameter guaranteed, but not tested. * Advance Information

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

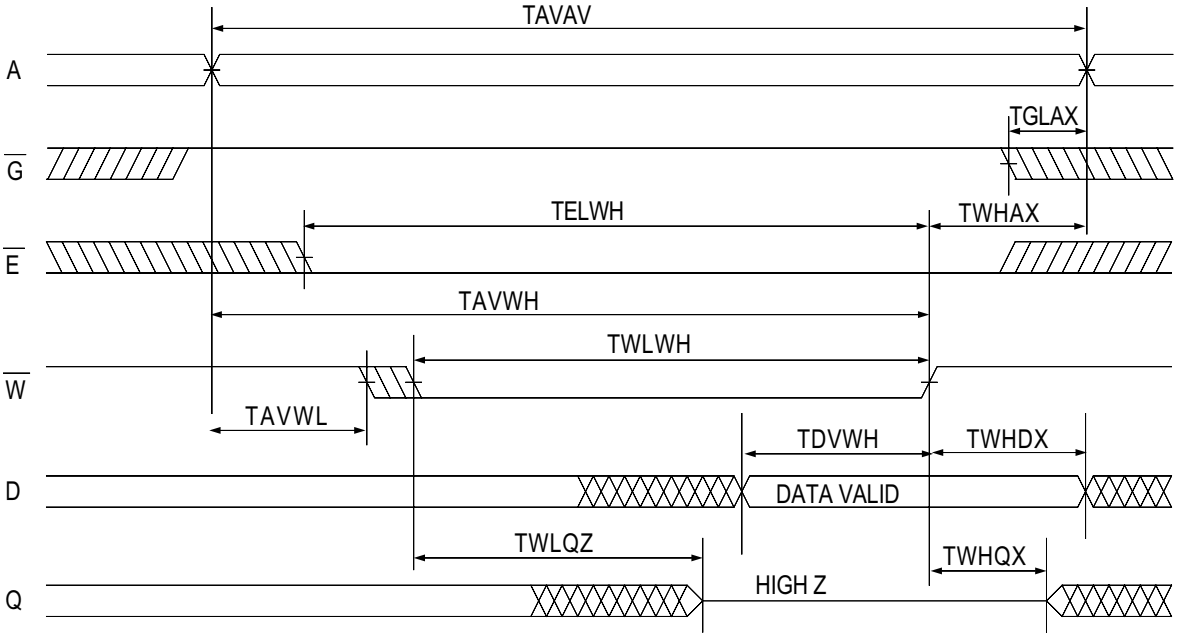


AC Characteristics Write Cycle

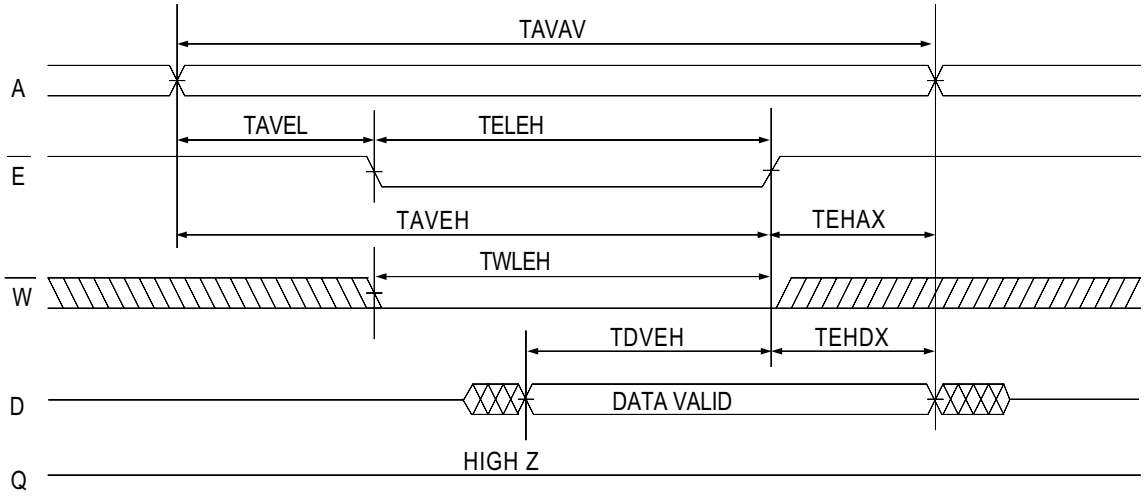
	Symbol		15ns		17ns		20ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	15		17		20		ns
Chip Enable to End of Write	TELWH	TCW	9		10		15		ns
	TELEH	TCW	9		10		15		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	10		12		15		ns
	TAVEH	TAW	10		12		15		ns
Write Pulse Width	TWLWH	TWP	10		12		15		ns
	TWLEH	TWP	10		12		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	5	0	6	0	7	0	7 ns
Data to Write Time	TDVWH	TDW	6		8		8		ns
	TDVEH	TDW	6		8		8		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		ns

Note 1: Parameter guaranteed, but not tested. *Advance Information

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\bar{E}$ Controlled



Ordering Information

Commercial (0°C to +70°C)

Part Number	Speed (ns)	Package No.
EDI8L24128C15AC	15	99
EDI8L24128C17AC	17	99
EDI8L24128C20AC	20	99

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L24128C17AI	17	99
EDI8L24128C20AI	20	99

Package Description

Package No. 99
68 Lead PLCC
JEDEC MO-47AE