128Kx8 Plastic Monolithic SRAM

FEATURES

- Fast Access Times of 15*, 17*, 20, 25ns
- 2V Data Retention (EDI88130LPS)
  - Battery Back-up Operation
- $\overline{CS}_1$, CS_2 & $\overline{OE}$ Functions for Bus Control
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks
- Industrial and Military Temperature Ranges
- Surface Mount Package
  - 32 pin Plastic SOJ (Package 7)
- Single +5V (±10%) Supply Operation

** Industrial Temperature Range Only*

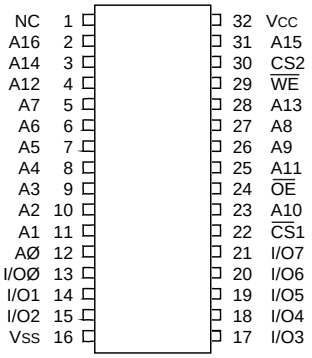
The EDI88130CS-RP is a ruggedized plastic 128Kx8 monolithic Static RAM that allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 128Kx8 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial temperature range. Using commercial test methods will not guarantee a device that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

WEDC ensures Low Power devices will retain data in Data Retention mode by characterizing the devices to determine the appropriate test conditions. This is crucial for systems operating at -40°C or below and using dense memories such as 128Kx8s. WEDC's ruggedized plastic SOJ is footprint compatible with WEDC's full military ceramic 32 pin SOJ.

FIG. 1 PIN CONFIGURATION

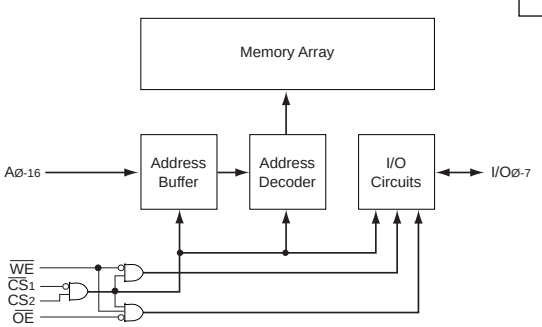
TOP VIEW



PIN DESCRIPTION

I/O_{0-7}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_1$, CS_2	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V ±10%)
V_{SS}	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.2 to 7.0	V
Operating Temperature T_A (Ambient)		
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +125	°C
Power Dissipation	1.7	W
Output Current	40	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	Vcc +0.3	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

TRUTH TABLE

$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	Mode	Output	Power
X	H	X	X	Standby	High Z	I_{CC2}, I_{CC3}
X	X	L	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	H	Output Deselect	High Z	I_{CC1}
L	L	H	H	Read	Data Out	I_{CC1}
X	L	H	L	Write	High Z	I_{CC1}

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max SOJ	Unit
Address Lines	C_I	V_{IN} = Vcc or Vss, f = 1.0MHz	8	pF
Data Lines	C_O	V_{OUT} = Vcc or Vss, f = 1.0MHz	10	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

(Typical: V_{CC} = 5V, T_A = 25°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		—	—	±5	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}, $\overline{CS_1} \geq V_{IH}$ and/or $CS_2 \leq V_{IL}$		—	—	±5	µA
Operating Power Supply Current	I_{CC1}	$\overline{WE}$, $\overline{CS_1}$ = V_{IL}, $I_{I/O}$ = 0mA, CS_2 = V_{IH}	(15-17ns)	—		300	mA
			(20-25ns)	—		225	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{CS_1} \geq V_{IH}$ and/or $CS_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$		—		35	mA
Full Standby Power Supply Current	I_{CC3}	$\overline{CS_1} \geq V_{CC}$ -0.2V and/or $CS_2 \leq 0.2V$ $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$	CS	—	—	20	mA
			LPS	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	—	—	V

AC TEST CONDITIONS

Figure 1

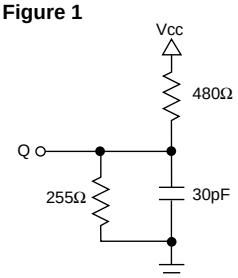
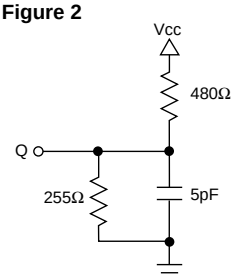


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2)

AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol JEDEC	Symbol Alt.	15ns* Min	15ns* Max	17ns* Min	17ns* Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Read Cycle Time	tAVAV	tRC	15		17		20		25		ns
Address Access Time	tAVQV	tAA		15		17		20		25	ns
Chip Select Access Time	tE1LQV tE2HQV	tACS tACS		15 15		17 17		20 20		25 25	ns ns
Chip Select to Output in Low Z (1)	tE1LQX tE2HQX	tCLZ tCLZ	5 5		5 5		5 5		5 5		ns ns
Chip Disable to Output in Low Z (1)	tE1HQZ tE2LQZ	tCHZ tCHZ		6 6		7 7		8 8		10 10	ns ns
Output Hold from Address Change	tAVQX	tOH	3		3		3		3		ns
Output Enable to Output Valid	tGLQV	tOE		6		6		7		8	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	0		0		0		0		ns
Output Disable to Output in High Z(1)	tGHQZ	tOHZ		5		6		7		9	ns
Chip Enable to Power Up (1)	tE1LICCH tE2HICCH	tPU tPU	0 0		0 0		0 0		0 0		ns ns
Chip Enable to Power Down (1)	tE1HICCL tE2LICCL	tPD tPD		15 15		17 17		20 20		25 25	ns ns

* Industrial Temperature Range Only

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

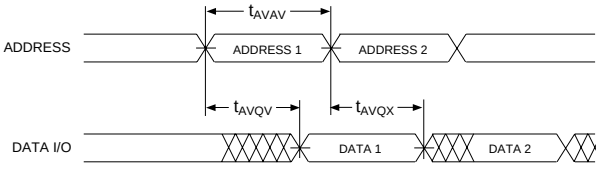
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol JEDEC	Symbol Alt.	15ns* Min	15ns* Max	17ns* Min	17ns* Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Write Cycle Time	tAVAV	tWC	15		17		20		25		ns
Chip Select to End of Write	tE1LWH tE1LE1H tE2HWH tE2HE2L	tCW tCW tCW tCW	12 12 12 12		13 13 13 13		15 15 15 15		16 16 16 16		ns ns ns ns
Address Setup Time	tAVWL tAVE1L tAVE2H	tAS tAS tAS	0 0 0		0 0 0		0 0 0		0 0 0		ns ns ns
Address Valid to End of Write	tAVWH	tAW	12		13		15		16		ns
Write Pulse Width	tWLWH tWLE1H tWLE2L	tWP tWP tWP	12 12 12		13 13 13		15 15 15		16 16 16		ns ns ns
Write Recovery Time	tWHAX tE1HAX tE2LAX	tWR tWR tWR	0 0 0		0 0 0		0 0 0		0 0 0		ns ns ns
Data Hold Time	tWHDX tE1HDX tE2LDX	tDH tDH tDH	0 0 0		0 0 0		0 0 0		0 0 0		ns ns ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	7	0	8	0	8	0	10	ns
Data to Write Time	tDVWH tDVE1H tDVE2L	tDW tDW tDW	7 7 7		8 8 8		8 8 8		10 10 10		ns ns ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		3		ns

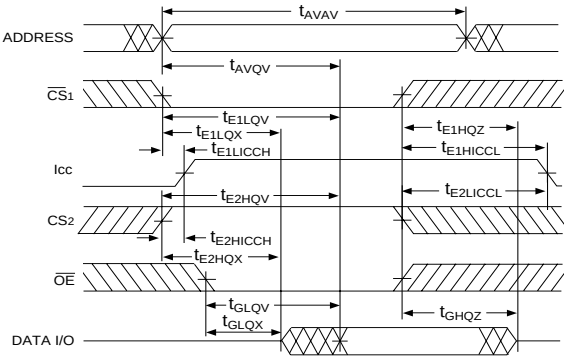
* Industrial Temperature Range Only

1. This parameter is guaranteed by design but not tested.

FIG. 2 TIMING WAVEFORM - READ CYCLES

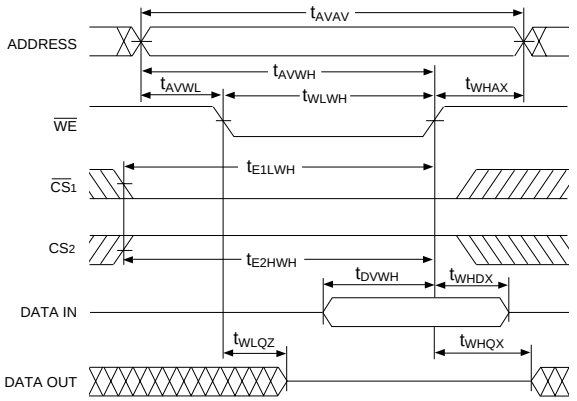


READ CYCLE 1 ($\overline{WE}$ HIGH; $\overline{OE}$, $\overline{CS}$ LOW)



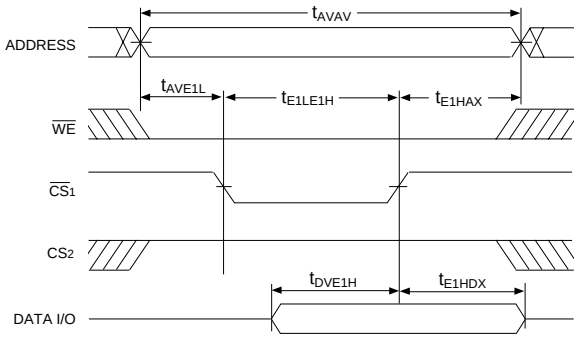
READ CYCLE 2 ($\overline{CS}$1 AND/OR CS2 CONTROLLED, $\overline{WE}$ HIGH)

FIG. 3 WRITE CYCLE 1



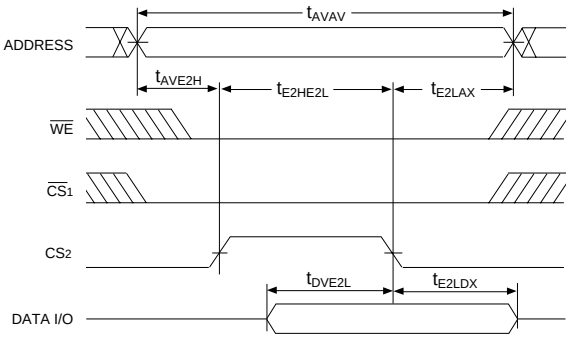
WRITE CYCLE 1 - LATE WRITE, $\overline{WE}$ CONTROLLED

FIG. 4 WRITE CYCLES 2



WRITE CYCLE 2 - EARLY WRITE, $\overline{CS}$1 CONTROLLED

WRITE CYCLES 3



WRITE CYCLE 3 - EARLY WRITE, CS2 CONTROLLED

DATA RETENTION CHARACTERISTICS (EDI88130LPS ONLY)

(T_A = -55°C to +125°C)

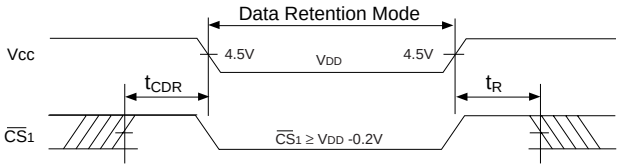
Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{DD}	V_{DD} = 2.0V	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	$\overline{CS_1} \geq V_{DD}$ -0.2V and/or $CS_2 \geq V_{SS}$ +0.2V	–	0.5	3	mA
Chip Disable to Data Retention Time (1)	T_{CDR}	$V_{IN} \geq V_{DD}$ -0.2V	0	–	–	ns
Operation Recovery Time (1)	T_R	or $V_{IN} \leq$ 0.2V	T_{AVAV}*	–	–	ns

NOTE:

1. Parameter guaranteed by design, but not tested.

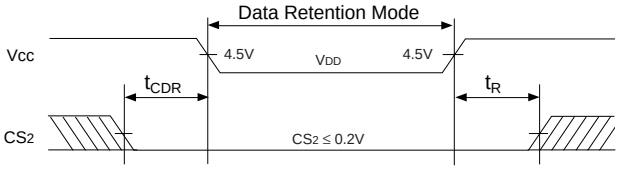
* Read Cycle Time

FIG. 5
DATA RETENTION - $\overline{CS_1}$ CONTROLLED



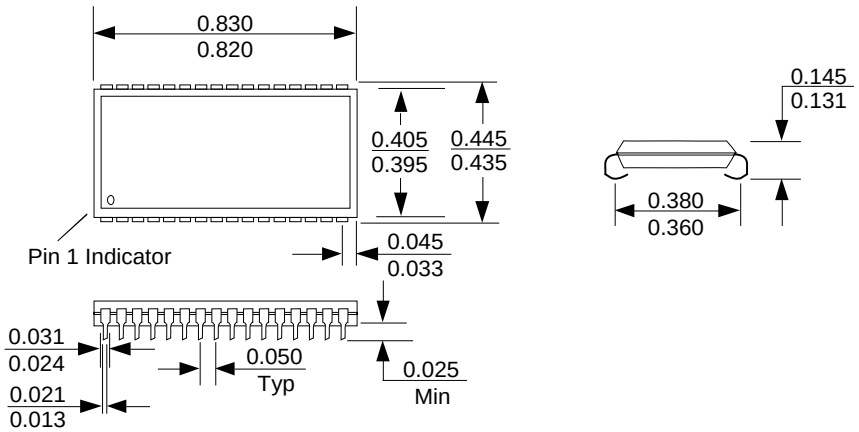
DATA RETENTION, $\overline{CS_1}$ CONTROLLED

FIG. 6
DATA RETENTION - CS_2 CONTROLLED



DATA RETENTION, CS_2 CONTROLLED

PACKAGE 7: 32 PIN PLASTIC SOJ



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 130 CS X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 128Kx8
(130 = Dual Chip Select)

TECHNOLOGY:
CS = CMOS Standard Power (5V)
LPS = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
M = 32 pin Plasticic SOJ (Package 7)

DEVICE GRADE:

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C