512Kx8 Plastic Monolithic 3.3V SRAM CMOS

FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times of 15, 17, 20, 25ns
  - Extended Temperature Testing
- 36 lead JEDEC Approved Revolutionary Pinout
  - Plastic SOJ (Package 319)
- Single +3.3V (±10%) Supply Operation

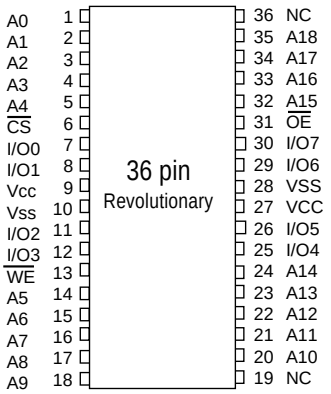
WEDC's ruggedized plastic 512Kx8 SRAM that allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 512Kx8 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of a device change when it is operated beyond the commercial temperature range. Using commercial methods will not guarantee a devicee that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

WEDC's ruggedized plastic SOJ is footprint compatible with WEDC's full military ceramic 36 pin SOJ.

FIG. 1 PIN CONFIGURATION

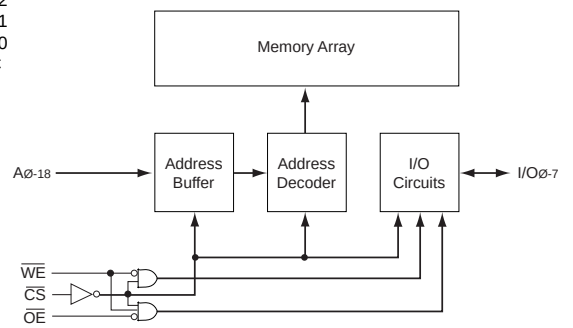
TOP VIEW



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
Vcc	Power (+3.3V)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature T_A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +125	°C
Power Dissipation	0.55	W
Output Current	20	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

$\overline{OE}$	$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
X	H	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	Output Deselect	High Z	I_{CC1}
L	L	H	Read	Data Out	I_{CC1}
X	L	L	Write	Data In	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	Vcc +0.3	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Address Lines	C_I	V_{IN} = Vcc or Vss, f = 1.0MHz	7	pF
Data Lines	C_O	V_{IN} = Vcc or Vss, f = 1.0MHz	8	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

(V_{CC} = 5V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	-2	2	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}	-2	2	µA
Operating Power Supply Current	I_{CC1}	$\overline{WE}$, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle (15ns)	—	170	mA
		(20-55ns)	—	160	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{CS} \geq V_{IH}$, $V_{IN} \leq V_{IL}$, $V_{IN} \geq V_{IH}$	—	50	mA
Full Standby Power Supply Current	I_{CC3}	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq$ Vcc -0.2V or $V_{IN} \leq$ 0.2V	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	—	V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc -0.3V

AC TEST CONDITIONS

Figure 1

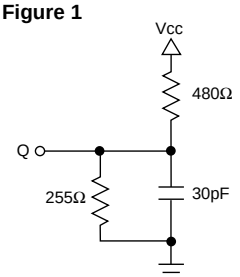
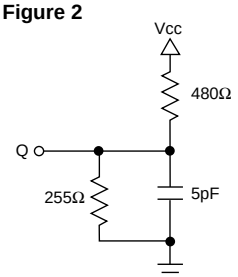


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2)

AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol JEDEC	Symbol Alt.	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Read Cycle Time	tAVAV	tRC	15		17		20		25		ns
Address Access Time	tAVQV	tAA		15		17		20		25	ns
Chip Enable Access Time	tELQV	tACS		15		17		20		25	ns
Chip Enable to Output in Low Z (1)	tELQX	tCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ	0	7	0	7	0	8	0	10	ns
Output Hold from Address Change	tAVQX	tOH	0		0		0		0		ns
Output Enable to Output Valid	tGLQV	tOE		7		8		10		12	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	0		0		0		0		ns
Output Disable to Output in High Z(1)	tGHQZ	tOHZ	0	7	0	7	0	8	0	10	ns

1. This parameter is guaranteed by design but not tested.

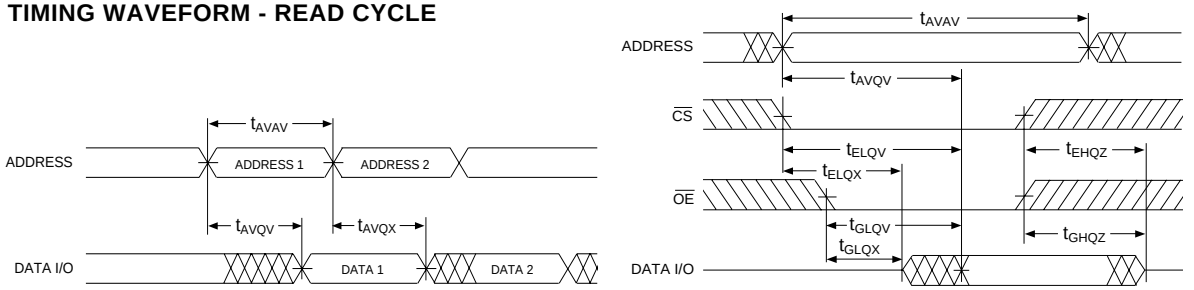
AC CHARACTERISTICS – WRITE CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol JEDEC	Symbol Alt.	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Write Cycle Time	tAVAV	tWC	15		17		20		25		ns
Chip Enable to End of Write	tELWH tELEH	tCW tCW	13 13		14 14		15 15		17 17		ns ns
Address Setup Time	tAVWL tAVEL	tAS tAS	0 0		0 0		0 0		0 0		ns ns
Address Valid to End of Write	tAVWH tAVEH	tAW tAW	12 12		14 14		15 15		17 17		ns ns
Write Pulse Width	tWLWH tWLEH	tWP tWP	12 12		14 14		15 15		17 17		ns ns
Write Recovery Time	tWHAX tEHAX	tWR tWR	0 0		0 0		0 0		0 0		ns ns
Data Hold Time	tWHDX tEHDX	tDH tDH	0 0		0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	7	0	8	0	8	0	10	ns
Data to Write Time	tDVWH tDVEH	tDW tDW	8 8		8 8		10 10		12 12		ns ns
Output Active from End of Write (1)	tWHQX	tWLZ	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

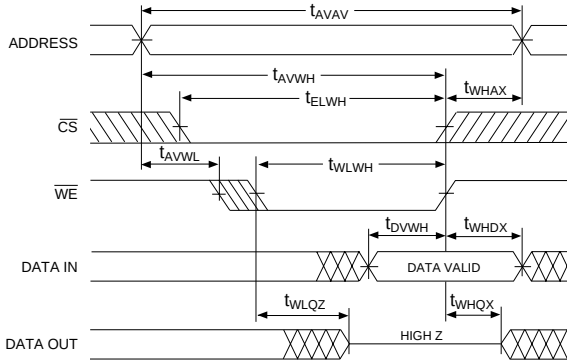
FIG. 2
TIMING WAVEFORM - READ CYCLE



READ CYCLE 1 ($\overline{WE}$ HIGH; $\overline{OE}$, $\overline{CS}$ LOW)

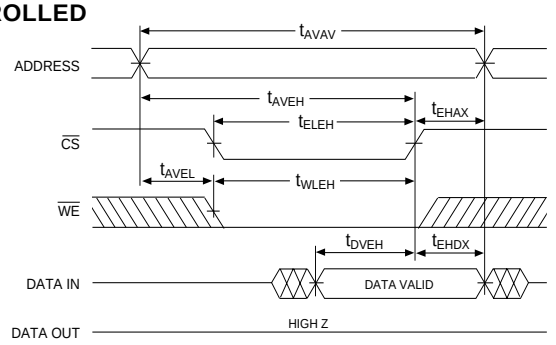
READ CYCLE 2 ($\overline{WE}$ HIGH)

FIG. 3
WRITE CYCLE - $\overline{WE}$ CONTROLLED



WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

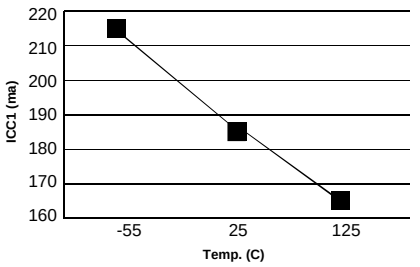
FIG. 4
WRITE CYCLE - $\overline{CS}$ CONTROLLED



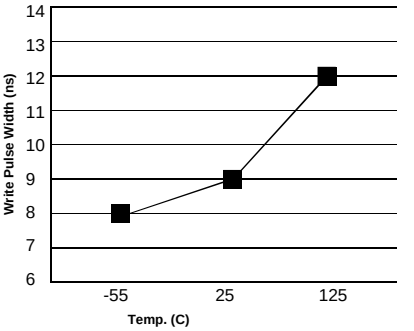
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

FIG. 5
NORMALIZED OPERATING GRAPHS

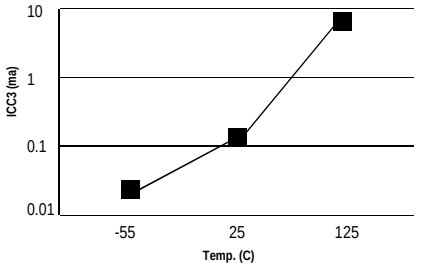
ICC1 (20ns) vs Temp



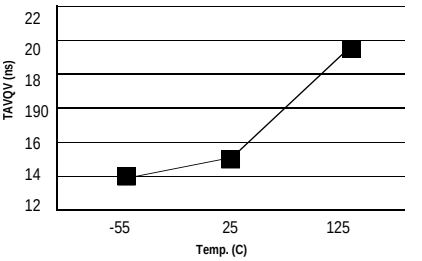
Write Pulse Width vs. Temp.



ICC3 vs. Temp

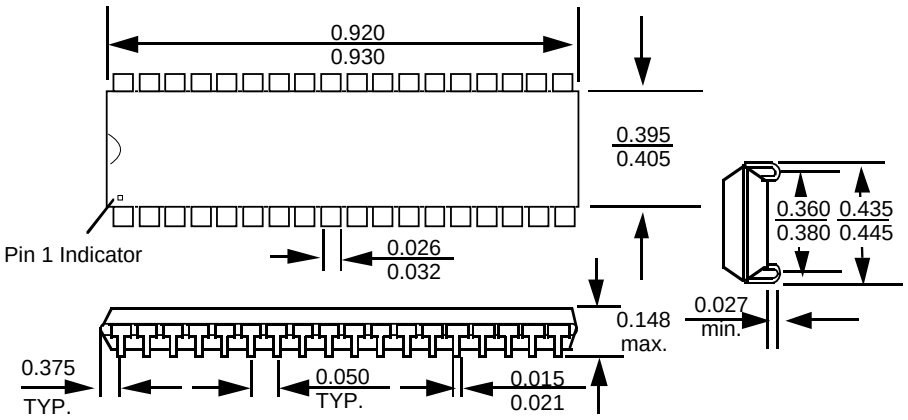


TAVQV vs. Temp



Normalized curves are offered as a service to our customers. They are not to be construed as a guarantee of operating characterics. Characteristics of actual devices will vary.

PACKAGE 319: 36 LEAD, PLASTIC SMALL OUTLINE J-LEAD (SOJ)



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 512 VA X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 512Kx8

TECHNOLOGY:
VA = 3.3V CMOS Standard Power

ACCESS TIME (ns)

PACKAGE TYPE:
M = 36 lead Plastic SOJ

DEVICE GRADE:

B = MIL-STD-883 Compliant	
M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C