



## 512Kx8 Plastic Monolithic SRAM CMOS

### FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times of 17, 20, 25ns
  - Data Retention Function (LPA version)
  - Extended Temperature Testing
  - Data Retention Functionality Testing
- 36 lead JEDEC Approved Revolutionary Pinout
  - Plastic SOJ (Package 319)
- Single +5V ( $\pm 10\%$ ) Supply Operation

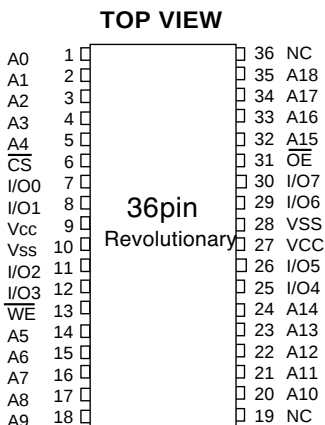
WEDC's ruggedized plastic 512Kx8 SRAM that allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 512Kx8 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial guarantee a device that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

WEDC ensures Low Power devices will retain data in Data Retention mode by characterizing the devices to determine the appropriate test conditions. This is crucial for systems operating at  $-40^{\circ}\text{C}$  or below and using dense memories such as 512Kx8s.

WEDC's ruggedized plastic SOJ is footprint compatible with WEDC's full military ceramic 36 pin SOJ.

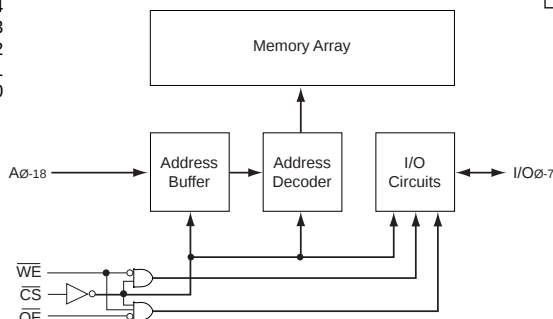
FIG. 1 PIN CONFIGURATION

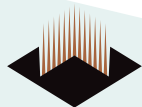


PIN DESCRIPTION

|        |                         |
|--------|-------------------------|
| I/O0-7 | Data Inputs/Outputs     |
| A0-18  | Address Inputs          |
| WE     | Write Enables           |
| CS     | Chip Selects            |
| OE     | Output Enable           |
| Vcc    | Power (+5V $\pm 10\%$ ) |
| Vss    | Ground                  |
| NC     | Not Connected           |

BLOCK DIAGRAM





### ABSOLUTE MAXIMUM RATINGS

| Parameter                                      |             | Unit |
|------------------------------------------------|-------------|------|
| Voltage on any pin relative to Vss             | -0.5 to 7.0 | V    |
| Operating Temperature T <sub>A</sub> (Ambient) |             |      |
| Commercial                                     | 0 to +70    | °C   |
| Industrial                                     | -40 to +85  | °C   |
| Military                                       | -55 to +125 | °C   |
| Storage Temperature, Plastic                   | -65 to +150 | °C   |
| Power Dissipation                              | 1.5         | W    |
| Output Current                                 | 20          | mA   |
| Junction Temperature, T <sub>J</sub>           | 175         | °C   |

#### NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### CAPACITANCE

(T<sub>A</sub> = +25°C)

| Parameter     | Symbol         | Condition                                                         | Max | Unit |
|---------------|----------------|-------------------------------------------------------------------|-----|------|
| Address Lines | C <sub>I</sub> | V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub> , f = 1.0MHz | 6   | pF   |
| Data Lines    | C <sub>O</sub> | V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub> , f = 1.0MHz | 8   | pF   |

These parameters are sampled, not 100% tested.

### DC CHARACTERISTICS

(V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

| Parameter                | Symbol          | Conditions                                                                                                                    | Min | Max | Units |
|--------------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------|-----|-----|-------|
| Input Leakage Current    | I <sub>LI</sub> | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>                                                   |     | 10  | μA    |
| Output Leakage Current   | I <sub>LO</sub> | $\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub> |     | 10  | μA    |
| Operating Supply Current | I <sub>CC</sub> | $\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5                       |     | 180 | mA    |
| Standby Current          | I <sub>SB</sub> | $\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5                       |     | 15  | mA    |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5                                                                               | 2.4 |     | V     |
| Output Low Voltage       | V <sub>OL</sub> | I <sub>OL</sub> = 8.0mA, V <sub>CC</sub> = 4.5                                                                                |     | 0.4 | V     |

NOTE: DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V

### AC TEST CONDITIONS

Figure 1

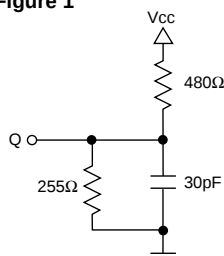
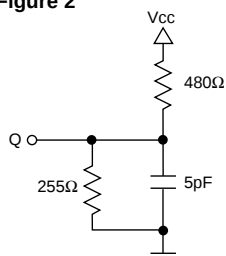


Figure 2



|                                |                         |
|--------------------------------|-------------------------|
| Input Pulse Levels             | V <sub>SS</sub> to 3.0V |
| Input Rise and Fall Times      | 5ns                     |
| Input and Output Timing Levels | 1.5V                    |
| Output Load                    | Figure 1                |

NOTE: For t<sub>EHZ</sub>, t<sub>SHZ</sub> and t<sub>WLOZ</sub>, C<sub>L</sub> = 5pF (Figure 2)



### AC CHARACTERISTICS – READ CYCLE

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0°C to +70°C)

| Parameter                             | Symbol |      | 17ns |     | 20ns |     | 25ns |     | Units |
|---------------------------------------|--------|------|------|-----|------|-----|------|-----|-------|
|                                       | JEDEC  | Alt. | Min  | Max | Min  | Max | Min  | Max |       |
| Read Cycle Time                       | tAVAV  | tRC  | 17   |     | 20   |     | 25   |     | ns    |
| Address Access Time                   | tAVQV  | tAA  |      | 17  |      | 20  |      | 25  | ns    |
| Chip Enable Access Time               | tELQV  | tACS |      | 17  |      | 20  |      | 25  | ns    |
| Chip Enable to Output in Low Z (1)    | tELQX  | tCLZ | 3    |     | 3    |     | 3    |     | ns    |
| Chip Disable to Output in High Z (1)  | tEHQZ  | tCHZ | 0    | 7   | 0    | 8   | 0    | 10  | ns    |
| Output Hold from Address Change       | tAVQX  | tOH  | 0    |     | 0    |     | 0    |     | ns    |
| Output Enable to Output Valid         | tGLQV  | tOE  |      | 8   |      | 10  |      | 12  | ns    |
| Output Enable to Output in Low Z (1)  | tGLQX  | tOLZ | 0    |     | 0    |     | 0    |     | ns    |
| Output Disable to Output in High Z(1) | tGHQZ  | tOHZ | 0    | 7   | 0    | 8   | 0    | 10  | ns    |

1. This parameter is guaranteed by design but not tested.

### AC CHARACTERISTICS – WRITE CYCLE

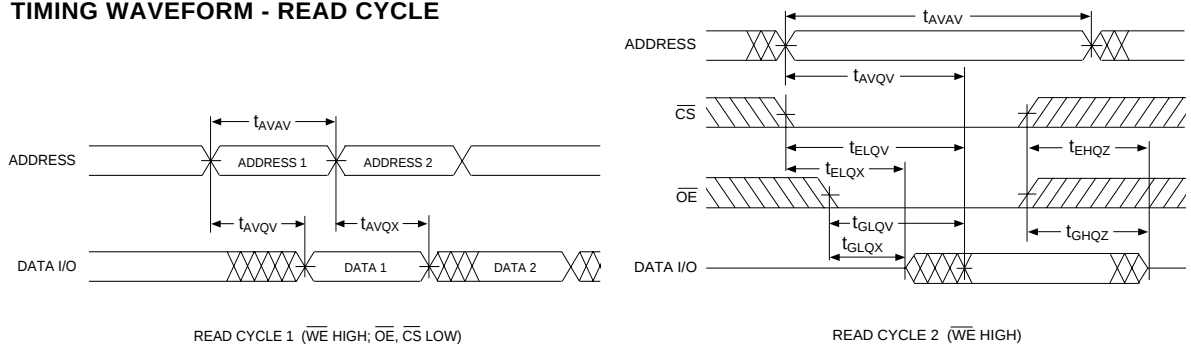
(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0°C to +70°C)

| Parameter                           | Symbol |      | 17ns |     | 20ns |     | 25ns |     | Units |
|-------------------------------------|--------|------|------|-----|------|-----|------|-----|-------|
|                                     | JEDEC  | Alt. | Min  | Max | Min  | Max | Min  | Max |       |
| Write Cycle Time                    | tAVAV  | tWC  | 17   |     | 20   |     | 25   |     | ns    |
| Chip Enable to End of Write         | tELWH  | tCW  | 14   |     | 15   |     | 17   |     | ns    |
|                                     | tELEH  | tCW  | 14   |     | 15   |     | 17   |     | ns    |
| Address Setup Time                  | tAVWL  | tAS  | 0    |     | 0    |     | 0    |     | ns    |
|                                     | tAVEL  | tAS  | 0    |     | 0    |     | 0    |     | ns    |
| Address Valid to End of Write       | tAVWH  | tAW  | 14   |     | 15   |     | 17   |     | ns    |
|                                     | tAVEH  | tAW  | 14   |     | 15   |     | 17   |     | ns    |
| Write Pulse Width                   | tWLWH  | tWP  | 14   |     | 15   |     | 17   |     | ns    |
|                                     | tWLEH  | tWP  | 14   |     | 15   |     | 17   |     | ns    |
| Write Recovery Time                 | tWHAX  | tWR  | 0    |     | 0    |     | 0    |     | ns    |
|                                     | tEHAX  | tWR  | 0    |     | 0    |     | 0    |     | ns    |
| Data Hold Time                      | tWHDX  | tDH  | 0    |     | 0    |     | 0    |     | ns    |
|                                     | tEHDX  | tDH  | 0    |     | 0    |     | 0    |     | ns    |
| Write to Output in High Z (1)       | tWLQZ  | tWHZ | 0    | 8   | 0    | 8   | 0    | 10  | ns    |
| Data to Write Time                  | tDVWH  | tDW  | 8    |     | 10   |     | 12   |     | ns    |
|                                     | tDVEH  | tDW  | 8    |     | 10   |     | 12   |     | ns    |
| Output Active from End of Write (1) | tWHQX  | tWLZ | 0    |     | 0    |     | 0    |     | ns    |

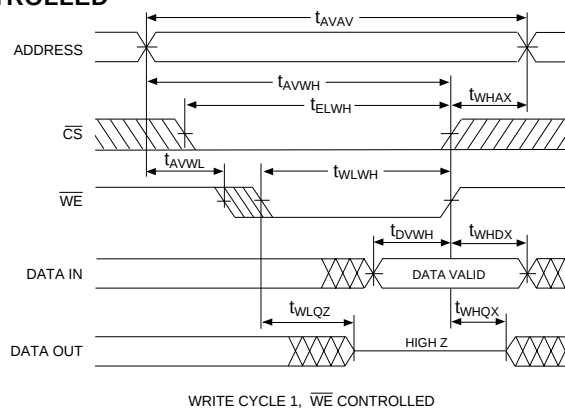
1. This parameter is guaranteed by design but not tested.



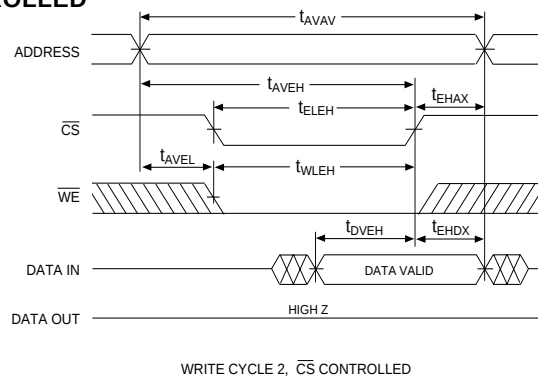
**FIG. 2**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 3**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**



**FIG. 4**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**



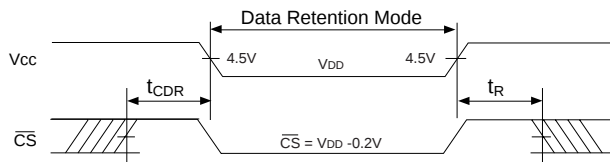


### DATA RETENTION CHARACTERISTICS (EDI88512LPA ONLY)

(TA = -55°C to +125°C)

| Characteristic<br>Low Power Version only | Sym               | Conditions                               | Min               | Typ | Max | Units |
|------------------------------------------|-------------------|------------------------------------------|-------------------|-----|-----|-------|
| Data Retention Voltage                   | V <sub>DD</sub>   | V <sub>DD</sub> = 2.0V                   | 2                 | –   | –   | V     |
| Data Retention Quiescent Current         | I <sub>CCDR</sub> | $\overline{CS} \geq V_{DD} - 0.2V$       | –                 | –   | 2   | mA    |
| Chip Disable to Data Retention Time      | T <sub>CDR</sub>  | V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V | 0                 | –   | –   | ns    |
| Operation Recovery Time                  | T <sub>R</sub>    | or V <sub>IN</sub> ≤ 0.2V                | T <sub>AVAV</sub> | –   | –   | ns    |

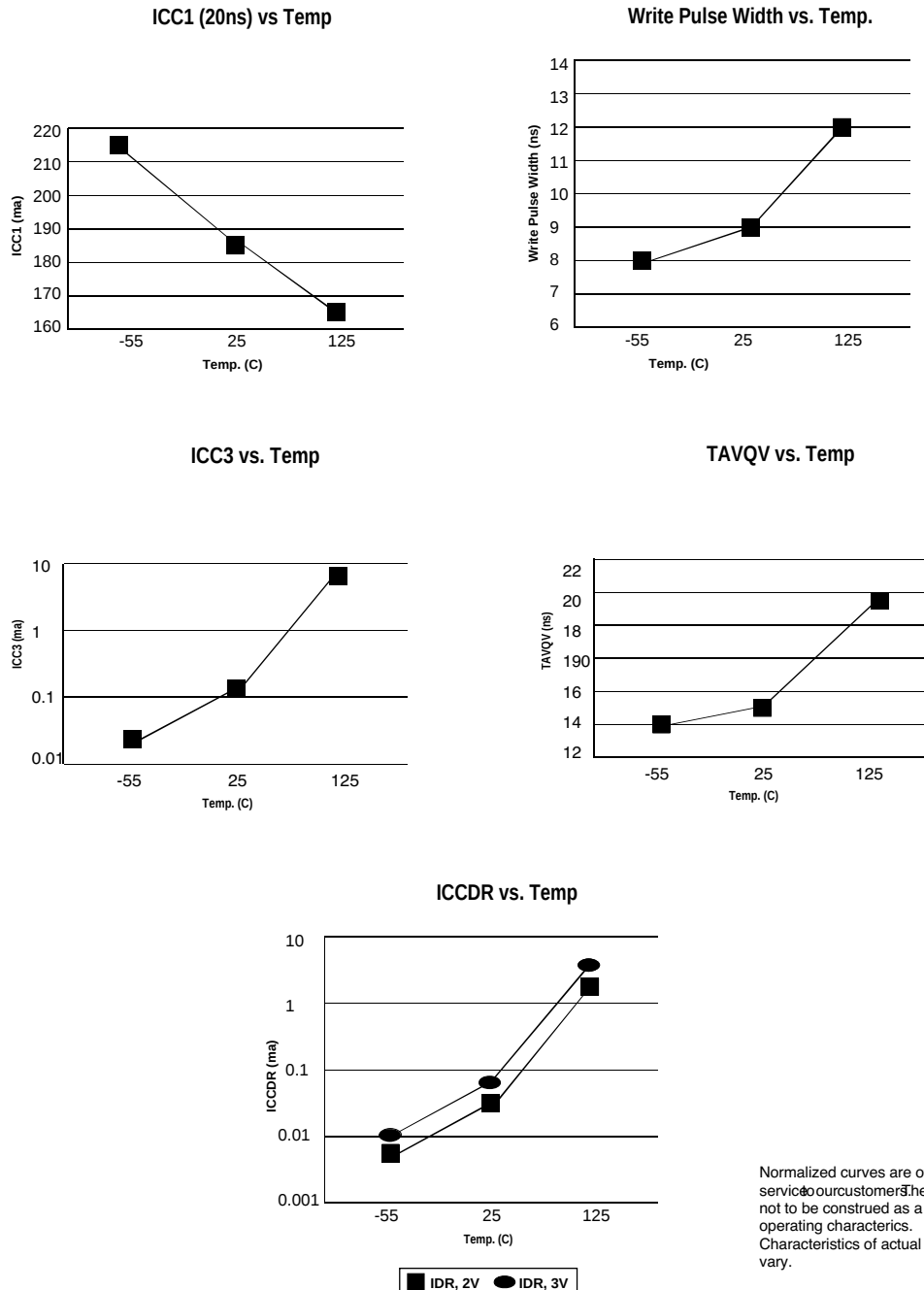
**FIG. 5**  
**DATA RETENTION -  $\overline{CS}$  CONTROLLED**



DATA RETENTION,  $\overline{CS}$  CONTROLLED

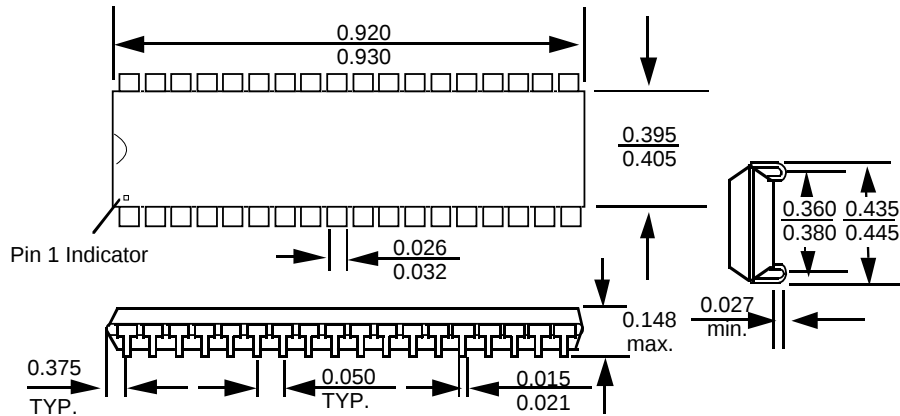


**FIG. 6**  
**NORMALIZED OPERATING GRAPHS**





### PACKAGE 319: 36 LEAD, PLASTIC SMALL OUTLINE J-LEAD (SOJ)



ALL DIMENSIONS ARE IN INCHES

### ORDERING INFORMATION

**EDI 8 8 512 CA X X X**

**WHITE ELECTRONIC DESIGNS** \_\_\_\_\_

**SRAM** \_\_\_\_\_

**ORGANIZATION, 512Kx8** \_\_\_\_\_

**TECHNOLOGY:** \_\_\_\_\_  
CA = CMOS Standard Power  
LPA = Low Power

**ACCESS TIME (ns)** \_\_\_\_\_

**PACKAGE TYPE:** \_\_\_\_\_  
M = 36 lead Plastic SOJ

**DEVICE GRADE:** \_\_\_\_\_  
B = MIL-STD-883 Compliant  
M = Military Screened      -55°C to +125°C  
I = Industrial                -40°C to +85°C  
C = Commercial              0°C to +70°C