



128Kx8 Plastic Monolithic 3.3V SRAM

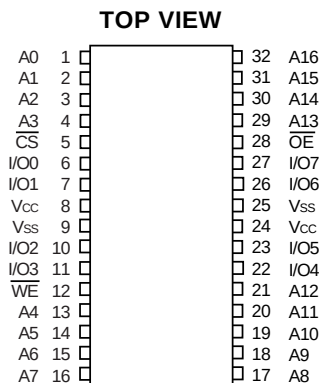
FEATURES

- Access Times of 15, 20, 25ns
- TTL Compatible Inputs and Outputs
- Fully Static Operation
- Center Power and Ground Pins
- Industrial and Military Temperature Ranges
- JEDEC Approved Revolutionary Pinout
 - 32 pin Plastic SOJ (Package 7)
- Single +3.3V ($\pm 10\%$) Supply Operation

WEDC's ruggedized plastic 128Kx8 SRAM allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 128Kx8 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial temperature range. Using commercial test methods will not guarantee a device that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

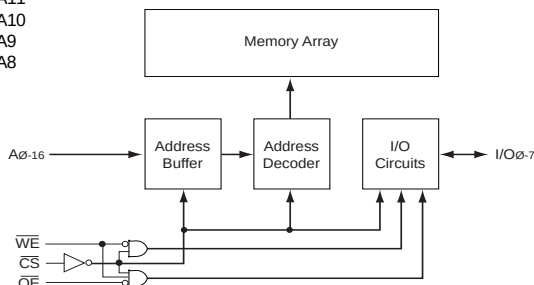
FIG. 1 PIN CONFIGURATION

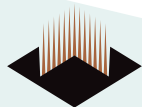


PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
Vcc	Power (+3.3V $\pm 10\%$)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 4.6	V
Operating Temperature TA (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +125	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{OE}$	$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.2	—	6.0	V
Input Low Voltage	VIL	-0.3	—	+0.8	V

CAPACITANCE

(TA = +25°C)

Parameter	Symbol	Condition	Max	Unit
Address Lines	CI	VIN = Vcc or Vss, f = 1.0MHz	6	pF
Data Lines	Co	VOU = Vcc or Vss, f = 1.0MHz	8	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

(Vcc = 5V, TA = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	ILI	VIN = 0V to Vcc	-10	+10	μA
Output Leakage Current	ILO	VIO = 0V to Vcc	-10	+10	μA
Operating Power Supply Current	Icc1	$\overline{WE}$, $\overline{CS}$ = VIL, IIO = 0mA, Min Cycle	—	170	mA
Standby (TTL) Power Supply Current	Icc2	$\overline{CS} \geq V_{IH}$, VIN ≤ VIL, VIN ≥ VIH	—	30	mA
Full Standby Power Supply Current	Icc3	$\overline{CS} \geq V_{cc} - 0.2V$ VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V	—	10	mA
Output Low Voltage	VOL	IOL = 8.0mA	—	0.4	V
Output High Voltage	VOH	IOH = -4.0mA	2.4	—	V

NOTE: DC test conditions: VIL = 0.3V, VIH = Vcc - 0.3V



AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	15		20		25		ns
Address Access Time	t _{AVQV}	t _{AA}		15		20		25	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		15		20		25	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	3		3		3		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		7		8		10	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		ns
Output Disable to Output in High Z (1)	t _{GHQZ}	t _{OHZ}	0	7	0	8	0	10	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	15		20		25		ns
Chip Enable to End of Write	t _{ELWH}	t _{CW}	10		12		17		ns
	t _{ELEH}	t _{CW}	10		12		17		ns
Address Setup Time	t _{AWWL}	t _{AS}	0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		ns
Address Valid to End of Write	t _{AWWH}	t _{AW}	10		12		17		ns
	t _{AVEH}	t _{AW}	10		12		17		ns
Write Pulse Width	t _{WLWH}	t _{WP}	10		12		17		ns
	t _{WLEH}	t _{WP}	10		12		17		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		ns
	t _{EHAX}	t _{WR}	0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
	t _{EHDX}	t _{DH}	0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	7	0	8	0	10	ns
Data to Write Time	t _{DVWH}	t _{DW}	7		10		12		ns
	t _{DVEH}	t _{DW}	7		10		12		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CONDITIONS

Figure 1

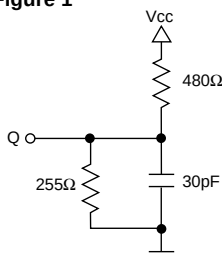
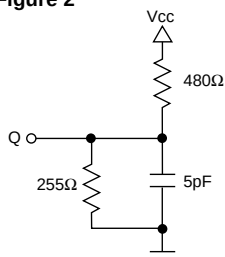


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2)



FIG. 2
TIMING WAVEFORM - READ CYCLE

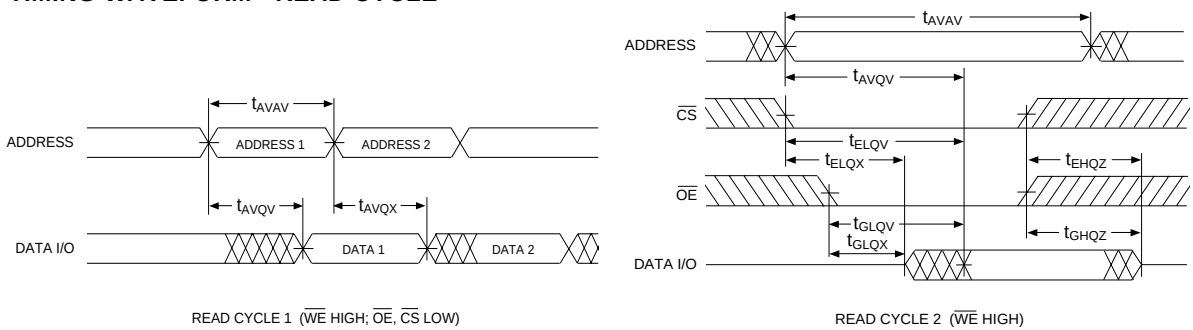


FIG. 3
WRITE CYCLE - $\overline{WE}$ CONTROLLED

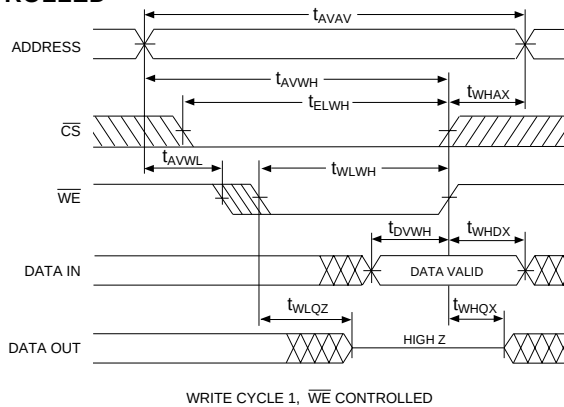
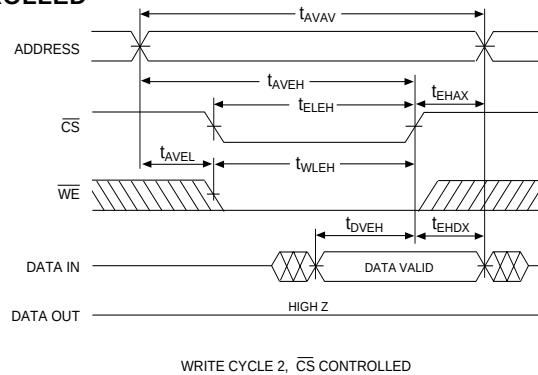
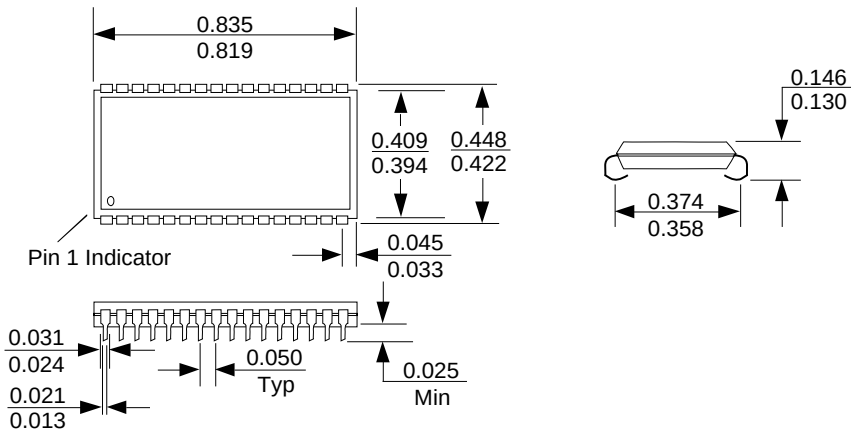


FIG. 4
WRITE CYCLE - $\overline{CS}$ CONTROLLED





PACKAGE 7: 32 PIN PLASTIC SOJ



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 128 V X X X

WHITE ELECTRONIC DESIGNS —————

SRAM —————

ORGANIZATION, 128Kx8 —————

3.3V POWER SUPPLY —————

ACCESS TIME (ns) —————

PACKAGE TYPE: —————

M = 32 pin Plastic SOJ (Package 7)

DEVICE GRADE: —————

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C