# ETC691/ETC693
# µP Supervisory Circuits

## Description

The ETC691/ETC693 micro-processor supervisory circuits are multifunction circuits which monitor battery control functions and power supplies in microprocessor based systems. The circuit functions include a watchdog timer, microprocessor reset, back-up battery switchover, CMOS RAM write protection, and power failure warning.

The supply is monitored with a comparator and an internal reference. $\overline{\text{RESET}}$ will remain logic low with $V_{CC}$ as low as 1.4V and will remain low for 200ms after $V_{CC}$ rises above the reset threshold voltage. Battery-backup mode is activated when $V_{CC}$ falls below both the reset threshold and $V_{BATT}$. $V_{CC}$ is connected to $V_{OUT}$ through a low impedance PMOS switch and is capable of output currents up to 250mA.

The ETC691 has a 4.65V reset threshold, while the ETC693 has a lower reset threshold of 4.4V.

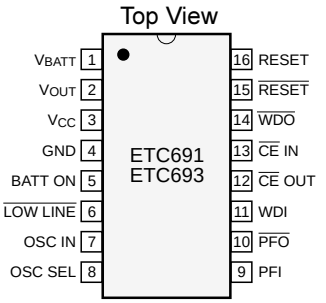
## Typical Applications

- Automotive Systems
- Intelligent Instruments
- Critical Microprocessor Power Monitoring
- Battery Powered Computers
- Controllers

## Ordering Information

| Part | Package | Temp. Range |
|---|---|---|
| ETC691NC | 16-Lead PDIP | 0°C to +70°C |
| ETC691MC | 16-Lead SOIC | 0°C to +70°C |
| ETC691D | Tested Die | 0°C to +70°C |
| ETC693NC | 16-Lead PDIP | 0°C to +70°C |
| ETC693MC | 16-Lead SOIC | 0°C to +70°C |
| ETC693D | Tested Die | 0°C to +70°C |

## Pin Configuration

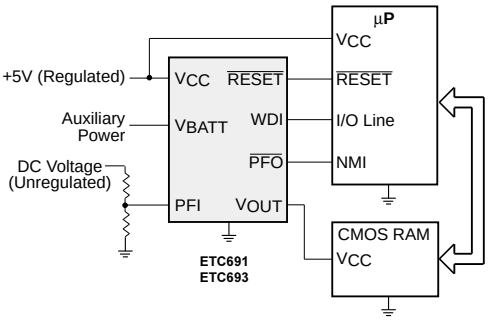



ETC691N - 16 Lead Plastic DIP Package
ETC691M - 16 Lead Plastic SOIC Package

## Features

- Power OK/Reset Time Delay, 200ms
- Watchdog Timer, 100ms, 1.6s or Adj.
- 4.65V or 4.40V Precision Voltage Monitor
- $V_{OUT}$ Capable of Sourcing up to 250mA
- Available in 16-pin Surface Mount (SO)
- <1µA Standby Current
- Early Power Fail Warning or Low Battery Detect

## Typical Operating Circuit



## Absolute Maximum Ratings

Terminal Voltage
- $V_{CC}$, $V_{BATT}$ . . . . . -0.3V to 6.0V
- All Other Inputs . . . . . -0.3V to ($V_{OUT}$ + 0.3V)

Input Current
- $V_{CC}$ . . . . . 250mA
- $V_{BATT}$, Gnd, All Other Inputs. . . . . 25mA

Operating Temperature Range
- ETC69_NC, ETC69_MC, ETC69_D . . . . . 0°C to 70°C

Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering - 10 sec.) . . . . . 300°C
Power Dissipation . . . . . 700mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Operating ranges define those limits between which the functionality of the device is guaranteed.

## Electrical Characteristics

$V_{CC}$ = 4.75V to 5.5V, $V_{BATT}$ = 2.8V, $T_A$ = Operating Temperature Range, unless otherwise noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Battery Backup Switching** | | | | | |
| Operating Voltage Range, $V_{CC}$ & $V_{BATT}$ (see note 1) | | 0 | | 5.5 | V |
| Supply Current (Excludes $I_{OUT}$) | $V_{CC}$ > $V_{BATT}$ - 1.0V | | 35 | 100 | µA |
| Supply Current, Battery-Backup Mode | $V_{BATT}$ = 2.8V, $T_A$ = 25°C<br>$T_A$ = Operating Temp. Range | | 0.001 | 1<br>5 | µA |
| Battery Standby Current | $V_{CC}$ ≥ $V_{BATT}$ + 0.2V, $T_A$ = 25°C<br>$T_A$ = Operating Temp. Range | -0.1<br>-1.0 | | 0.02<br>0.02 | µA |
| $V_{OUT}$ Output Voltage | $V_{CC}$ = 4.5V, $I_{OUT}$ = 25mA<br>$V_{CC}$ = 4.5V, $I_{OUT}$ = 250mA | $V_{CC}$ - 0.05<br>$V_{CC}$ - 0.3 | $V_{CC}$ - 0.025<br>$V_{CC}$ - 0.25 | | V |
| $V_{OUT}$, Battery-Backup Mode | $V_{CC}$ < $V_{BATT}$ - 0.2V, $I_{OUT}$ = 20mA | $V_{BATT}$ - 0.3 | | | V |
| $V_{CC}$ to $V_{OUT}$ On Resistance | $V_{CC}$ = 4.5V | | 0.70 | 1.2 | Ω |
| $V_{BATT}$ to $V_{OUT}$ on Resistance | $V_{BATT}$ = 4.5V<br>$V_{BATT}$ = 2.8V | | | 15<br>25 | Ω |
| Battery Switchover Threshold | Power Up<br>Power Down | | $V_{BATT}$ + 0.03<br>$V_{BATT}$ - 0.03 | | V |
| Battery Switchover Hysteresis | | | 60 | | mV |
| BATT ON Output Low Voltage | ISINK=3.2mA | | | 0.4 | V |
| BATT ON Output Short-Circuit Current | Sink Current<br>Source Current | <br>1 | 60<br>15 | <br>100 | mA<br>µA |

## Electrical Characteristics

$V_{CC}$ = 4.75V to 5.5V, $V_{BATT}$ = 2.8V, $T_A$ = Operating Temperature Range, unless otherwise noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Reset and Watchdog Timer** | | | | | |
| Reset Voltage Threshold | ETC691<br>ETC693 | 4.50<br>4.25 | 4.65<br>4.4 | 4.75<br>4.5 | V |
| Reset Threshold Hysteresis | | | 25 | | mV |
| Reset Active Timeout Period, Internal Oscillator | Power Up | 140 | 200 | 320 | ms |
| Reset Active Timeout Period, External Clock | Power Up | | 2048 | | clock cycles |
| $V_{CC}$-to-RESET Delay | Power Down | | 80 | | µs |
| $\overline{\text{LOW LINE}}$-to-$\overline{\text{RESET}}$ Delay | Power Down | | 50 | | ns |
| $\overline{\text{RESET}}$ Output Voltage | $V_{CC}$ = 5V, $I_{Source}$ = 1.6mA<br>$I_{Sink}$ = 3.2mA, $V_{CC}$ = 4.25V<br>$I_{Sink}$ = 50 µA, $V_{CC}$ = 1.4V | 3.5 | | <br>0.4<br>0.4 | V<br>V<br>V |
| RESET Output Voltage | $I_{Sink}$ = 3.2mA | | | 0.4 | V |
| $\overline{\text{RESET}}$ Output Short-Circuit Current | Source Current | | 7 | 20 | mA |
| Watchdog Timeout Period, Internal Oscillator | Long Period<br>Short Period | 1000<br>70 | 1600<br>100 | 2600<br>160 | ms |
| Watchdog Timeout Period, External Clock | Long Period<br>Short Period | | 4064<br>992 | | clock cycles |
| $\overline{\text{LOW LINE}}$ Output Voltage | $V_{CC}$ = 4.25V, $I_{Sink}$ = 3.2mA<br>$V_{CC}$ = 5V, $I_{Source}$ = 1µA | <br>3.5 | | 0.4 | V |
| $\overline{\text{LOW LINE}}$ Output Short-Circuit Current | Source Current | 1 | 15 | 100 | µA |
| $\overline{\text{WDO}}$ Output Voltage | $I_{Sink}$ = 3.2mA<br>$V_{CC}$ = 5V, $I_{Source}$ = 500µA | <br>3.5 | | 0.4 | V |
| $\overline{\text{WDO}}$ Output Short-Circuit Current | Source Current | | 3 | 10 | mA |
| WDI Minimum Input Pulse | $V_{IL}$ = 0.8V, $V_{IH}$ = 75% of $V_{CC}$ | 100 | | | ns |
| WDI Threshold Voltage | $V_{IH}$<br>$V_{IL}$ | 0.75 X $V_{CC}$ | | <br>0.7 | V |
| WDI Input Current | WDI = 0V<br>WDI = $V_{OUT}$ | -50 | -10<br>20 | <br>50 | µA |

## Electrical Characteristics

$V_{CC}$ = 4.75V to 5.5V, $V_{BATT}$ = 2.8V, $T_A$ = Operating Temperature Range, unless otherwise noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Power Fail Detector** | | | | | |
| PFI Input Threshold | $V_{CC}$ = 5V | 1.2 | 1.25 | 1.3 | V |
| PFI Leakage Current | | -25 | 0.01 | +25 | nA |
| $\overline{PFO}$ Output Voltage | $I_{Sink}$ = 3.2mA<br>$V_{CC}$ = 5V, $I_{Source}$ = 1μA | <br>3.5 | | 0.4 | V |
| $\overline{PFO}$ Output Short-Circuit Current | Source Current | 1 | 15 | 100 | μA |
| PFI Comparator Response Time | $V_{IN}$ = -20mV, $V_{OD}$ = 15mV<br>$V_{IN}$ = 20mV, $V_{OD}$ = 15mV | | 5<br>30 | | μs |
| **Chip Enable Gating** | | | | | |
| $\overline{CE}$ IN Leakage Current | Disabled Mode | | ±0.001 | ±1 | μA |
| $\overline{CE}$ OUT Output Voltage | $V_{CC}$ = 0V, $V_{BATT}$ = 2.8V, $I_{Source}$ = 1μA<br>$V_{CC}$ = 5V, $I_{Source}$ = 100μA | 2.7<br>3.5 | | | V |
| $\overline{CE}$ IN to CE OUT On Resistance | VCC = 4.75V for ETC691<br>VCC = 4.50V for ETC693 | | 75 | 150 | Ω |
| $\overline{CE}$ OUT Output Short-Circuit Current | CE OUT = 0V, Disabled Mode | 0.1 | 0.75 | 2.0 | mA |
| $\overline{CE}$ Propagation Delay | 50Ω Source, $C_{Load}$ = 50pF | | 2 | 10 | ns |
| **Internal Oscillator** | | | | | |
| OSC IN Leakage Current | OSC SEL = 0V | | 0.1 | ±5 | μA |
| OSC IN Input Pullup Current | OSC SEL = $V_{OUT}$, OSC IN = 0V | | 10 | 100 | μA |
| OSC SEL Input Pullup Current | OSC SEL = 0V | | 10 | 100 | μA |
| OSC IN Frequency Range | OSC SEL = 0V | | 30 | | kHz |
| OSC IN Frequency with External Capacitor | OSC SEL = 0V, $C_{OSC}$ = 47pF | | 1.4 | | kHz |
| OSC IN Threshold $V_{IH}$ | | $V_{OUT}$ - 0.4 | $V_{OUT}$ - 0.6 | | V |
| OSC IN Threshold $V_{IL}$ | | | 3.65 | 2.0 | V |

Note 1: $V_{CC}$ or $V_{BATT}$ can go to 0V if the other is ≥ 2V.

## Pin Functions

Pin 1: **$V_{BATT}$** - Backup battery/auxiliary power input. When $V_{CC}$ falls below $V_{BATT}$, auxiliary power is routed to $V_{OUT}$ through a PMOS switch. $V_{BATT}$ pin should be connected to GND if backup battery or auxiliary power is not used.

Pin 2: **$V_{OUT}$** - Output for supply voltage. During normal operation ($V_{CC}$ > $V_{BATT}$), $V_{CC}$ is routed to $V_{OUT}$ through a PMOS switch with a typical on-resistance of less than 1Ω. The $V_{OUT}$ pin can source a continuous current of up to 250mA. When $V_{CC}$ drops below $V_{BATT}$, auxiliary power is routed from the $V_{BATT}$ pin to $V_{OUT}$ through a PMOS switch with a typical on-resistance of less than 15Ω. The $V_{OUT}$ pin can source a continuous current of up to 25mA when in battery backup mode ($V_{CC}$ < $V_{BATT}$). $V_{OUT}$ should be connected to $V_{CC}$ if a backup battery is not used.

Pin 3: **$V_{CC}$** - Primary supply input, +5V.

Pin 4: **GND** - IC ground pin.

Pin 5: **BATT ON** - Backup battery mode indicator. Logic low during normal operation ($V_{CC}$ > $V_{BATT}$), goes high when $V_{CC}$ drops below $V_{BATT}$. BATT ON output can typically sink 60mA. This output can also be used for high current applications which require the $V_{OUT}$ pin to source more than 250mA by providing base drive to an external PNP transistor.

Pin 6: **$\overline{\text{LOW LINE}}$** - Low $V_{CC}$ indicator, goes low when $V_{CC}$ drops below the reset threshold.

Pin 7: **OSC IN** - External oscillator input. When OSC SEL is driven low, an external clock or an external capacitor can be connected to OSC IN to set the watchdog and reset timeout periods (see Table 1). The internal oscillator is enabled when OSC SEL is driven high or left floating. When using the internal oscillator, the watchdog timeout period is set to 100ms by connecting the OSC IN pin to GND or to 1.6 seconds if the OSC IN pin is left floating. In either case, the watchdog timeout period following a reset is 1.6 seconds.

Pin 8: **OSC SEL** - Oscillator select input. An internal oscillator sets the watchdog timeout period and reset delay when OSC SEL is driven high or left floating. When OSC SEL is driven low, an external clock or capacitor on the OSC IN pin can be used to set the watchdog timeout period and reset delay.

Pin 9: **PFI** - Power fail input. Internally connected to the power fail comparator which is referenced to 1.25V. The power fail output ($\overline{\text{PFO}}$) remains high if PFI is above 1.25V. PFI should be connected to GND or $V_{OUT}$ if the power fail comparator is not used.

Pin 10: **$\overline{\text{PFO}}$** - Power fail output. The power fail comparator is independent of all other functions on this device.

Pin 11: **WDI** - Watchdog input. Monitors μP activity, watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ are forced low. The watchdog function can be disabled by floating the WDI pin.

Pin 12: **$\overline{\text{CE}}$ OUT** - Chip enable output. $\overline{\text{CE}}$ OUT follows $\overline{\text{CE}}$ IN when $\overline{\text{RESET}}$ and RESET are not asserted. $\overline{\text{CE}}$ OUT is forced to $V_{OUT}$ when $\overline{\text{RESET}}$ and RESET are asserted.

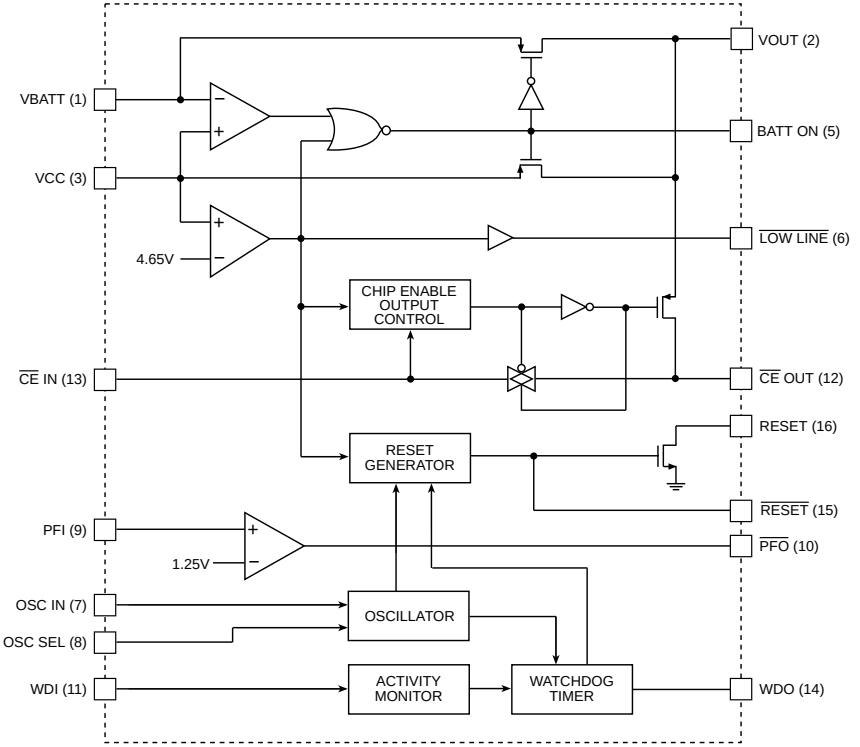
Pin 13: **$\overline{\text{CE}}$ IN** - Chip enable input. $\overline{\text{CE}}$ IN is the input for the chip enable gating circuit. Decoder ouput or address line from μP can be used to generate $\overline{\text{CE}}$ IN. Connect to $V_{OUT}$ or GND if chip enable gating circuit is not used.

Pin 14: **$\overline{\text{WDO}}$** - Output for the watchdog timer. Watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ are forced low. The watchdog function can be disabled by floating the WDI pin.

Pin 15: **$\overline{\text{RESET}}$** - Output for μP reset circuitry. $\overline{\text{RESET}}$ is asserted if either $V_{CC}$ goes below the reset threshold or the watchdog times out. $\overline{\text{RESET}}$ remains asserted for one reset timeout period (see Table 1) after $V_{CC}$ exceeds the reset threshold or after the watchdog times out.

Pin 16: **RESET** - Output for μP reset circuitry. RESET is active high with an open drain and is the inverse of $\overline{\text{RESET}}$.

## Block Diagram



## Circuit Description

**Battery Switchover Section**

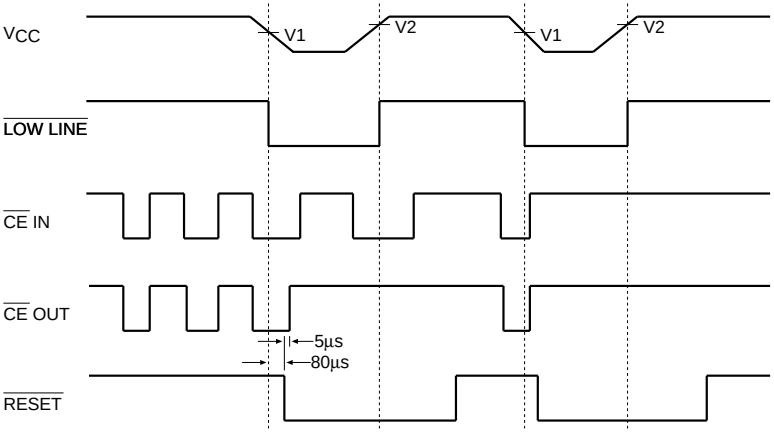
The ETC691/ETC693 monitors the supply voltage applied to the $V_{CC}$ pin. Whenever $V_{CC}$ falls below the reset threshold voltage and $V_{BATT}$, the device enters battery-backup mode. When this happens, the auxiliary supply on $V_{BATT}$ is routed through a low impedence PMOS switch to the $V_{OUT}$ pin. The $V_{OUT}$ pin is capable of sourcing upto 25mA when in the backup mode. $V_{CC}$ is routed to $V_{OUT}$ through a large PMOS switch during normal operation ($V_{CC}$ > $V_{BATT}$) and can source continuous currents of up to 250mA. $V_{OUT}$ can be used to drive CMOS RAM. The BATT ON pin can be used to indicate the status of battery backup mode or as the base drive for an external pass transistor when $V_{OUT}$ has to source more than 25mA in battery-backup mode. $V_{CC}$ is connected to $V_{OUT}$ and the substrate whenever $V_{CC}$ exceeds the reset threshold. If $V_{BATT}$ is connected to a voltage source that is greater than 0.6V above $V_{CC}$, the parasitic diode of the $V_{BATT}$ switch will conduct from $V_{BATT}$ to the substrate.

**Microprocessor Reset**

The $\overline{\text{RESET}}$ and RESET pins are asserted whenever $V_{CC}$ falls below the reset threshold voltage. The reset pins remain asserted for a period of 200ms after $V_{CC}$ has risen above the reset threshold voltage. The reset timeout period can also be selected by the end user (see Table 1). The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. $\overline{\text{RESET}}$ and RESET will remain valid with $V_{CC}$ as low as 1.4V and when auxiliary power is connected to $V_{BATT}$ ($V_{BATT}$ > 2.0V), the reset pins will remain valid with $V_{CC}$ from 0V to 5.5V.

**Chip Enable Gating**

The ETC691/ETC693 also include memory protection circuitry which inhibits the writing of memory during a power fail condition. During normal operation, chip enable transitions are gated through a series transmission gate from $\overline{\text{CE}}$ IN to $\overline{\text{CE}}$ OUT. The typical propagation delay through the chip enable gating circuitry is 2ns. $\overline{\text{CE}}$ OUT follows $\overline{\text{CE}}$ IN unless $V_{CC}$ drops below the reset voltage threshold, at which time $\overline{\text{CE}}$ OUT will remain high until $V_{CC}$ returns to a valid level. EEPROMs can be write protected in a similar manner by connecting the $\overline{\text{CE}}$ OUT pin to the store or write input.




V1 = Reset Voltage Threshold
V2 = Reset Voltage Threshold + Reset Threshold Hysteresis

**Figure 1. Timing Diagram for Reset and Chip Enable**

## Circuit Description

**Power Fail Warning**

An additional comparator which is independent of other functions on the ETC691/ETC693 is provided for early warning of power failure. An external voltage divider can be used to compare unregulated DC to an internal 1.25V reference. The voltage divider ratio on the input of the power fail comparator (PFI) can be chosen so as to trip the power fail comparator a few milliseconds before $V_{CC}$ falls below the maximum reset threshold voltage. The output of the power fail comparator (PFO)

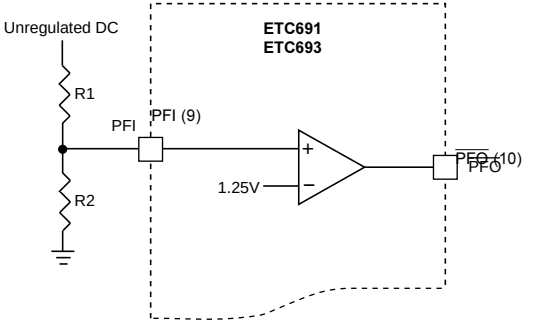



**Figure 2. Power Fail Comparator**

can be used to interrupt the microprocessor when used in this mode and execute shut-down procedures prior to power loss. Hysteresis can be added to this comparator with external resistors, as is commonly done with any comparator. When $V_{CC} < V_{BATT}$ - 1.2V (typ.), the power-fail comparator is turned off and $\overline{PFO}$ is pulled low in order to conserve power.

**Watchdog Timer**

The microprocessor can be monitored by connecting the WDI pin (watchdog input) to a bus line or I/O line. If

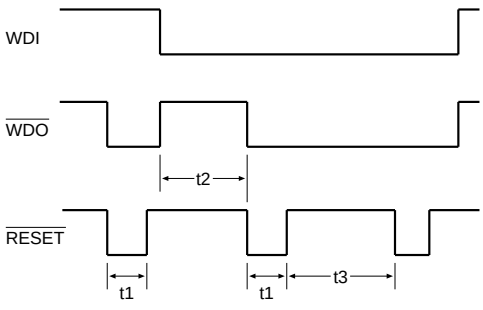



**Figure 3. Watchdog Timeout Period and Reset Active Time**

a transition doesn't occur on the WDI pin within the watchdog timeout period (see Table 1), the microprocessor is reset. $\overline{RESET}$ and RESET will remain asserted for 200ms when this occurs. A minimum pulse of 100ns or any transition low-to-high or high-to-low on the WDI pin will reset the watchdog timer. The output of the watchdog timer ($\overline{WDO}$) will remain high if WDI sees a valid transition within the watchdog timeout period. WDO is high and the watchdog timer is disabled when the WDI input is left floating, VCC is below the reset threshold or when in battery-backup mode.

## Circuit Description

**Table 1. Reset Pulse Width and Watchdog Time-out Selections**

| OSC SEL | OSC IN | Watchdog Time-out Period | | Reset Time-out Period |
|---|---|---|---|---|
| | | Normal | Immediately After Reset | |
| Low | External Clock Input | 992 Clocks | 4064 Clocks | 2048 Clocks |
| Low | External Capacitor | $\frac{600ms}{47pF}$ X C | $\frac{2.4s}{47pF}$ X C | $\frac{1.2s}{47pF}$ X C |
| Floating or High | Low | 100ms | 1.6 seconds | 200ms |
| Floating or High | Floating or High | 1.6 seconds | 1.6 seconds | 200ms |

## Circuit Description

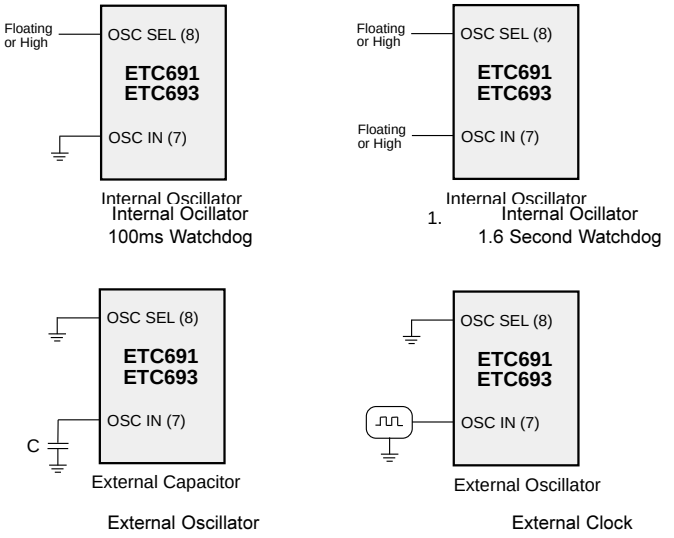


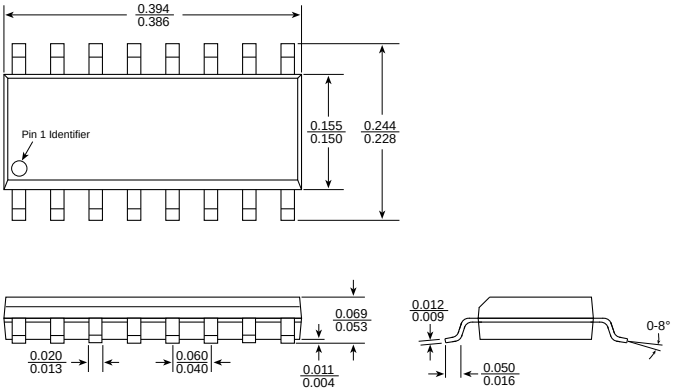

**Figure 4. Oscillator Configurations**

## Alternate Source Cross Reference Guide

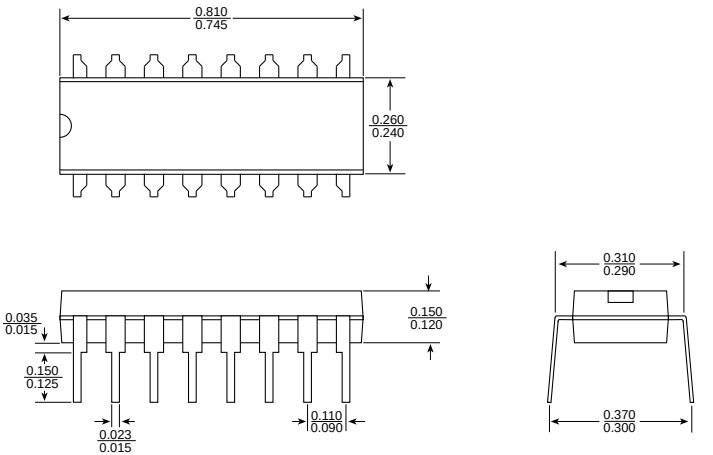
| Industry P/N | ETC Direct Replacement |
|---|---|
| MAX691ACPE | ETC691NC |
| MAX691ACSE | ETC691MC |
| MAX691AC/D | ETC691DC |
| ADM691AN | ETC691NC |
| ADM691AR | ETC691MC |
| LTC691CS | ETC691MC |
| LTC691CN | ETC691NC |
| MAX693ACPE | ETC693NC |
| MAX693ACSE | ETC693MC |
| MAX693AC/D | ETC693DC |

## Packaging Information

### M Package, 16-Pin Small Outline




### N Package, 16-Pin Plastic Dual-In-Line



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