Product Overview
June 1999

National Semiconductor®

MediaGX™ MMX™-Enhanced Processor Integrated x86 Solution with MMX Support

General Description

The MediaGX™ MMX™-Enhanced Processor is an advanced 64-bit x86 compatible processor offering high performance, fully accelerated 2D graphics, a 64-bit synchronous DRAM controller and a PCI bus controller, all on a single chip. Plus it is compatible with MMX™ technology.

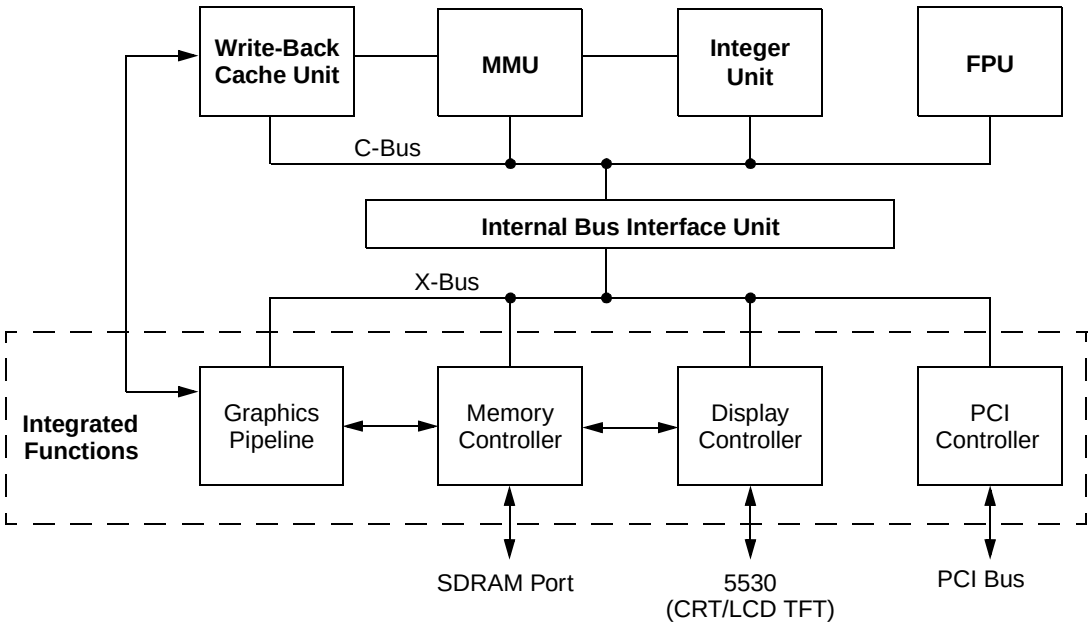
The MediaGX processor core is a proven design that offers competitive CPU performance. It has integer and floating point execution units that are based on sixth-generation technology. The integer core contains a single, six-stage execution pipeline and offers advanced features such as operand forwarding, branch target buffers, and extensive write buffering. A 16 KB write-back L1 cache is accessed in a unique fashion that eliminates pipeline stalls to fetch operands that hit in the cache.

In addition to the advanced CPU features, the MediaGX processor integrates a host of functions which are typically implemented with external components. A full-function graphics accelerator provides pixel processing and rendering functions.

A separate on-chip video buffer enables >30 fps MPEG1 video playback when used together with the 5530 I/O Companion chip. Graphics and system memory accesses are supported by a tightly-coupled synchronous DRAM (SDRAM) memory controller. This tightly coupled memory subsystem eliminates the need for an external L2 cache.

The MediaGX processor includes Virtual System Architecture™ (VSA™ technology) enabling XpressGRAPHICS™ and XpressAUDIO™ subsystems as well as generic emulation capabilities. Software handler routines for the XpressGRAPHICS and XpressAUDIO subsystems can be included in the BIOS and provide compatible VGA and 16-bit industry standard audio emulation. XpressAUDIO technology eliminates much of the hardware traditionally associated with audio functions.

Internal Block Diagram



Highlights (Continued)

Features

General Features

- Packaged in:
  - 352-Terminal Ball Grid Array (BGA) or
  - 320-Pin Staggered Pin Grid Array (SPGA)
- 0.35-micron four layer metal CMOS process
- Split rail design (3.3V I/O and 2.9V core)

64-Bit x86 Processor

- Supports the MMX™ instruction set extension for the acceleration of multimedia applications
- Speeds offered up to 300 MHz
- 16 KB unified L1 cache
- Integrated Floating Point Unit (FPU)
- Re-entrant System Management Mode (SMM) enhanced for VSA

PCI Controller

- Fixed, rotating, hybrid, or ping-pong arbitration
- Supports up to three PCI bus masters
- Synchronous CPU and PCI bus clock frequency
- Supports concurrency between PCI master and L1 cache

Power Management

- Designed to support 5530 power management architecture
- CPU only Suspend or full 3V Suspend supported:
  - Clocks to CPU core stopped for CPU Suspend
  - All on-chip clocks stopped for 3V Suspend
  - Suspend refresh supported for 3V Suspend

Virtual Systems Architecture Technology

- Architecture allows OS independent (software) virtualization of hardware functions
- Provides compatible high performance legacy VGA core functionality

  Note: GUI (Graphical User Interface) graphics acceleration is pure hardware.
- Provides 16-bit XpressAUDIO subsystem

2D Graphics Accelerator

- Graphics pipeline performance significantly increased over previous generations by pipelining burst reads/writes
- Accelerates BitBLTs, line draw, text
- Supports all 256 raster operations
- Supports transparent BLTs
- Runs at core clock frequency
- Full VGA and VESA mode support
- Special "Driver level" instructions utilize internal scratchpad for enhanced performance

Display Controller

- Video Generator (VG) improves memory efficiency for display refresh with SDRAM
- Supports a separate MPEG1 video buffer and data path to enable video acceleration in the 5530
- Internal palette RAM for use with the 5530
- Direct interface to 5530 for CRT and TFT flat panel support which eliminates need for external RAMDAC
- Hardware frame buffer compressor/decompressor
- Hardware cursor
- Supports up to 1280x1024x8 bpp and 1024x768x16 bpp

XpressRAM™ Subsystem

- Memory control/interface directly from CPU
- 64-Bit wide memory bus
- Support for:
  - Two 168-pin unbuffered DIMMs
  - Up to 16 open banks simultaneously
  - Single or 16-byte reads (burst length of two)

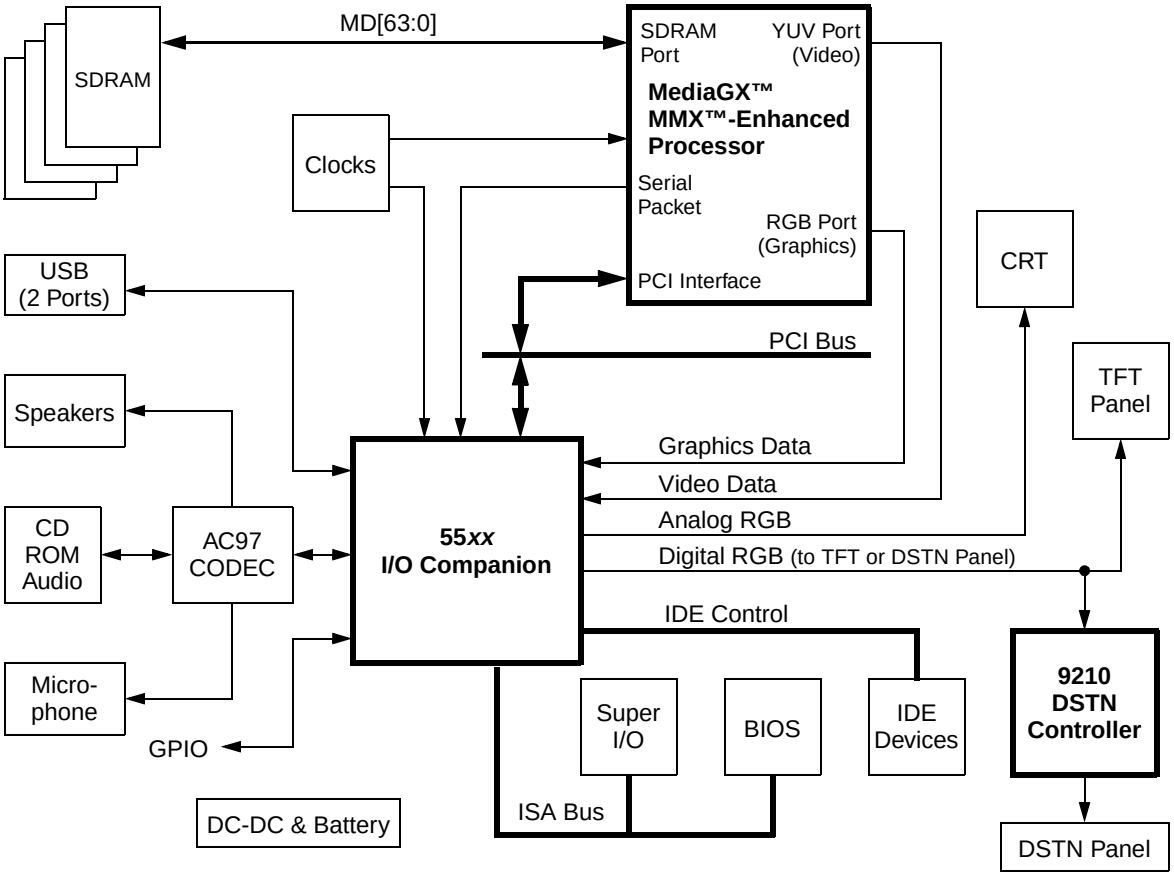
Highlights (Continued)

System Designs

The system consists of two chips, the MediaGX MMX-Enhanced Processor and the 5530 I/O Companion. The system provides high performance using 64-bit x86 processing. The two chips integrate video, audio and memory interface functions normally performed by external hardware.

The figure below shows a typical system block diagram. It includes the 9210 Dual-Scan Flat Panel Display Controller for designs that need to interface to a DSTN panel (instead of a TFT panel).

System Block Diagram



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