ESS Technology, Inc.

ES3308
MPEG2 Audio/Video Decoder
Product Brief

OVERVIEW

The ES3308 decoder is an MPEG2 system, audio, video, and transport-layer decoder designed for Set-Top box, DVD, and Broadcast PC applications. It is fully programmable and can decode a wide variety of compression algorithms. In addition, it integrates a transport layer with 32 PID's as required by the Digital Video Broadcast (DVB) standard. The ES3308 has the largest feature set and is the most-highly integrated and cost-effective MPEG2 solution currently available.

The ES3308 provides auxiliary control pins, a glueless 8/16-bit YUV or 24-bit RGB video interface, and Color Space Conversion (CSC) hardware. The chip also includes an integrated audio DAC interface to reduce audio glue-logic.

The ES3308 can decode MPEG2 video and layer 1 or layer 2 audio simultaneously. For embedded applications, the ES3308's internal RISC processor can be used in place of a microcontroller to provide all system controls and user features. Additional features, such as video error concealment using ESS's SmartStream™ technology, video standards conversion, and video post-processing are also included.

The MPEG2 system bitstream is passed to the decoder through the 16-bit parallel host interface. The ES3308 then parses the system layer and demultiplexes the audio and video streams. Audio is decoded and passed through an audio serial bus to an external audio DAC and then to the speaker. Video is decoded and output as YUV or RGB digital pixels to an NTSC or PAL video encoder. System control and housekeeping functions (keypad and remote control) are also provided by the ES3308 decoder.

FEATURES

- MPEG2 Video decoding at MP@ML (Main Profile at Main Level)
- MPEG audio layer 1 and layer 2 (Musicam)
- Video scaling, video interlacing hardware
- General auxiliary pin can be configured as DSA or I^2C
- Built-in transport layer with 32 PIDs for DVB standard
- On-chip error concealment with SmartStream™
- Color Space Conversion (CSC)
- STC interpretation and audio/video clock PLL control
- Includes CD block decoder functions
- 8-/16-bit YUV mode output
- 2, 4, or 8 bits per pixel OSD with blending capabilities
- Supports 256Fs or 384Fs audio system clock
- Interface to EDO or Fast Page mode DRAM up to 8 MB
- 208 PQFP, power consumption < 1 Watt
- 80MHz clock, 3.45 V power supply with 5 V tolerant I/O's

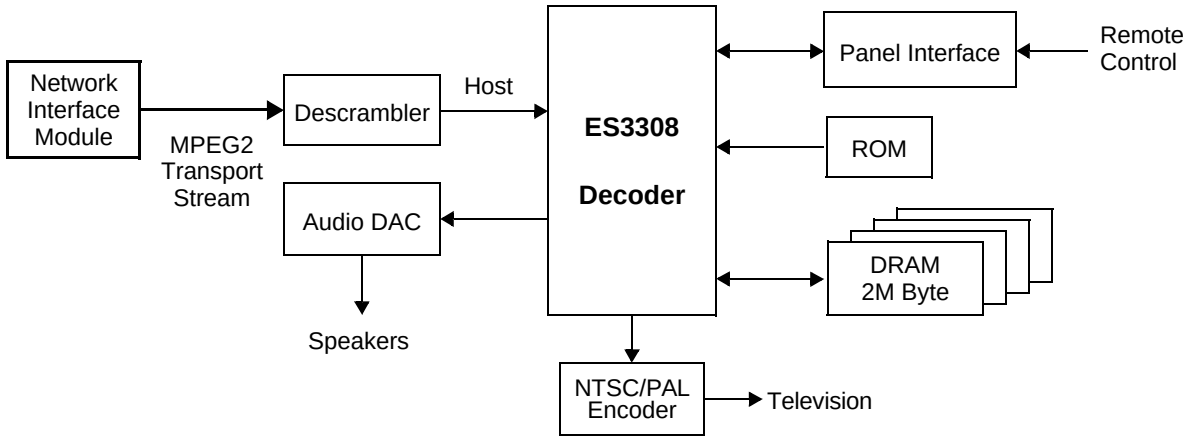

Figure 1 ES3308 System Block Diagram

ES3308 FUNCTIONAL DESCRIPTION

Figure 2 shows the internal architecture of the ES3308. The left (DMA and RISC processor) side of the figure deals with compressed data types and command and control. The right (DRAM, DMA, and MPEG processor) side handles uncompressed and intermediate data.

The Video Output bus outputs uncompressed video from the chip. The host bus, TDM bus, and the audio interface transfer low-data-rate, compressed information, or audio/network data. Passage of data through the system is controlled by the DMA controller (DRAM) associated with the internal buses. These run under the supervision of the RISC processor.

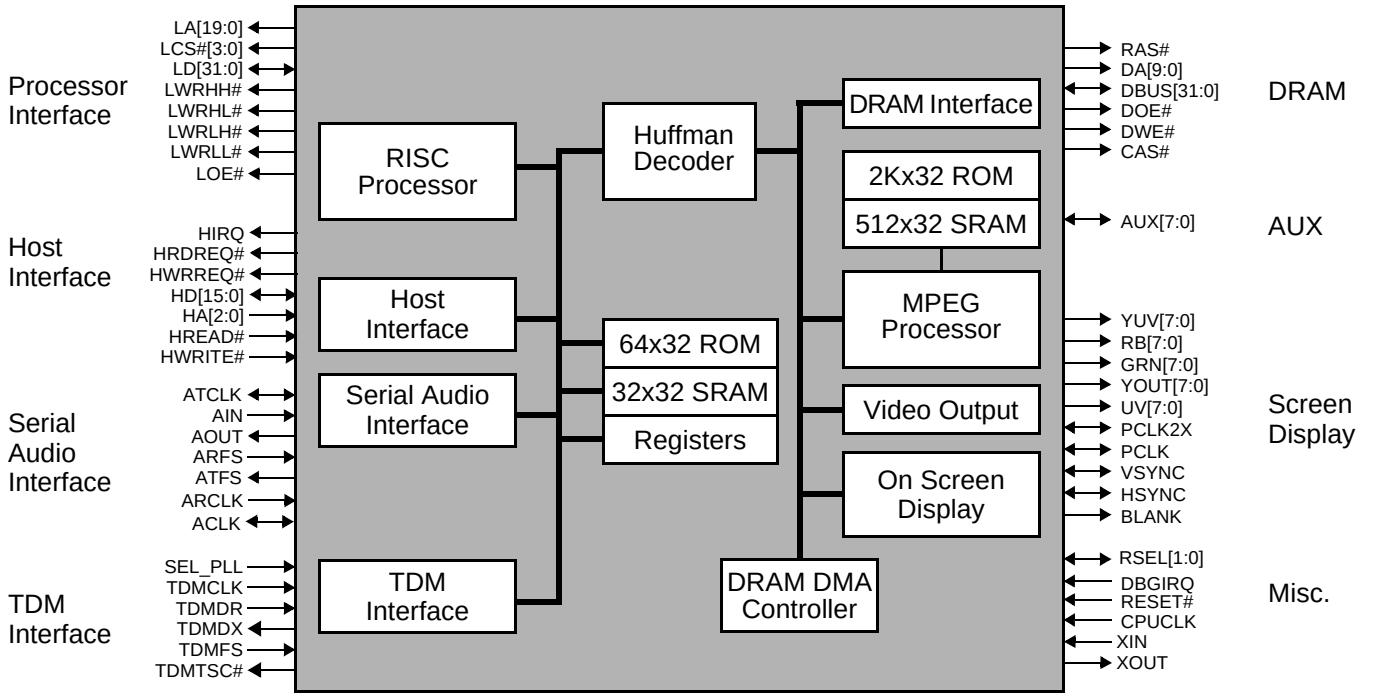

Figure 2 ES3308 Block Diagram

RISC Processor

The ES3308 microprocessor is a 32-bit instruction and 32-bit data pipelined RISC processor. The processor adds a number of instructions that speed up byte and word accesses, and it has improved interrupt processing capabilities. The microprocessor has an instruction cache which improves code access time by a factor of two.

The ES3308 does not require an external boot ROM for power-up initialization; the microprocessor can boot from either on-chip ROM or through the external interface. It also has a small amount of on-chip SRAM to keep commonly used data. Access to this memory is overlapped with the next instruction fetch and has no cost.

The microprocessor uses pipelined architecture and is programmed using an enhanced, optimizing C-language compiler.

Host Interface

The host interface provides a general-purpose parallel interface to the ES3308. It contains three ports: a debug port, a command port, and a DMA port. It is used for communication between a host processor and the ES3308. It can also be used for bitstream input or user data input/output.

The host interface has three registers that control the operation of the flags and interrupts. Flags are used to indicate the ES3308's readiness to accept or supply data over the host port DMA channel. The interrupts may be used for exception indication from RISC-to-host or from host-to-RISC. The interrupts are maskable. The host port is usually connected to the source of command and control information and of any high- or low-speed data.

Audio Interface

The audio interface is a bidirectional serial port that connects to a DAC serial port for the transferring of PCM (Pulse Code Modulation) audio data. It supports 16/24-bit audio frames and normal left/right-justified mode. No external master clock is required. It can also be connected to audio DACs or to a DSP for advanced audio processing. Audio decompression is handled inside the ES3308. This close coupling allows accurate audio/video synchronization.

The ES3308 has an additional audio mode, selected by an internal register, that allows direct connection to audio DACs without glue logic. This is done by changing TFS (audio transmit frame sync) to RFS (audio receive frame sync).

TDM Interface

The TDM (Time Division Multiplexed) interface implements a high-speed, bidirectional serial bus, which is intended to transfer the encoded bitstream to the network interface. It can implement a number of high-speed serial protocols, including Concentration Highway Interface (CHI), GCI, K2, SLD, MVIP, and IOM2 formats. The TDM port can also act as a general-purpose 16 Mbit/sec serial link when not constrained by the TDM protocols; for example, I^2S serial interface for direct connection to a CD-ROM drive.

DRAM Interface

The DRAM interface provides glueless connection to DRAM memory chips. It supports from 512 Kbytes to 4 Mbytes of DRAM, implemented using x1, x4, or x16 chips. The DRAM interface is also configurable in depth to allow 16M-bit addressing and Extended Data Out (EDO) DRAMS. A wide variety of DRAM speed grades may be used.

The DRAM interface is 32-bits wide and, at high ES3308 clock speeds, provides sufficient bandwidth to decode MPEG and display 1024x768 resolution images at 75 Hz. For less demanding applications the bus can operate in a 16-bit mode. In this mode a single 256kx16 DRAM chip can be used. The single DRAM, 16-bit mode is able to display up to 800x600 video at a 75 Hz refresh rate.

DRAM DMA Controller

The DRAM DMA controller has multiple channels that transfer 32-bit data between the DRAM and the video interface, the Huffman decoder, the portal, the MPEG processor, and DRAM refresh.

The video interface, Huffman decoder, and the MPEG processor sections all contain memory that allows the DMA controller to transfer data in DRAM page mode. One DMA channel provides DRAM refresh.

MPEG Processor

The MPEG processor implements a programmable video signal processor that executes the decompression operations required by the MPEG, JPEG, and H.261 standards as well as some proprietary algorithms. The MPEG processor performs video pre-processing and post-processing functions in software, which enables the ES3308 to perform arbitrary filtering and scaling of outgoing video.

The microcode program for the MPEG processor is stored in 2K words of on-chip ROM. 512 words of on-chip SRAM allow new microcode subroutines to be downloaded. Most MPEG processor instructions are 32-bits wide.

Video Output

The video output section displays video frames stored in the DRAM. It also provides hardware post-processing functions that can be used with software running on the MPEG processor. In particular, it contains storage-to-buffer outgoing video, multi-tap decimation, color conversion circuitry and interpolation filters, and a temporal filter. The decimation and interpolation filters allow conversion between SIF, CIF, QCIF, or any commonly used display formats for computer and TV video encoder chips such as CCIR601 and 640x480 VGA. The video output contains a programmable CRT controller to handle interlaced and progressive scanning. The CRT controller can be programmed to generate video syncs and blanks or can be genlocked to an external video source.

On-Screen Display

The video output section also includes dedicated on-screen display (OSD) hardware. The OSD can have 2-, 4-, or 8-bits per pixel palletized colors, including transparent, and can take up the full or a partial screen area. It is multiplexed into the output video stream after scaling and before color space conversion has been completed. The OSD bitmap is stored in the reference DRAM.

Huffman Decoder

The Huffman decoder is a high-speed engine that decodes using MPEG Huffman tables. The decode tables are programmable and can be changed by the user's application. Zero-run-length/amplitude (RLA) tokens are transferred on the DRAM bus to the MPEG processor core. The Huffman coded data is transferred by a DMA channel.

Internal ROM and SRAM

The ES3308 has a 64x32 ROM and a 32x32 SRAM dedicated to the RISC processor, and a 2Kx32 ROM and a 512x32 SRAM dedicated to the MPEG processor.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage temperature range	-65°C to 150°C
Operating temperature range	-65°C to 110°C
Voltage range on any pin	-0.5V to (VDD + 0.5V)
Power dissipation	0.5 W

Recommended Operating Conditions

Operating temperature range	0°C to 70°C
Supply voltage VDD	3.45V ± 5 %
Supply voltage VPP	5V ± 5 %

DC Electrical Characteristics

(Over recommended operating conditions)

Table 1 DC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit	Comments
Vih	High-level input voltage	2.0	VDD+0.25	V	All inputs TTL levels except CLK
Vil	Low-level input voltage	-0.3	0.8	V	All inputs TTL levels except CLK
Vch	CLK high-level input	2.0	VDD+0.25	V	TTL level input
Vcl	CLK low-level input	-0.3	0.8	V	TTL level input
Voh	High-level output voltage	3.0	–	V	IOH = 1 mA
Vol	Low-level output voltage	–	0.45	V	IOL = 4 mA
Ili	Input leakage current	–	±15	µA	
Ilo	Output leakage current	–	±15	µA	
Cin	Input capacitance	–	10	pF	fc = 1 MHz
Co	Input/output capacitance	–	12	pF	fc = 1 MHz
Cclk	CLK capacitance	–	20	pF	fc = 1 MHz

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: 510-492-1088
Fax: 510-492-1098