OVERVIEW

The ES3301 is a versatile transport-layer demultiplexer, parser, and descrambler designed for Set-Top Box, DVD, and Broadcast PC applications. It is fully programmable and incorporates a 32-bit RISC processor which eliminates the need for an external microcontroller. The RISC processor can be used to provide system control, DVD navigation, and user interface, and supports a wide variety of input formats. Together with the ES3308, the ES3301 offers the largest feature set and the most cost-effective MPEG2 solution currently available.

Each valid input bitstream should contain adequate information for the transport layer to identify, process, and channel it to an appropriate control line or data path. The bitstream is descrambled and parsed to the PID table where the data is compared to determine input format and its data type. The transport layer contains a 32-entry PID (Packet ID) that meets the DVB (Digital Video Broadcast) standard.

Then, the same descrambled input bitstream is processed through various continuity and conditional logic for data validation. An error detection mechanism is employed in the continuity check logic. The invalid data is discarded. Under the control of program sequencer and router logic, valid data is automatically demultiplexed and transferred to its intended destination.

FEATURES

- DVD, DVB and DBS transport-layer demultiplexing and descrambling
- Internal 32-bit RISC microprocessor
- Supports a wide variety of input formats:
  - PES (Packetized Elementary Stream)
  - TS (MPEG-2 Transport Stream)
  - PS (MPEG-2 Program Stream)
  - MPEG-1 System Stream
  - DSS (Digital Satellite System)
- Full DVD 1.0 Navigation Control, DVD Packet Stream Control
- CSS (Content Scrambling System) and CAD (Conditional Access Decryption)
- Automatic packet routing
- Transport layer demux with 32-entry PID table per DVB standard
- Advanced error detection logic
- STC interpretation and audio/video clock for PLL control
- Programmable with internal cache RAM
- General auxiliary pin can be configured as DSA or I2C
- 208 PQFP, power consumption < 1 Watt
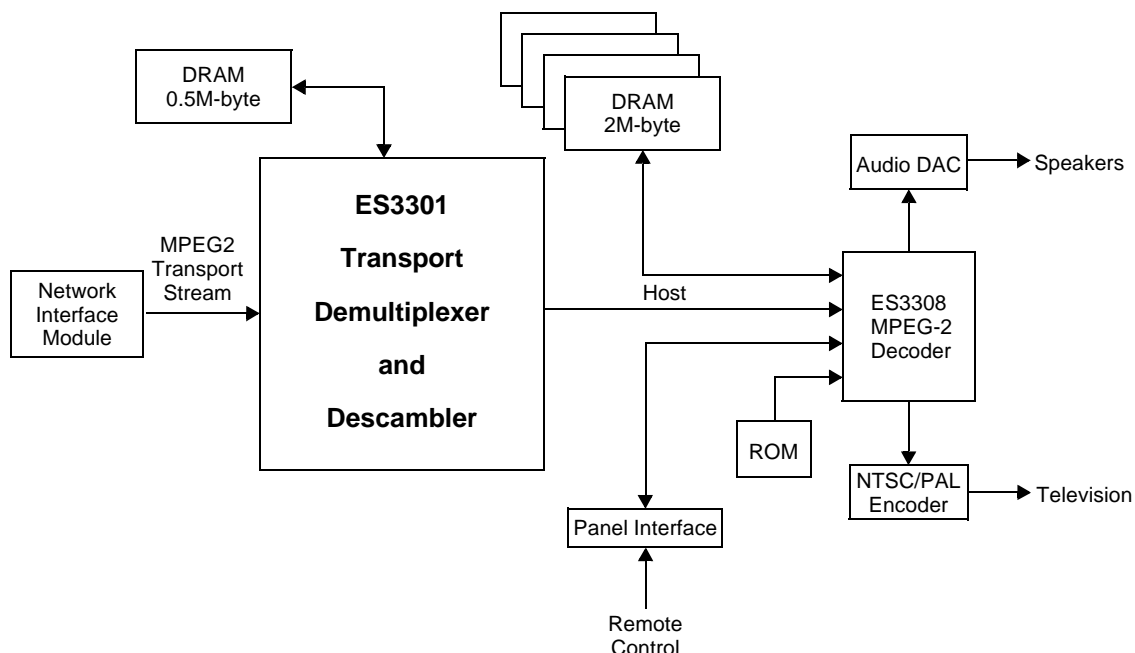- 80MHz clock, 3.45V power supply with 5V tolerant I/Os

Figure 1 Set-Top Box Using the ES3301

FUNCTIONAL DESCRIPTION

Figure 2 shows the internal architecture of the ES3301. The input is 16-bit and selectable either through the TDM or host interface. The input format can be in the form of Program, Transport and Digital Satellite System streams.

The input stream is translated into control signals and data. The control signal is channeled to one of the request lines: RISC-DMA, video, audio or data (aux1 and aux2). The data is then routed to a data path.
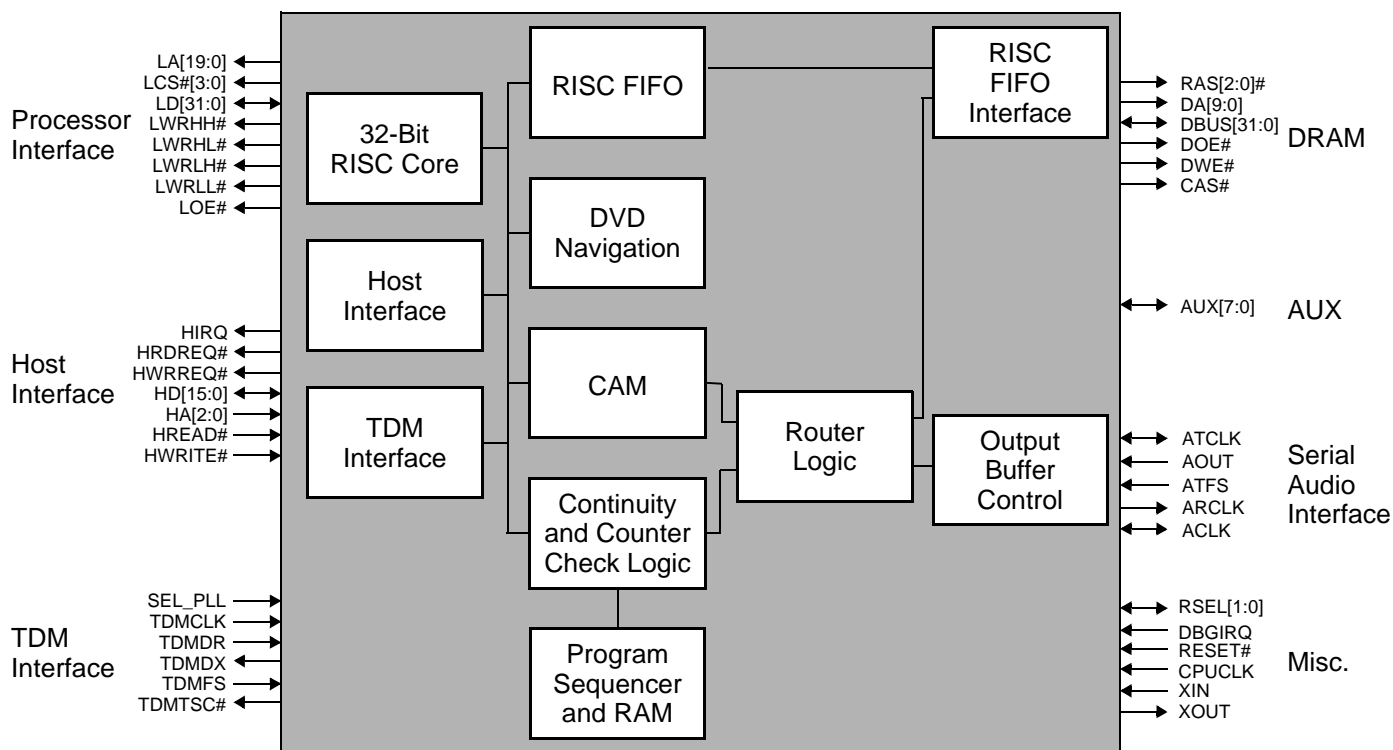

Figure 2 ES3301 Block Diagram

RISC Processor

The ES3301 microprocessor is a 32-bit instruction and 32-bit data pipelined RISC processor. The processor adds a number of instructions that speed up byte and word accesses, and it has improved interrupt processing capabilities. The microprocessor has an instruction cache which improves code access time by a factor of two.

The ES3301 does not require an external boot ROM for power-up initialization; the microprocessor can boot from either on-chip ROM or through the external interface. It also has a small amount of on-chip SRAM to keep commonly used data. Access to this memory is overlapped with the next instruction fetch and has no cost.

The microprocessor uses pipelined architecture and is programmed using an enhanced, optimizing C-language compiler.

Host Interface

The host interface provides a general-purpose parallel interface to the ES3301. It contains three ports:

- a debug port
- a command port, and
- a DMA port

It is used for communication between a host processor and the ES3301. It can also be used for bitstream input or user data input/output.

The host interface has three registers that control the operation of the flags and interrupts. Flags are used to indicate the ES3301's readiness to accept or supply data over the host port DMA channel. These interrupts may be used for exception indication from RISC-to-host or from host-to-RISC and are maskable. The host port is usually connected to the source of command and control information and of any high- or low-speed data.

TDM Interface

The TDM (Time Division Multiplexed) interface implements a high-speed, bidirectional serial bus, which is intended to transfer the encoded bitstream to the network interface. It can implement a number of high-speed serial protocols, including Concentration Highway Interface (CHI), GCI, K2, SLD, MVIP, and IOM2 formats. The TDM port can also act as a general-purpose 16-Mbps serial link when not constrained by the TDM protocols; for example, an I2S serial interface for direct connection to a DVD-ROM drive.

CAM (Content Addressable Memory)

The content addressable memory holds a 32-entry PID. Each valid entry typically contains the PID of the desirable packets corresponding to a particular component of a selectable channel, and its intended destination. The PID table is downloadable from the RISC.

Continuity Counter and Condition Check Logic

Data received from the host or TDM module is in the form of packetized block. Each block contains a header information that identifies the packet number. Most of the time the data blocks received are not in sequential order. The ES3301 employs Continuity Counter logic to verify order. After the data is verified for continuity, it is then compared against various conditional checks to identify the data type.

Sequencer Program Counter and RAM

As the name implies, this module puts together valid data blocks in sequential order. The Program Sequencer RAM contains 128 micro-instructions, downloadable from the host. Under micro-program control, input packets with PID matching those in the PID table, can be automatically routed to their intended destination with little or no intervention from the RISC core inside the ES3301.

Router Control Logic

The Router Control Logic directs the valid sequential data blocks to the appropriate control lines through the RISC FIFO or Output Buffer Control interface. The output data is routed to the data lines.

DVD Navigation

The ES3301 supports standard DVD Navigation 1.0, which allows the user to navigate various program chains, and implements the annex J features, such as:

- interactive viewing modes: multi-angle, multi-versions of the film
- title/chapter search, fast forward & fast reverse, next & previous, etc.
- multi-languages & multi-subtitles
- multi-aspect ratio TV modes
- parental control

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage temperature range	-65 °C to 150 °C
Operating temperature range	-65 °C to 110 °C
Voltage range on any pin	-0.5 V to (VDD + 0.5 V)
Power dissipation	0.5 W

Recommended Operating Conditions

Operating temperature range	0 °C to 70 °C
Supply voltage VDD	3.45 V ± 5%
Supply voltage V_{PP}	5 V ± 5%

DC Electrical Characteristics

(over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Comments
Vih	High-level input voltage	2.0	VDD + 0.25	V	All inputs TTL levels except CLK
Vil	Low-level input voltage	-0.3	0.8	V	All inputs TTL levels except CLK
Vch	CLK high-level input	2.0	VDD + 0.25	V	TTL level input
Vcl	CLK low-level input	-0.3	0.8	V	TTL level input
Voh	High-level output voltage	3.0	–	V	IOH = 1mA
Vol	Low-level output voltage	–	0.45	V	IOL = 4mA
Ili	Input leakage current	–	± 15	µA	
Ilo	Output leakage current	–	± 15	µA	
Cin	Input capacitance	–	10	pF	fc = 1 MHz
Co	Input/output capacitance	–	12	pF	fc = 1 MHz
Cclk	CLK capacitance	–	20	pF	fc = 1 MHz

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