

## EM512W16

### 512Kx16 bit Ultra-Low Power Asynchronous Static RAM

#### Overview

The EM512W16 is an integrated memory device containing a low power 8 Mbit Static Random Access Memory organized as 524,288 words by 16 bits. The base design is the same as NanoAmp's standard low voltage version, EM512W16. The device is fabricated using NanoAmp's advanced CMOS process and high-speed/ultra low-power/low-voltage circuit technology. The device pinout is compatible with other standard 512K x 16 SRAMs. The device is designed such that a creative user can improve system power and performance parameters through use of it's unique page mode operation.

FIGURE 1: Pin Configuration

	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	$\text{A}_0$	$\text{A}_1$	$\text{A}_2$	$\text{CE}_2$
B	$\text{I/O}_8$	$\overline{\text{UB}}$	$\text{A}_3$	$\text{A}_4$	$\overline{\text{CE}_1}$	$\text{I/O}_0$
C	$\text{I/O}_9$	$\text{I/O}_{10}$	$\text{A}_5$	$\text{A}_6$	$\text{I/O}_1$	$\text{I/O}_2$
D	$\text{V}_{\text{SS}}$	$\text{I/O}_{11}$	$\text{A}_{17}$	$\text{A}_7$	$\text{I/O}_3$	$\text{V}_{\text{CC}}$
E	$\text{V}_{\text{CC}}$	$\text{I/O}_{12}$	NC	$\text{A}_{16}$	$\text{I/O}_4$	$\text{V}_{\text{SS}}$
F	$\text{I/O}_{14}$	$\text{I/O}_{13}$	$\text{A}_{14}$	$\text{A}_{15}$	$\text{I/O}_5$	$\text{I/O}_6$
G	$\text{I/O}_{15}$	NC	$\text{A}_{12}$	$\text{A}_{13}$	$\overline{\text{WE}}$	$\text{I/O}_7$
H	$\text{A}_{18}$	$\text{A}_8$	$\text{A}_9$	$\text{A}_{10}$	$\text{A}_{11}$	NC

48 Pin BGA (top)

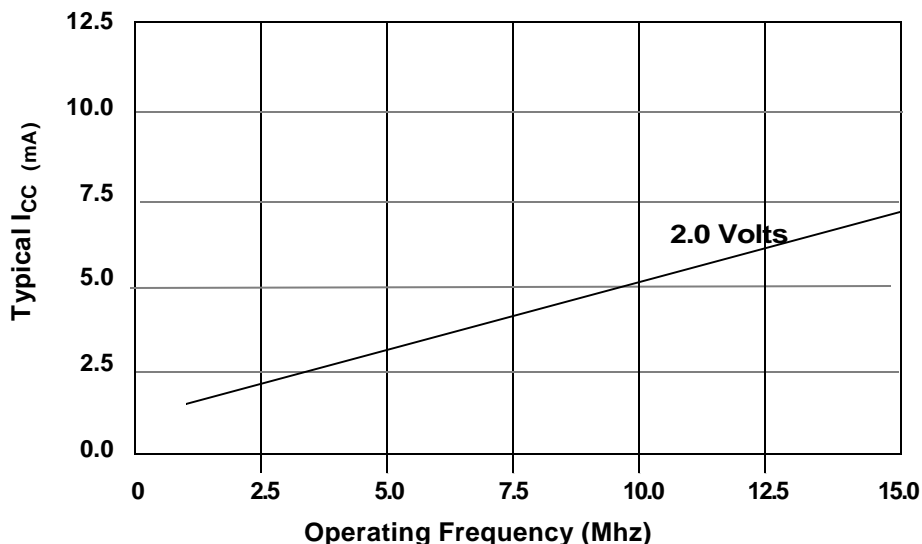
#### Features

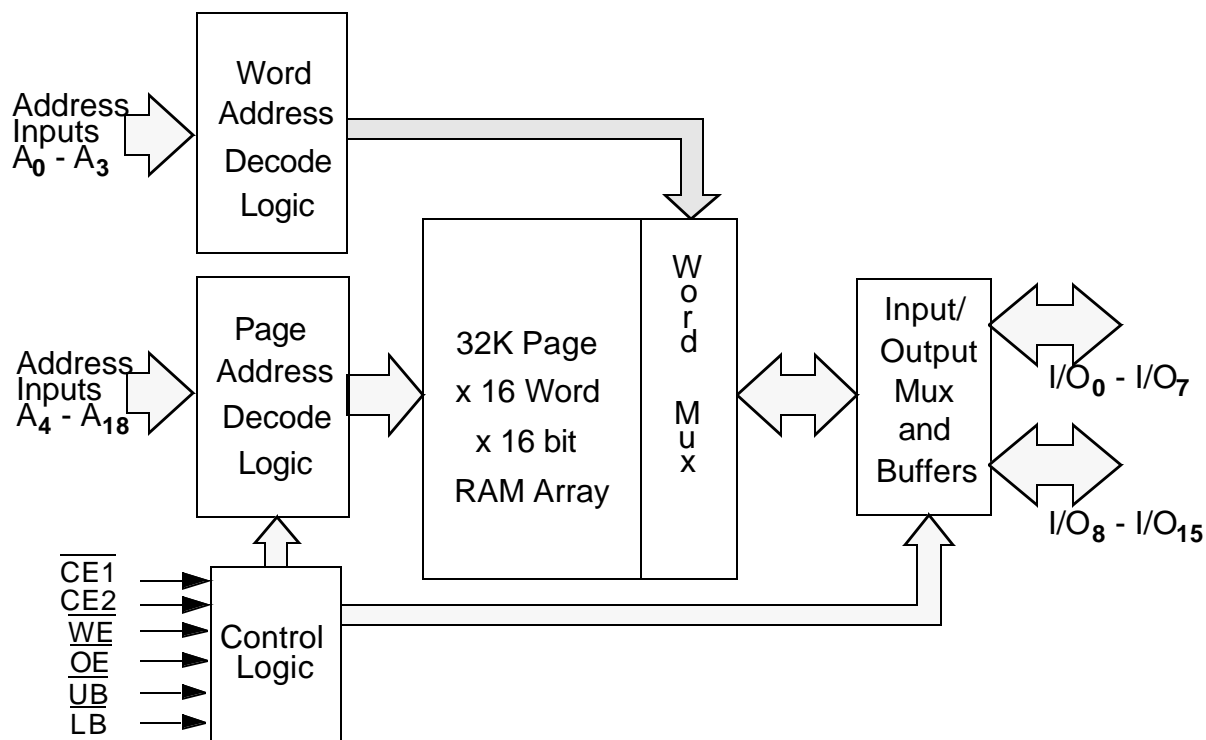
- Extended Operating Voltage Range:**  
 $\text{V}_{\text{CC}}$  - 1.65 to 2.2 Volts
- Extended Temperature Range:**  
-40 to +85 °C
- Fast Cycle Time:**  
Random Access < 70 ns  
Page-Mode < 25 ns
- Very Low Operating Current:**  
 $\text{I}_{\text{CC}}$  < 10.0 mA typical at 2V, 10 Mhz
- Very Low Standby Current:**  
 $\text{I}_{\text{SB}}$  < 2 uA @ 55 °C
- 16 Word Fast Page-Mode Operation**
- 48-Pin BGA or Known Good Die available**

TABLE 1: Pin Descriptions

Pin Name	Pin Function
$\text{A}_0\text{-A}_{18}$	Address Inputs
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{CE}_1}, \text{CE}_2$	Chip Enable Inputs
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{UB}}$	Upper Byte Enable Input
$\overline{\text{LB}}$	Lower Byte Enable Input
$\text{I/O}_0\text{-I/O}_{15}$	Data Inputs/Outputs
$\text{V}_{\text{CC}}$	Power
$\text{V}_{\text{SS}}$	Ground
NC	Not Connected

FIGURE 1: Typical Operating Envelope (Serial R/W Mix)



**FIGURE 3: Functional Block Diagram****TABLE 2: Functional Description**

$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\text{I/O}_0 - \text{I/O}_{15}^1$	MODE	POWER
H	X	X	X	X	X	High Z	Standby <sup>2</sup>	Standby
X	L	X	X	X	X	High Z	Standby <sup>2</sup>	Standby
X	X	X	X	H	H	High Z	Standby <sup>2</sup>	Standby
L	H	L	X <sup>3</sup>	L <sup>1</sup>	L <sup>1</sup>	Data In	Write <sup>3</sup>	Active
L	H	H	L	L <sup>1</sup>	L <sup>1</sup>	Data Out	Read	Active
L	H	H	H	L <sup>1</sup>	L <sup>1</sup>	High Z	Active	Active

1. When  $\overline{\text{UB}}$  and  $\overline{\text{LB}}$  are in select mode (low), I/O<sub>0</sub> - I/O<sub>15</sub> are affected as shown. When  $\overline{\text{LB}}$  only is in the select mode only I/O<sub>0</sub> - I/O<sub>7</sub> are affected as shown. When  $\overline{\text{UB}}$  is in the select mode only I/O<sub>8</sub> - I/O<sub>15</sub> are affected as shown. If both  $\overline{\text{UB}}$  and  $\overline{\text{LB}}$  are in the deselect mode (high), the chip is in a standby mode.
2. When the device is in standby mode, control inputs ( $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{UB}}$ , and  $\overline{\text{LB}}$ ), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When  $\overline{\text{WE}}$  is invoked, the  $\overline{\text{OE}}$  input is internally disabled and has no effect on the circuit.

**TABLE 3: Capacitance\***

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		8	pF
I/O Capacitance	C <sub>I/O</sub>	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		8	pF

Note: These parameters are verified in device characterization and are not 100% tested

**TABLE 4: Absolute Maximum Ratings\***

Item	Symbol	Rating	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN,OUT}$	$-0.3$ to $V_{CC}+0.3$	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	$-0.3$ to $3.0$	V
Storage Temperature	$T_{STG}$	$-40$ to $125$	$^{\circ}C$
Operating Temperature	$T_A$	$-40$ to $+85$	$^{\circ}C$

\* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**TABLE 5: Operating Characteristics (Over specified Temperature Range)**

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$		1.65		2.2	V
Minimum Data Retention Voltage	$V_{DR}$	Chip Disabled (Note 2)	1.2			V
Input High Voltage	$V_{IH}$		$0.7V_{CC}$		$V_{CC}+0.5$	V
Input Low Voltage	$V_{IL}$		$-0.5$		$0.3V_{CC}$	V
Output High Voltage	$V_{OH}$	$I_{OH} = 0.2mA$	$V_{CC}-0.2$			V
Output Low Voltage	$V_{OL}$	$I_{OL} = -0.2mA$			0.2	V
Input Leakage Current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$			0.5	$\mu A$
Output Leakage Current	$I_{LO}$	$\overline{OE} = V_{IH}$ or Chip Disabled			0.5	$\mu A$
Read/Write Operating Supply Current @ 1 $\mu s$ Cycle Time	$I_{CC1}$	$V_{CC}=2.2V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OL} = 0$			2.0	mA
Random Access Operating Supply Current @ 70 nS Cycle Time	$I_{CC2}$	$V_{CC}=2.2V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OL} = 0$			15.0	mA
Page Mode Operating Supply Current @ 25 nS Cycle Time	$I_{CC2}$	$V_{CC}=2.2V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OL} = 0$			7.0	mA
Read/Write Quiescent Operating Supply Current (Note 2)	$I_{CC3}$	$V_{IN} = V_{CC}$ or $0V$ Chip Enabled, $I_{OL} = 0$ f = 0, $t_A = 85^{\circ}C$ , $V_{CC} = 3.6V$			2.0	mA
Operating Standby Current (Note 2)	$I_{SB1}$	$V_{IN} = V_{CC}$ or $0V$ Chip Disabled $t_A = 55^{\circ}C$ , $V_{CC} = 2.2V$			2	$\mu A$
Maximum Standby Current (Note 2)	$I_{SB2}$	$V_{IN} = V_{CC}$ or $0V$ Chip Disabled $t_A = 85^{\circ}C$ , $V_{CC} = 2.2V$			20	$\mu A$
Maximum Data Retention Current (Note 2)	$I_{DR}$	$V_{CC} = 1.2V$ , $V_{IN} = V_{CC}$ or $0$ Chip Disabled, $t_A = 85^{\circ}C$			5	$\mu A$

1. This device assumes a standby mode if the chip is disabled ( $\overline{CE1}$  high or  $CE2$  low). It will also go into a standby mode whenever if both  $UB$  and  $LB$  are high. In order to achieve low standby current all inputs must be within 0.2 volts of either  $V_{CC}$  or  $V_{SS}$ .
2. The Chip is Disabled when  $\overline{CE1}$  is high or  $CE2$  is low. The Chip is Enabled when  $\overline{CE1}$  is low and  $CE2$  is high.

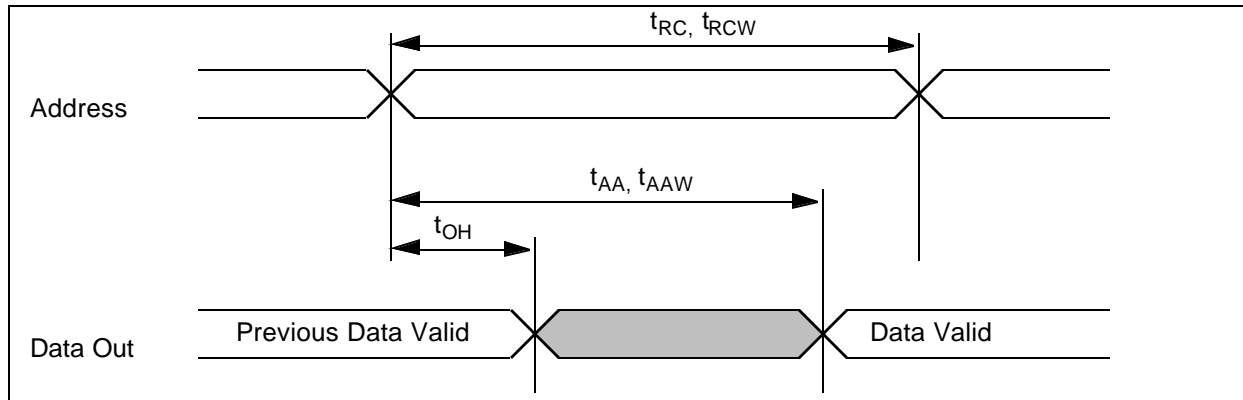
**TABLE 6: Timing Test Conditions**

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5V_{CC}$
Output Loading	30 pF
Operating Temperature	-40 to +85°C

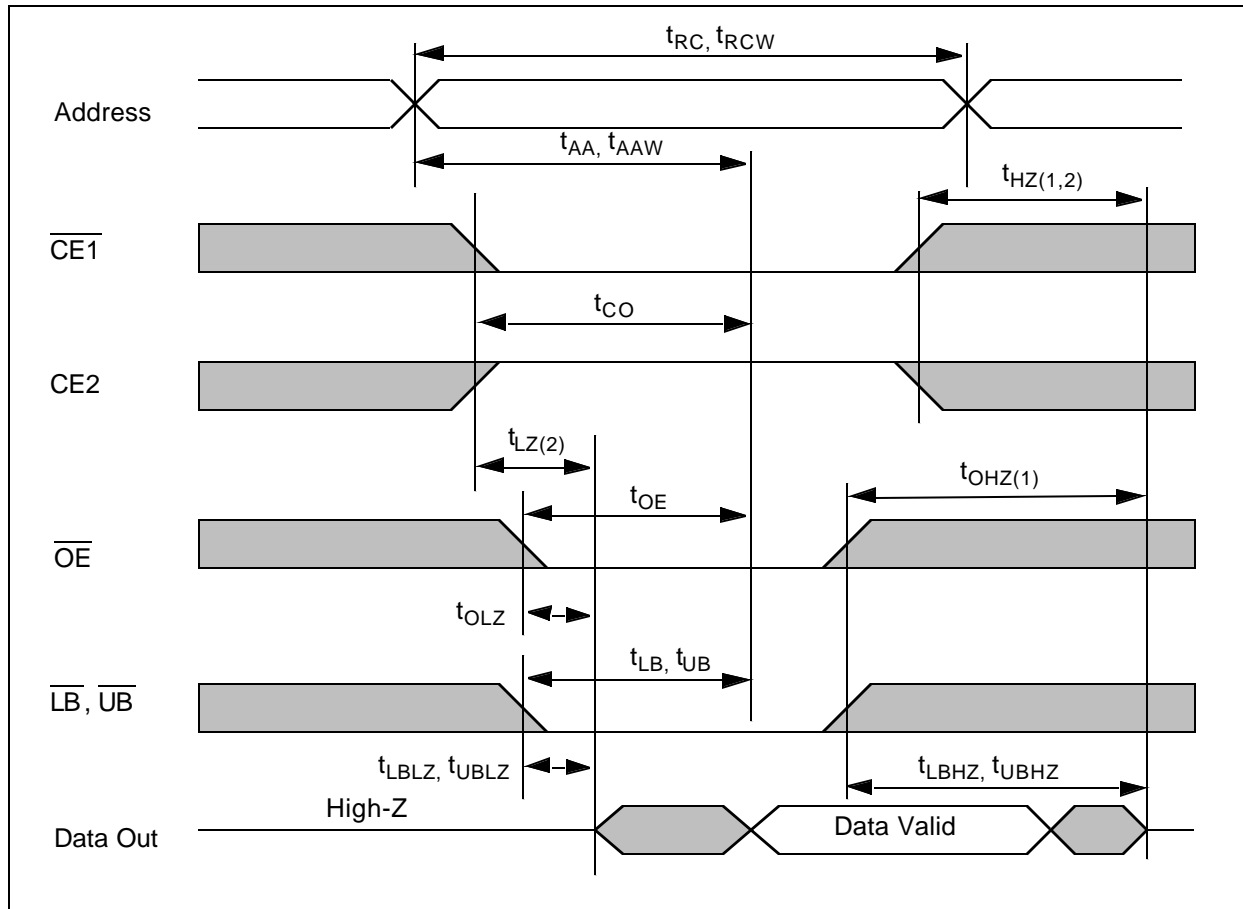
**TABLE 7: Timing**

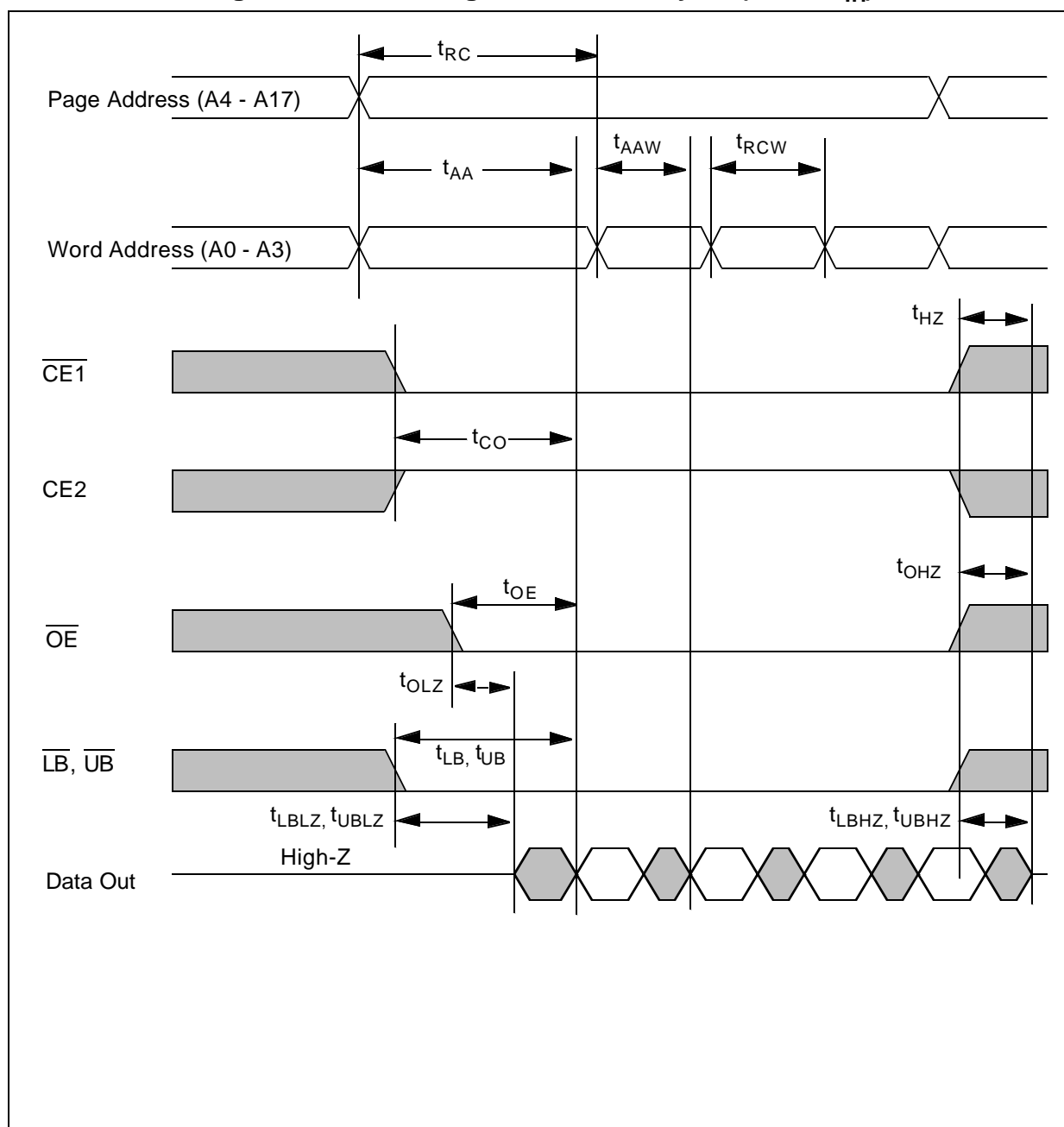
Item	Symbol	$V_{CCQ} = 1.65 - 2.2 V$		$V_{CCQ} = 1.8 - 2.2 V$		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	85		70		ns
Address Access Time (Random Access)	$t_{AA}$		85		70	ns
Address Access Time (Word Mode)	$t_{AAW}$		85		70	ns
Chip Enable to Valid Output	$t_{CO}$		85		70	ns
Output Enable to Valid Output	$t_{OE}$		30		25	ns
Byte Select to Valid Output	$t_{LB}, t_{UB}$		85		70	ns
Chip Enable to Low-Z output	$t_{LZ}$	10		10		ns
Output Enable to Low-Z Output	$t_{OLZ}$	5		5		ns
Byte Select to Low-Z Output	$t_{LBZ}, t_{UBZ}$	10		10		ns
Chip Disable to High-Z Output	$t_{HZ}$	0	20	0	20	ns
Output Disable to High-Z Output	$t_{OHZ}$	0	20	0	20	ns
Byte Select Disable to High-Z Output	$t_{LBHZ}, t_{UBHZ}$	0	20	0	20	ns
Output Hold from Address Change	$t_{OH}$	10		10		ns
Write Cycle Time	$t_{WC}$	85		70		ns
Chip Enable to End of Write	$t_{CW}$	50		50		ns
Address Valid to End of Write	$t_{AW}$	40		40		ns
Byte Select to End of Write	$t_{LBW}, t_{UBW}$	50		50		ns
Write Pulse Width	$t_{WP}$	40		40		ns
Address Setup Time	$t_{AS}$	0		0		ns
Write Recovery Time	$t_{WR}$	0		0		ns
Write to High-Z Output	$t_{WHZ}$		20		20	ns
Data to Write Time Overlap	$t_{DW}$	40		40		ns
Data Hold from Write Time	$t_{DH}$	0		0		ns
End Write to Low-Z Output	$t_{OW}$	5		5		ns

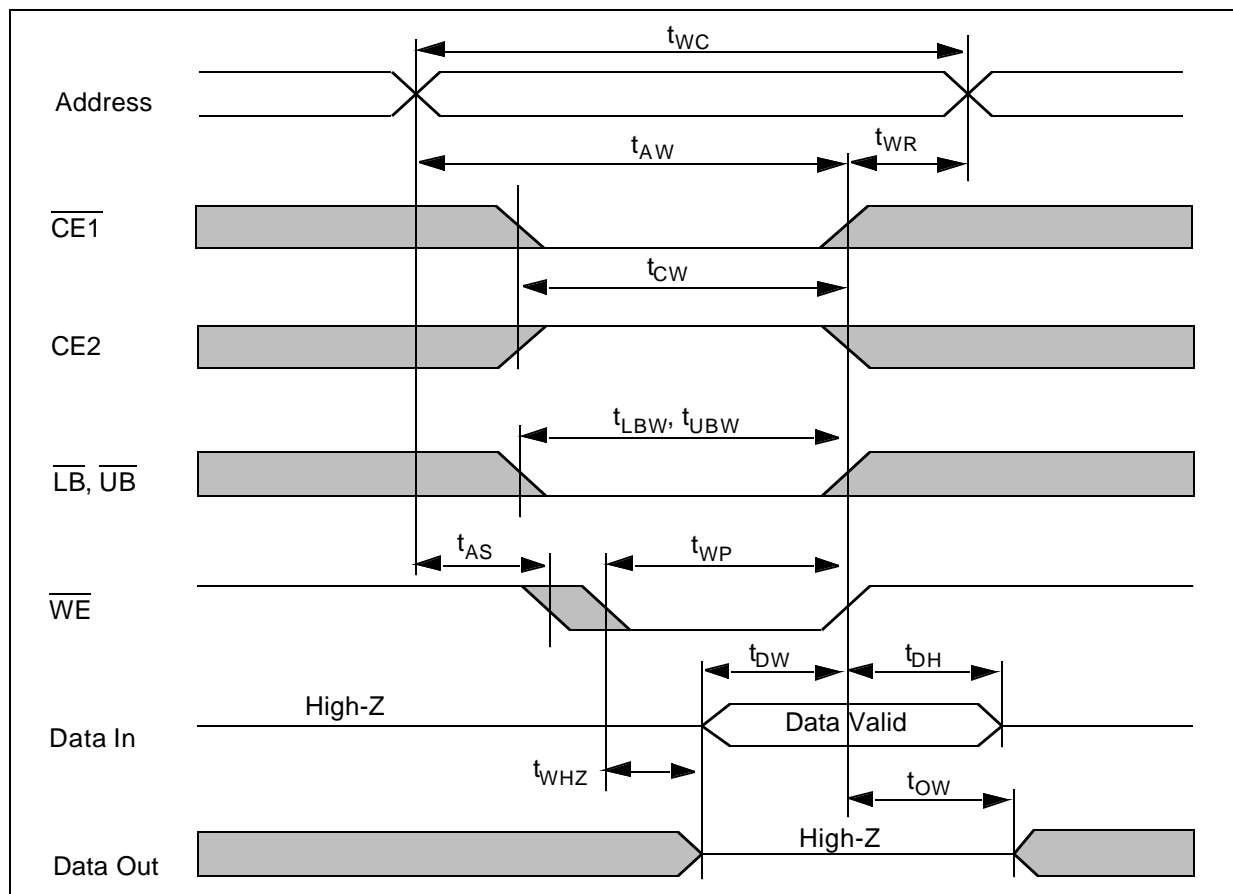
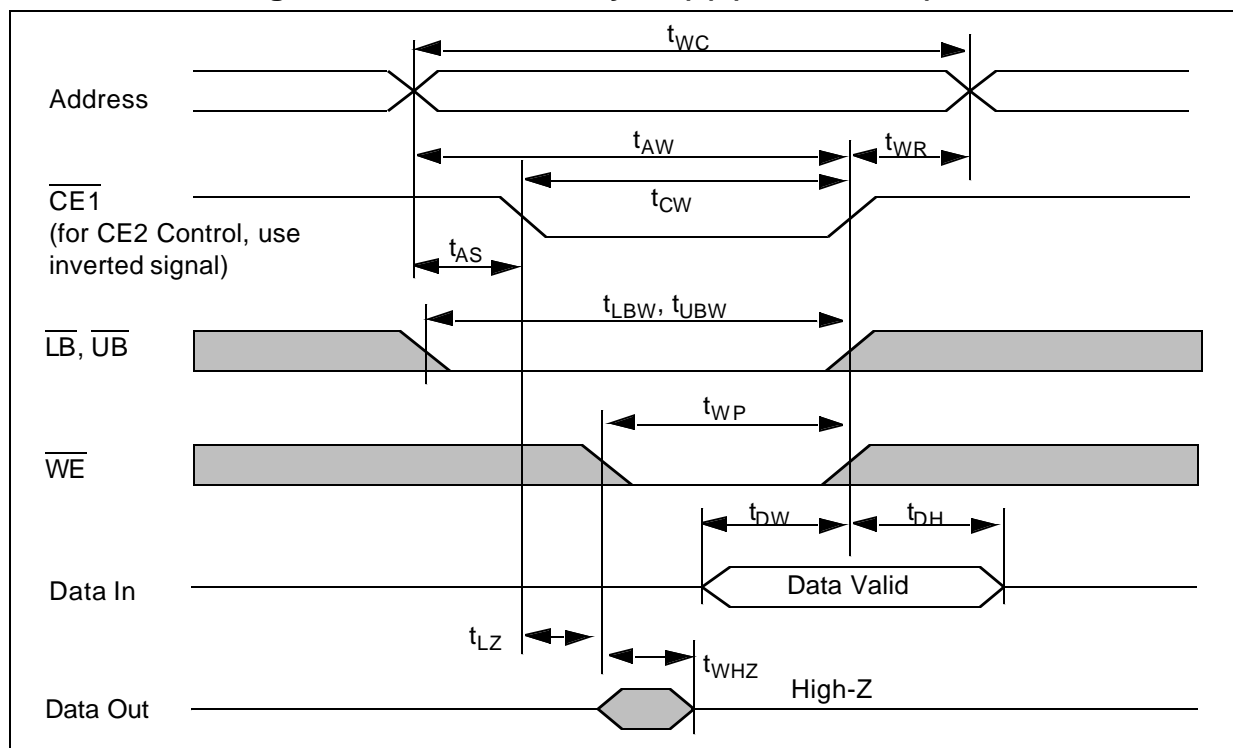
**FIGURE 4: Timing of Read Cycle (1) ( $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{WE}} = V_{\text{IH}}$ )**



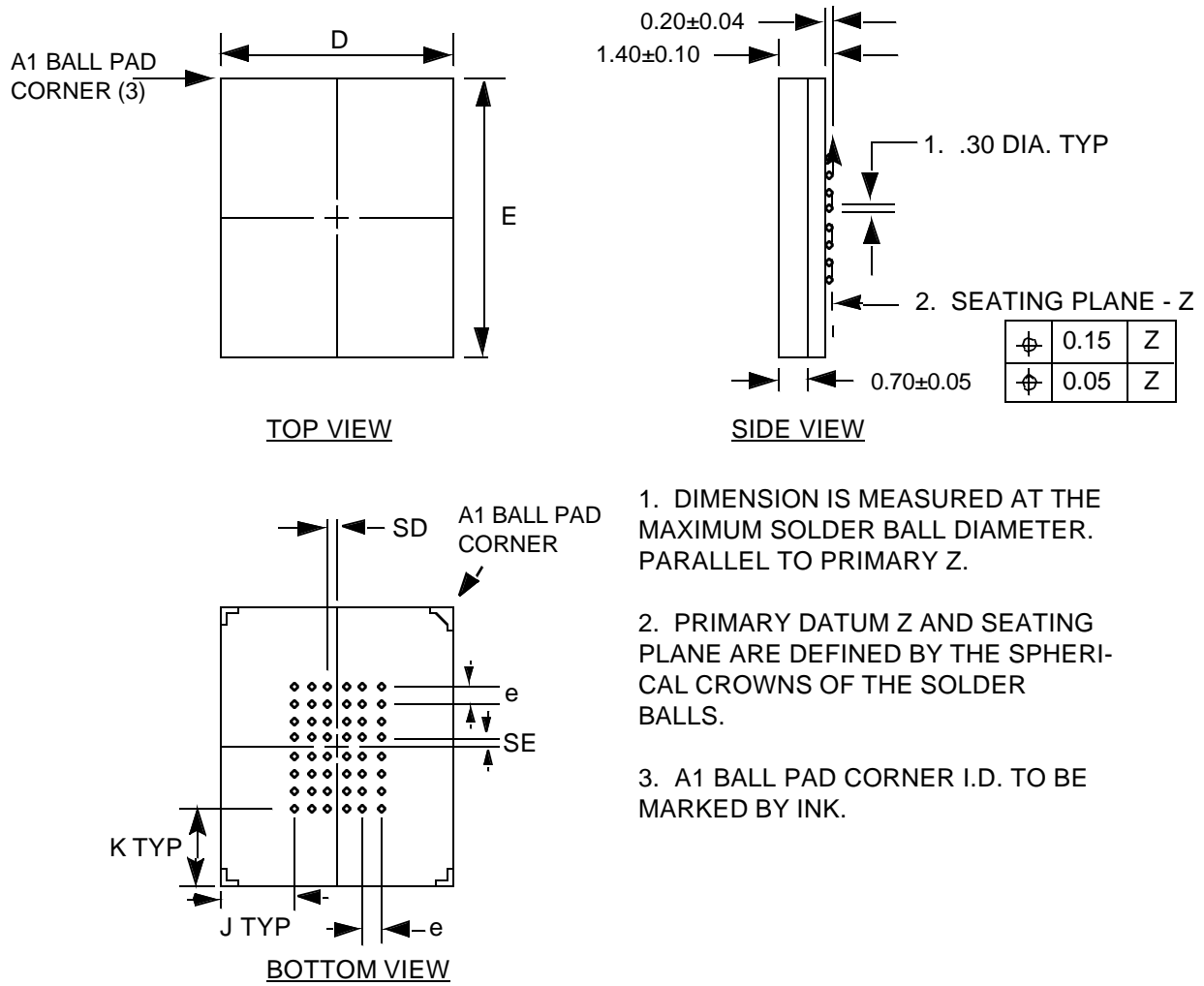
**FIGURE 5: Timing Waveform of Read Cycle (2) ( $\overline{\text{WE}} = V_{\text{IH}}$ )**



**FIGURE 6: Timing Waveform of Page Mode Read Cycle ( $\overline{WE} = V_{IH}$ )**

**FIGURE 7: Timing Waveform of Write Cycle (1) ( $\overline{\text{WE}}$  control)****FIGURE 8: Timing Waveform of Write Cycle (2) ( $\overline{\text{CE1}}$  Control)**

**FIGURE 9: BALL GRID ARRAY PACKAGING**



**TABLE 8: Dimensions (mm)**

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
8.0	10.0	0.375	0.375	2.125	2.375	FULL



**TABLE 9: Revision History**

Revision	Date	Change Description
A	Jan. 1, 2001	Initial Advance Release
B	Mar 2001	Corrected voltage in table 7: timing

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