ESS Technology, Inc.

# ES4438
# DVD Processor
# Product Brief

## DESCRIPTION

Built on ESS's proprietary and flexible Programmable Multimedia Processor architecture, the ES4438 DVD decoder combines audio/video stream data processing, system control and housekeeping functions, video postprocessing, and display format encoding in an industry-standard 208-pin PQFP package, enabling various DVD-based multimedia electronics to be built with minimal external components. Topped with speed enhancement and design optimization, the ES4438 has all the features supported by ESS's highly acclaimed Swan™ series of decoder ICs, plus added features in DVD-Audio support, progressive scan video output, and built-in TV encoder and video DACs.

The ES4438 includes two parallel processing units and hardware resources for implementing specialized encoding and decoding tasks. To maximize operational efficiency, these processing units and hardware resources are interconnected with two separate data buses, each with its own DMA unit and interface to external memory, enabling simultaneous parallel execution of system commands and data processing. The two processing units, a RISC processor and a vector engine, are independently programmable, and each has its own on-chip cache memory. The RISC processor and its associated hardware units perform bit stream parsing, control audio data output, transfer video and audio data to the vector engine and service system control and housekeeping functions. The vector engine and associated hardware units perform audio and video microcode processing required by A/V standards such as Dolby Digital™, DTS™, MPEG and JPEG. These processing tasks include audio DSP, video motion compensation and estimation, loop filtering, discrete cosine transforms (DCT) and inverse DCT, quantization and inverse quantization, and zig-zag scanning.

To support a wide range of system platforms and reduce overall system cost, the ES4438 features both parallel and serial drive interface for system MPEG A/V data stream input, industry standard-I²S bus for audio data input and output, direct system EPROM and SDRAM access for high-speed command fetching and audio/video data buffering, and selection of direct video output to TV or discrete YUV pixel data output for special video signal processing. In addition, the ES4438 provides a set of multipurpose auxiliary pins for customizing DVD system controls.

On top of the ES4438's high performance architecture, ESS has developed a set of highly efficient and powerful firmware for the chip, based on many years of engineering experience in consumer video electronics. As a result, the ES4438 can provide best solutions for high-end DVD player, portable DVD, car DVD, DVD HiFi, Web DVD, set-top box, and other DVD-based internet appliances and digital home systems at low cost.

## FEATURES

- Single-chip DVD solution in a 208-pin PQFP package.
- Dual power supplies, 3.3 V and 2.65 V, for low-power operation.
- Integrated 32-bit RISC processor for system host, eliminating requirements of an external host CPU.
- Support DVD-Video, DVD-Audio, VideoCD 1.1, 2.0, and 3.0, Super VideoCD (SVCD), OKO, CD-DA, MP3, Compact Flash, and Kodak Picture-CD.
- Glueless interface to IDE/ATAPI DVD drives, 8-bit A/V bus (DCI) DVD drives from Sony, Panasonic and Sanyo, and serial interface DVD drives from Thomson.
- Direct interface to 8- or 16-bit SDRAM of up to 128-Mb capacity at a variety of speed grades.
- Direct interface to up to 4 banks of 8- or 16-bit EPROM or Flash EPROM with up to 4-MB in each bank.
- Provide automatic firmware updating on Flash EPROM through DVD drive for fast and easy system upgrade.

### Video

- MPEG-1 system, MPEG-2 program and JPEG decoding streams supported.
- Built-in NTSC/PAL/480P encoder.
- Video outputs are compliant with both Macrovision 7.1 for interlaced video (NTSC and PAL) and Macrovision AGC 1.03 for 480-pixel progressive scan.
- Field-adaptive de-interlacing for progressive scan video output provides clearer and more stable display.
- Four built-in 10-bit Video DAC provides simultaneous video outputs of Composite and S-video, and Composite and YUV.
- Selectable 8-bit CCIR 601 4:2:2 YUV outputs.
- 8-bit On-Screen Display (OSD) controller with 3-bit blending provides display with 256 colors in 8 degrees of transparency
- On-chip Subpicture Unit (SPU) decoder supports karaoke lyric, and subtitle display functions.
- SmartStream™ for video error concealment.
- SmartScale™ for NTSC to PAL conversion and vice versa.
- SmartZoom™ for motion zoom and pan.

### Audio

- Dolby Digital™ (AC-3), DVD-Audio, Pro Logic, Digital Theater System (DTS), MPEG-1 layer 2 and 3 Audio (MP3) and High Definition Compatible Digital (HDCD) decoding.
- On-chip Dolby Digital™ (AC-3) and DTS 5.1 channel decoding and output.
- Dolby Digital™ and DTS™ S/PDIF digital audio output
- Dolby Digital™ Class A, DTS™ and HDCD™ certified.
- Meridian Lossless Packing (MLP) decoding, Linear PCM for DVD-Audio, and built-in Content Protection for Prerecorded Media (CPPM) decryption.
- Sensaura Virtual Surround Sound supported.

## PINOUT

Figure 1 shows the ES4438 device pinout.

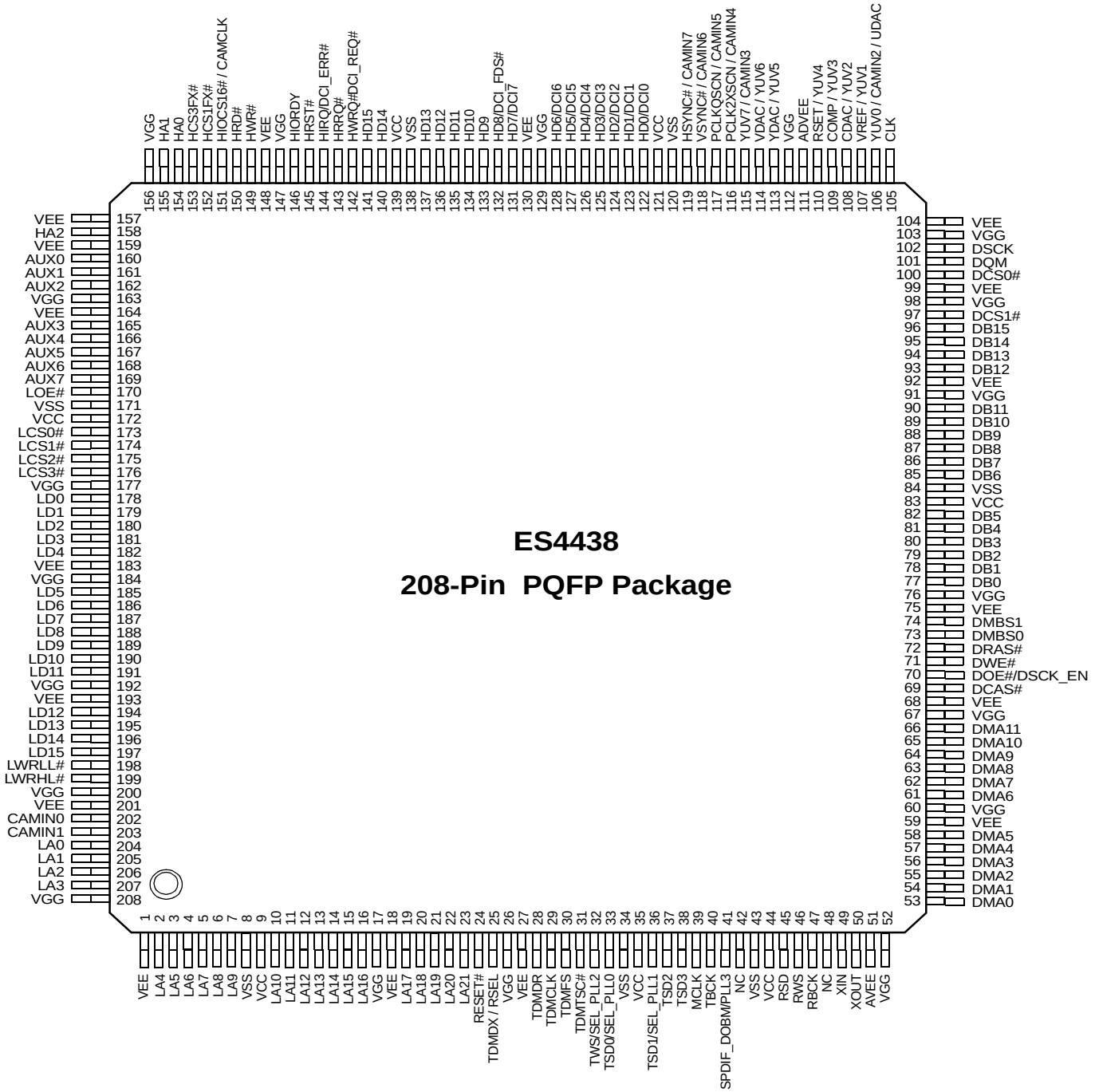


Figure 1 ES4438 Device Pinout

## ES4438 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES4438.

Table 1 ES4438 Pin Description

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VEE</td><td>1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201</td><td>I</td><td>3.3V power supply.</td></tr>
<tr><td>VGG</td><td>17, 26, 52, 60, 67, 76, 91, 98, 103, 112, 129, 147, 156, 163, 177, 184, 192, 200, 208</td><td>I</td><td>Ground for 3.3V supply.</td></tr>
<tr><td>LA[21:0]</td><td>23:19, 16:10, 7:2, 207:204</td><td>O</td><td>Device address output.</td></tr>
<tr><td>VSS</td><td>8, 34, 43, 84, 120, 138, 171</td><td>I</td><td>Ground for 2.65V supply.</td></tr>
<tr><td>VCC</td><td>9, 35, 44, 83, 121, 139, 172</td><td>I</td><td>2.65V digital logic power supply.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data.</td></tr>
<tr><td>RSEL</td><td>I</td><td>ROM select.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit ROM</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection at reset time. The matrix below lists the available clock frequencies and their respective PLL bit settings.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Output</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>VCO doesn’t work.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>27 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>54 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>121.5 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>81 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>94.5 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>108 MHz</td></tr>
</table></td></tr>
<tr><td>TSD0</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD1</td><td rowspan="2">36</td><td>O</td><td>Audio transmit serial data port 1.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD[2]</td><td>37</td><td>O</td><td>Audio transmit serial data output 2.</td></tr>
<tr><td>TSD[3]</td><td>38</td><td>O</td><td>Audio transmit serial data output 3.</td></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>I/O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPDIF_DOBM</td><td rowspan="2">41</td><td>O</td><td>S/PDIF output.</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select.
<table>
<tr><th>SEL_PLL3</th><th>Clock Source</th></tr>
<tr><td>0</td><td>Crystal oscillator</td></tr>
<tr><td>1</td><td>DCLK input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>42, 48</td><td></td><td>No connect pins. Leave open.</td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync.</td></tr>
</table>

Table 1 ES4438 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock.</td></tr>
<tr><td>XIN</td><td>49</td><td>I</td><td>Crystal input.</td></tr>
<tr><td>XOUT</td><td>50</td><td>O</td><td>Crystal output.</td></tr>
<tr><td>AVEE</td><td>51</td><td>I</td><td>Analog power for PLL.</td></tr>
<tr><td>DMA[11:0]</td><td>66:61, 58:53</td><td>O</td><td>DRAM address bus [11:0].</td></tr>
<tr><td>DCAS#</td><td>69</td><td>O</td><td>DRAM column address strobe, active low.</td></tr>
<tr><td>DOE#</td><td rowspan="2">70</td><td>O</td><td>DRAM output enable, active low.</td></tr>
<tr><td>DSCK_EN</td><td>I</td><td>DRAM clock enable, active low.</td></tr>
<tr><td>DWE#</td><td>71</td><td>O</td><td>DRAM write enable, active low.</td></tr>
<tr><td>DRAS#</td><td>72</td><td>O</td><td>DRAM row address strobe, active low.</td></tr>
<tr><td>DMBS0</td><td>73</td><td>O</td><td>SDRAM bank select 0.</td></tr>
<tr><td>DMBS1</td><td>74</td><td>O</td><td>SDRAM bank select 1.</td></tr>
<tr><td>DB[15:0]</td><td>96:93, 90:85, 82:77</td><td>I/O</td><td>DRAM data bus [15:0].</td></tr>
<tr><td>DCS[1:0]#</td><td>97,100</td><td>O</td><td>SDRAM chip select [1:0], active low.</td></tr>
<tr><td>DQM</td><td>101</td><td>O</td><td>Data input/output mask.</td></tr>
<tr><td>DSCK</td><td>102</td><td>O</td><td>Output clock to SDRAM.</td></tr>
<tr><td>DCLK</td><td>105</td><td>I</td><td>27-MHz clock input to PLL.</td></tr>
<tr><td>YUV0</td><td rowspan="3">106</td><td>O</td><td>YUV0 pixel output data.</td></tr>
<tr><td>CAMIN2</td><td>I</td><td>Camera input 2.</td></tr>
<tr><td>UDAC</td><td>O</td><td>Video DAC output.
<table>
<tr><th>YDAC</th><th>UDAC</th><th>VDAC</th><th>CDAC</th></tr>
<tr><td>Y</td><td>C</td><td>Composite</td><td>C</td></tr>
<tr><td>Y</td><td>Composite</td><td>Composite</td><td>C</td></tr>
<tr><td>Y</td><td>U</td><td>Composite</td><td>V</td></tr>
<tr><td>Y</td><td>U</td><td>C</td><td>V</td></tr>
</table>
Y: Luma component for YUV and Y/C processing.<br>C: Chrominance signal for Y/C processing.<br>U: Chrominance component signal for YUV mode.<br>V: Chrominance component signal for YUV mode.</td></tr>
<tr><td>YUV1</td><td>107</td><td>O</td><td>YUV1 pixel output data.</td></tr>
<tr><td>VREF</td><td rowspan="2">107</td><td>I</td><td>0.1 µF analog ground input for internal common-mode reference voltage generation.</td></tr>
<tr><td>YUV2</td><td>O</td><td>YUV2 pixel output data.</td></tr>
<tr><td>CDAC</td><td>108</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 106.</td></tr>
<tr><td>YUV3</td><td>109</td><td>O</td><td>YUV3 pixel output data.</td></tr>
<tr><td>COMP</td><td rowspan="2">109</td><td>I</td><td>Compensation capacitor input.</td></tr>
<tr><td>YUV4</td><td>110</td><td>O</td><td>YUV4 pixel output data.</td></tr>
<tr><td>RSET</td><td rowspan="2">110</td><td>I</td><td>DAC current adjustment resistor input.</td></tr>
<tr><td>ADVEE</td><td>111</td><td>I</td><td>Analog power for DAC.</td></tr>
<tr><td>YUV5</td><td>113</td><td>O</td><td>YUV5 pixel output data.</td></tr>
<tr><td>YDAC</td><td rowspan="2">113</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 106.</td></tr>
<tr><td>YUV6</td><td>114</td><td>O</td><td>YUV6 pixel output data.</td></tr>
<tr><td>VDAC</td><td rowspan="2">114</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 106.</td></tr>
<tr><td>YUV7</td><td>115</td><td>O</td><td>YUV7 pixel output data.</td></tr>
<tr><td>CAMIN3</td><td rowspan="2">115</td><td>I</td><td>Camera input 3.</td></tr>
<tr><td>PCLK2XSCN</td><td>116</td><td>O</td><td>27-MHz video output pixel clock.</td></tr>
<tr><td>CAMIN4</td><td rowspan="2">116</td><td>I</td><td>Camera input 4.</td></tr>
<tr><td>PCLKQSCN</td><td>117</td><td>O</td><td>13.5-MHz video output pixel clock.</td></tr>
<tr><td>CAMIN5</td><td rowspan="2">117</td><td>I</td><td>Camera input 5.</td></tr>
<tr><td>VSYNC#</td><td>118</td><td>I/O</td><td>Vertical sync, active low.</td></tr>
<tr><td>CAMIN6</td><td rowspan="2">118</td><td>I</td><td>Camera input 6.</td></tr>
<tr><td>HSYNC#</td><td>119</td><td>I/O</td><td>Horizontal sync, active low.</td></tr>
<tr><td>CAMIN7</td><td rowspan="2">119</td><td>I</td><td>Camera input 7.</td></tr>
</table>

Table 1 ES4438 Pin Description (Continued)

| Name | Number | I/O | Definition |
|---|---|---|---|
| HD[7:0] | 131, 128:122 | I/O | Host data I/O [7:0]. |
| DCI[7:0] | | I/O | DVD channel data I/O [7:0]. |
| AUX1[7:0] | | I/O | Aux1 data I/O [7:0]. |
| HD[8] | 132 | I/O | Host data bus 8. |
| DCI_FDS# | | I/O | DVD input sector start. |
| AUX2[0] | | I/O | Aux2 data I/O 0. |
| HD[15:9] | 141:140, 137: 133 | I/O | Host data bus [15:9]. |
| AUX2[7:1] | | I/O | Aux2 data I/O [7:1]. |
| HWRQ# | 142 | O | Host write request. |
| DCI_REQ# | | O | DVD control interface request. |
| AUX4[1] | | I/O | Aux4 data I/O 1. |
| HRRQ# | 143 | O | Host read request. |
| AUX4[0] | | I/O | Aux4 data I/O 0. |
| HIRQ | 144 | I/O | Host interrupt. |
| DCI_ERR# | | I/O | DVD channel data error. |
| AUX4[7] | | I/O | Aux4 data I/O 7. |
| HRST# | 145 | O | Host reset. |
| AUX3[5] | | I/O | Aux3 data I/O 5. |
| HIORDY | 146 | I | Host I/O ready. |
| AUX3[3] | | I/O | Aux3 data I/O 3. |
| HWR# | 149 | I/O | Host write. |
| DCI_CLK | | I/O | DVD channel data clock. |
| AUX4[5] | | I/O | Aux4 data I/O 5. |
| HRD# | 150 | O | Host read. |
| DCI_ACK# | | O | DVD channel data valid. |
| AUX4[6] | | I/O | Aux4 data I/O 6. |
| HIOCS16# | 151 | I | Device 16-bit data transfer. |
| CAMCLK | | I | Camera port pixel clock input. |
| AUX3[4] | | I/O | Aux3 data I/O 4. |
| HCS1FX# | 152 | O | Host select 1. |
| AUX3[7] | | I/O | Aux3 data I/O 7. |
| HCS3FX# | 153 | O | Host select 3. |
| AUX3[6] | | I/O | Aux3 data I/O 6. |
| HA[2:0] | 158, 155:154 | I/O | Host address bus. |
| AUX4[4:2] | | I/O | Aux4 data I/Os [4:2]. |
| AUX[7:0] | 169:165,162:160 | I/O | Auxiliary ports. |
| LOE# | 170 | O | Device output enable, active low. |
| LCS[3:0]# | 176:173 | O | Chip select [3:0], active low. |
| LD[15:0] | 197:194, 191:185, 182:178 | I/O | EPROM device data bus. |
| LWRLL# | 198 | O | Device write enable, active low. |
| LWRHL# | 199 | O | Device write enable, active low. |
| CAMIN0 | 202 | I | Camera input 0. |
| CAMIN1 | 203 | I | Camera input 1. |

## SYSTEM BLOCK DIAGRAM

Figure 2 shows the ES4438 system block diagram.

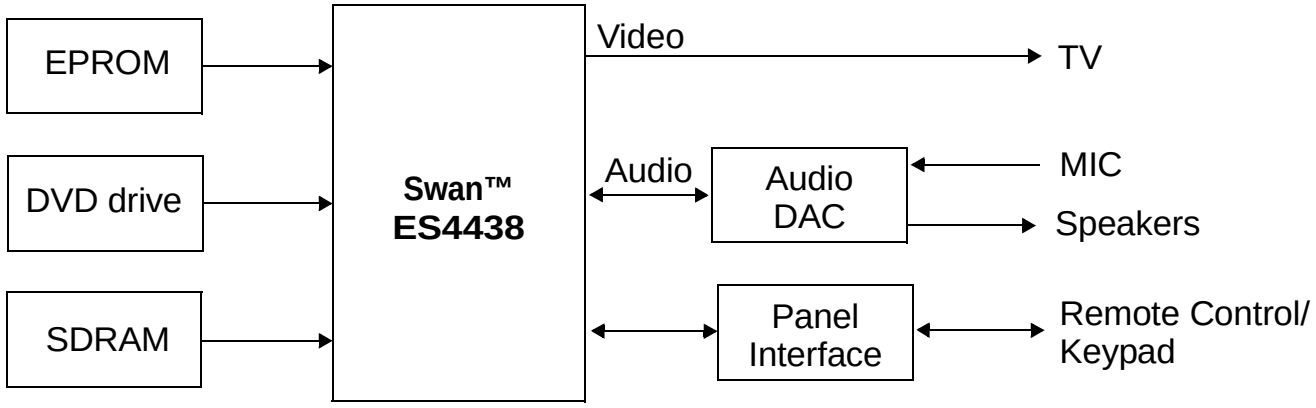


Figure 2 ES4438 System Block Diagram

## ORDERING INFORMATION

| Part Number | Description | Package |
|---|---|---|
| ES4438 | DVD Processor | 208-pin PQFP |

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: 510-492-1088
Fax: 510-492-1098