

ESA8UN324(2/4)-(60/70)(J/T)(G/S)-S

32MByte (8M x 32) CMOS EDO DRAM Module

General Description

The ESA8UN324(2/4)-(60/70)(J/T)(G/S)-S is a high performance, EDO (Extended Data Out) 32-megabyte dynamic RAM module organized as 4M words by 32bits, in a 72-pin, leadless, single-in-line memory module (SIMM) package. ESA8UN3242 supports 2K refresh. ESA8UN3244 supports 4K refresh.

The module utilizes sixteen, Fujitsu MB811(7/6)405A-(60/70)PJ CMOS 4Mx4 EDO dynamic RAM in a surface mount package on an epoxy laminate substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

Control lines provided are such that byte control is possible.

Features

- High Density: 32MByte
- Fast Access Time of 60/70 ns (max.)
- Low Power:
 - Active (60/70 ns)
 - 4.7/4.0 W (max.) - 2K
 - 3.4/2.9 W (max.) - 4K
 - 176mW (max.) - Standby (TTL)
 - 88mW (max.) - Standby (CMOS)
- TTL-compatible inputs and outputs
- Separate power and ground planes
- Single power supply of $5V \pm 10\%$
- Height: 1.00 inch

ABSOLUTE MAXIMUM RATINGS

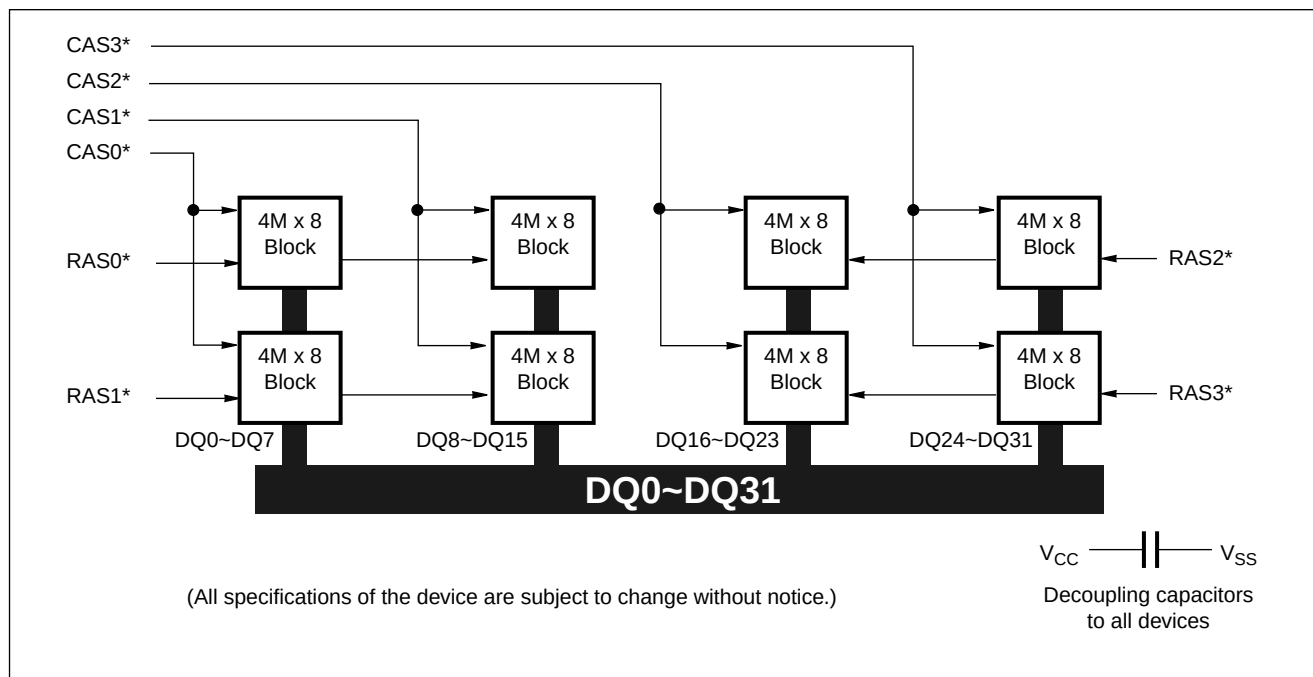
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-1 to +7.0	V
Power Dissipation	P_T	8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	-50 to +50	mA

RECOMMENDED DC OPERATING CONDITIONS

($T_A = 0$ to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.4	-	$V_{CC}+1$	V
V_{IL}	Input Low voltage	-1	-	0.8	V

Functional Diagram



- Notes:
1. A0 ~ A10/A11 to all devices (A11 is NC for 2K refresh module).
 2. WE* to all devices.
 3. OE* of all devices is grounded.
 4. Each 4Mx8 Block consists of two 4Mx4 devices.

ESA8UN324(2/4)-(60/70)(J/T)(G/S)-S

Pin Name

A0~A10†	Addresses for 2K Refresh Module	WE*	Write Enable
A0~A11	Row Addresses for 4K Refresh Module	PD1~PD4	Presence Detects
A0~A9	Column Addresses for 4K Refresh Module	V _{CC}	Power Supply
DQ0~DQ31	Data Inputs/Outputs	V _{SS}	Ground
CAS0*~CAS3*	Column Address Strokes	NC	No Connection
RAS0~RAS3	Row Address Strokes		

Presence Detect Pins

Pin	-60	-70
PD1	NC	NC
PD2	V _{SS}	V _{SS}
PD3	NC	V _{SS}
PD4	NC	NC

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V _{SS}	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	CAS0*	58	DQ28
5	DQ17	23	DQ21	41	CAS2*	59	V _{CC}
6	DQ2	24	DQ6	42	CAS3*	60	DQ29
7	DQ18	25	DQ22	43	CAS1*	61	DQ13
8	DQ3	26	DQ7	44	RAS0*	62	DQ30
9	DQ19	27	DQ23	45	RAS1*	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	A11†	47	WE*	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	RAS3*	51	DQ9	69	PD3
16	A4	34	RAS2*	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

†: A11 is NC for 2K refresh module.

ESA8UN324(2/4)-(60/70)(J/T)(G/S)-S

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0$ to $+70^\circ C$)

Parameter	Symbol	Test Condition	Refresh	60		70		Unit	Note
				Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	RAS*, CAS* cycling; $t_{RC} = \min.$	2K	-	856	-	736	mA	1, 2
			4K	-	616	-	536		
Standby current	I_{CC2}	TTL Interface RAS*, CAS* = V_{IH} $D_{out} = \text{High-Z}$		-	32	-	32	mA	
		CMOS Interface RAS*, CAS* $\geq V_{CC} - 0.2V$ $D_{out} = \text{High-Z}$		-	16	-	16		
RAS* -only Refresh Current	I_{CC3}	CAS* = V_{IH} ; RAS*, Address cycling @ $t_{RC} = \min$	2K	-	856	-	720	mA	2
			4K	-	616	-	536		
CAS*-before-RAS* Refresh Current	I_{CC4}	RAS*, CAS* cycling @ $t_{RC} = \min.$	2K	-	856	-	736	mA	
			4K	-	616	-	536		
Fast Page Mode Current	I_{CC5}	RAS* = V_{IL} ; CAS*, Address cycling @ $t_{PC} = \min$	2K	-	856	-	736	mA	1, 3
			4K	-	616	-	536		
Input Leakage Current	I_{LI}	$0V \leq V_{in} \leq V_{CC} + 0.5V$		-160	160	-160	160	μA	
Output Leakage Current	I_{LO}	$0V \leq V_{out} \leq V_{CC}$ $D_{out} = \text{Disable}$		-20	20	-20	20	μA	
Output High Voltage	V_{OH}	High $I_{out} = -5$ mA		2.4	-	2.4	-	V	
Output Low Voltage	V_{OL}	Low $I_{out} = 4.5$ mA		-	0.4	-	0.4	V	

- Notes:
1. Values depend on load condition when the device is selected. Maximum Values are specified at the output open condition.
 2. Address can be changed once or less while RAS* = V_{IL} .
 3. Address can be changed once or less while CAS* = V_{IH} .

CAPACITANCE

($T_A = +25^\circ C$, $V_{CC} = 5.0V \pm 10\% = 10V$)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	85	pF	1
Input Capacitance (RAS0*~RAS3*)	C_{I2}	25	pF	1
Input Capacitance (CAS0*~CAS3*)	C_{I3}	25	pF	1
Input Capacitance (WE*)	C_{I4}	85	pF	1
Input/Output Capacitance (DQ0~DQ31)	$C_{I/O}$	12	pF	1, 2

- Notes:
1. Capacitance is measured with Boonton Meter or effective capacitance method.
 2. CAS* = V_{IH} to disable D_{out} .

ESA8UN324(2/4)-(60/70)(J/T)(G/S)-S

AC CHARACTERISTICS

(TA = 0 to +70°C, V_{CC} = 5.0V±10%V, V_{SS} = 0V)

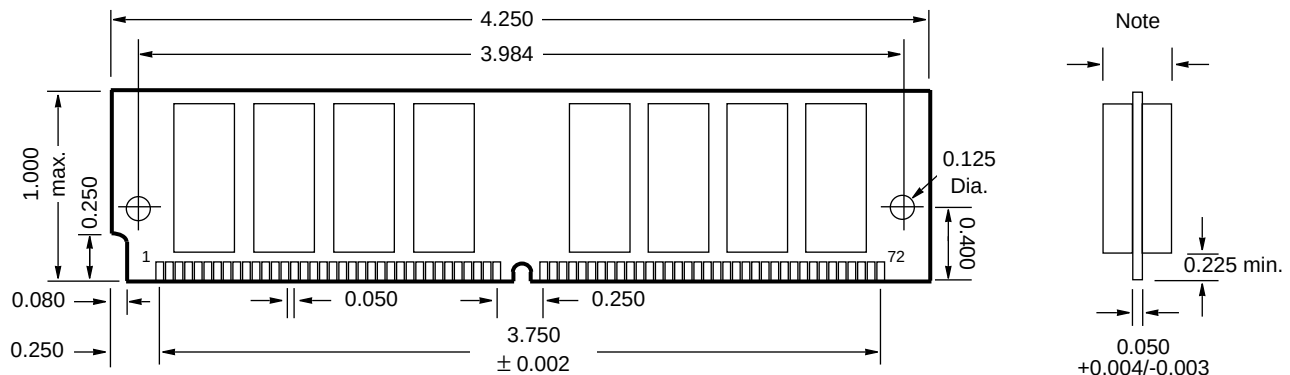
Parameter	Symbol	60		70		Unit	Notes
		Min	Max	Min	Max		
Random read/write cycle time	t _{RC}	110	-	130	-	ns	
Access time from RAS*	t _{RAC}	-	60	-	70	ns	3, 4
Access time from CAS*	t _{CAC}	-	15	-	20	ns	3, 4, 5
Access time from column address	t _{AA}	-	30	-	35	ns	3, 10
Output buffer turn-off time	t _{OFF}	0	15	0	17	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	ns	2
RAS* precharge time	t _{RP}	40	-	50	-	ns	
RAS* pulse width	t _{RAS}	60	10000	70	10000	ns	
RAS* hold time	t _{RS}	15	-	20	-	ns	
CAS* hold time	t _{CS}	60	-	70	-	ns	
CAS* pulse width	t _{CAS}	15	10000	20	10000	ns	
RAS* to CAS* delay time	t _{RCD}	20	45	20	50	ns	4
RAS* to column address delay time	t _{RAD}	15	30	15	35	ns	10
CAS* to RAS* precharge time	t _{CRP}	5	-	5	-	ns	
Row address set-up time	t _{ASR}	0	-	0	-	ns	
Row address hold time	t _{RAH}	10	-	10	-	ns	
Column address set-up time	t _{ASC}	0	-	0	-	ns	
Column address hold time	t _{CAH}	12	-	15	-	ns	
Column address to RAS* lead time	t _{RAL}	30	-	35	-	ns	
Read command set-up time	t _{RCS}	5	-	5	-	ns	
Read command hold time to CAS*	t _{RCH}	0	-	0	-	ns	8
Read command hold time to RAS*	t _{RRH}	0	-	0	-	ns	
Write command hold time	t _{WCH}	12	-	15	-	ns	
Write command pulse width	t _{WP}	10	-	15	-	ns	
Write command to RAS* lead time	t _{RWL}	15	-	20	-	ns	
Write command to CAS* lead time	t _{CWL}	15	-	20	-	ns	
Data-in set-up time	t _{DS}	0	-	0	-	ns	9
Data-in hold time	t _{DH}	12	-	15	-	ns	9
Refresh period	(2048 cycles)	t _{REF}	-	32	-	32	ms
	(4096 cycles)		-	64	-	64	ms
Write command set-up time	t _{WCS}	0	-	0	-	ns	7
CAS* set-up time (CBR refresh)	t _{CSR}	10	-	10	-	ns	1
CAS* hold time (CBR refresh)	t _{CHR}	10	-	15	-	ns	1
RAS* precharge to CAS* hold time	t _{RPC}	5	-	5	-	ns	
Access time from CAS* precharge	t _{CPA}	-	35	-	40	ns	3, 11
Hyper Page mode cycle time	t _{HPC}	25	-	30	-	ns	
CAS* precharge time (Hyper Page)	t _{CP}	8	-	10	-	ns	
RAS* pulse width (Hyper Page)	t _{RASP}	—	200000	—	200000	ns	12

ESA8UN324(2/4)-(60/70)(J/T)(G/S)-S

- Notes:
1. An initial pulse of at least 200 μ s is required after power-up followed by a minimum of eight RAS* cycles before device operation is achieved.
 2. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.) and are assumed to be 5 ns for all inputs.
 3. Measure with a load equivalent of 2 TTL loads and 100pF.
 4. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) limit can be met; t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
 6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL} .
 7. t_{WCS} is a non restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data-out pin will remain at high impedance for the duration of the cycle.
 8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. These parameters are referenced to the CAS* leading edge in early write cycles.
 10. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA} .
 11. Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{ACP} .
 12. t_{RASC} defines RAS* pulse width in fast page mode cycles.

Physical Dimensions

72-pin SIMM



(All dimensions are in inches with ± 0.005 " tolerance unless otherwise specified. Do not scale drawing)

- Notes:
- Thickness = 0.350 for SOJ DRAM
 - = 0.150 for TSOP DRAM

ESA8UN324(2/4)-(60/70)(J/T)(G/S)-S

Worldwide Headquarters

Japan

Fujitsu Limited

Tel: +81 44 754 3753
Fax: +81 44 754 3332

1015 Kamiodanaka
Nakaharaku
Kawasaki 211
Japan

<http://www.fujitsu.co.jp/>

Asia

Tel: +65 336 1600
Fax: +65 336 1609

<http://www.fsl.com.sg/>

Fujitsu Microelectronics Asia PTE Limited

No. 51 Bras Basah Road
Plaza by the Park
#06-04/07
Singapore 0718

USA

Tel: +1 408 922 9000
Fax: +1 408 922 9179

Fujitsu Microelectronics Inc
3545 North First Street
San José CA 95134-1804
USA

Tel: +1 800 866 8608
Fax: +1 408 922 9179

Customer Response Center
Mon-Fri: 7am-5pm (PST)

<http://www.fujitsumicro.com/>

Europe

Tel: +49 6103 6900
Fax: +49 6103 6901

<http://www.fujitsu.ede.com/>

Fujitsu Mikroelektronik GmbH

Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany

All Right Reserved.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu Microelectronics, Inc. assumes no responsibility for inaccuracies.

The information conveyed in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu Limited, its subsidiaries, or Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. reserves the right to change products or specifications without notice.

No part of the publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Fujitsu Microelectronics, Inc.

