EDC8BV724(2/4)B-60(J/T)G-S

64MByte (8M x 72) CMOS EDO DRAM Module - 3.3V (ECC), Buffered

General Description

The EDC8BV724(2/4)B-60(J/T)G-S is a high performance, EDO (Extended Data Out) 64-megabyte dynamic RAM module organized as 8M words by 72 bits, in a 168-pins, dual-in-line (DIMM) memory module with ECC.

The module utilizes thirty-six, Fujitsu MB81V1(7/6)405B-60(PJ/FN) CMOS 4Mx4 EDO dynamic RAMs in a surface mount package on an epoxy laminate substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

Control lines provided are such that Dword control is possible. All signals are buffered (74LVT16244 or equivalent) except RAS, data and IDs.

Features

- High Density: 64MByte
- Fast Access Time of 60ns (max.)
- Low Power: 6.6W (max.) - Active (60ns): 2KR
  5.0W (max.) - Active (60ns): 4KR
  295mW (max.) - Standby (LVTTL)
  166mW (max.) - Standby (CMOS)
- LVTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.500 inch
- 2K/4K Refresh Cycles

ABSOLUTE MAXIMUM RATINGS

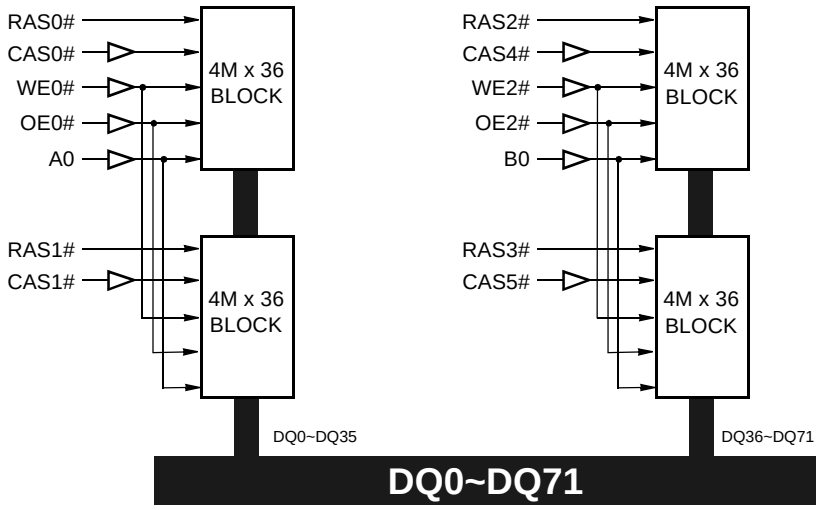
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Power Dissipation	P_T	38	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	-50 to +50	mA

RECOMMENDED DC OPERATING CONDITIONS

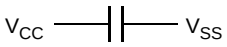
(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.0	-	V_{CC}+0.3	V
V_{IL}	Input Low voltage	-0.3	-	0.8	V

Functional Diagram



Notes:
1. All signals including PDs (with the exception of RAS#, data and IDs) are buffered.
2. Addresses A1~A10/A11 (A11 is NC for the 2K Refresh module) are connected to all DRAMs.
3. Each 4Mx36 block comprises of nine 4Mx4 EDO DRAMs.



Decoupling capacitors to all devices

All specifications of this device are subject to change without notice.

Pin Name

A0~A10, B0	Rows and Column Addresses for 2KR
A0~A11, B0	Row Addresses for 4KR
A0~A9, B0	Column Addresses for 4KR
DQ0~DQ71	Data Inputs/Outputs
WE0*, WE2*	Write Enable
RAS0*~RAS3*	Row Address Strobes
OE0*, OE2*	Output Enable
CAS0*, CAS1*, CAS4*, CAS5*	Column Address Strobes

V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection
PDE*	Presence Detect Enable
PD1~PD8	Presence Detect

PD	60ns
PD6	NC
PD7	NC

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	OE2* †	86	DQ36	128	NC
3	DQ1	45	RAS2*	87	DQ37	129	RAS3*
4	DQ2	46	CAS4* †	88	DQ38	130	CAS5* †
5	DQ3	47	NC	89	DQ39	131	NC
6	V_{CC}	48	WE2* †	90	V_{CC}	132	PDE*
7	DQ4	49	V_{CC}	91	DQ40	133	V_{CC}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V_{CC}	101	DQ49	143	V_{CC}
18	V_{CC}	60	DQ24	102	V_{CC}	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	V_{SS}	106	DQ53	148	NC
23	V_{SS}	65	DQ25	107	V_{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	WE0* †	69	DQ28	111	NC	153	DQ64
28	CAS0* †	70	DQ29	112	CAS1* †	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	RAS0*	72	DQ31	114	RAS1*	156	DQ67
31	OE0* †	73	V_{CC}	115	NC	157	V_{CC}
32	V_{SS}	74	DQ32	116	V_{SS}	158	DQ68
33	A0 †	75	DQ33	117	A1 †	159	DQ69
34	A2 †	76	DQ34	118	A3 †	160	DQ70
35	A4 †	77	DQ35	119	A5 †	161	DQ71
36	A6 †	78	V_{SS}	120	A7 †	162	V_{SS}
37	A8 †	79	PD1(V_{OL}) †	121	A9 †	163	PD2(V_{OL}) †
38	A10 †	80	PD3(NC)	122	A11 (Note) †	164	PD4(NC)
39	NC	81	PD5(V_{OL}) †	123	NC	165	PD6
40	V_{CC}	82	PD7	124	V_{CC}	166	PD8(V_{OL}) †
41	V_{CC}	83	ID0(V_{SS})	125	NC	167	ID1(V_{SS})
42	NC	84	V_{CC}	126	B0 †	168	V_{CC}

Notes: 1. Signals marked with "†" are buffered.
2. Address A11 is used only for 4K Refresh mode and is an NC pin for the 2K Refresh module.

DC CHARACTERISTICS

(V_{CC} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Condition		60		Unit	Note
				Min.	Max.		
Operating Current	I_{CC1}	RAS*, CAS* cycling; t_{RC} = min.	2KR	-	1846	mA	1, 2
			4KR	-	1396		
Standby current	I_{CC2}	LVTTL Interface RAS*, CAS* ≥ V_{IH} D_{out} = High-Z		-	82	mA	
		CMOS Interface RAS*, CAS* ≥ V_{cc} - 0.2V D_{out} = High-Z		-	46	mA	
RAS* -only Refresh Current	I_{CC3}	CAS* ≥ V_{IH}; RAS*, Address cycling @ t_{RC} = min	2KR	-	1846	mA	2
			4KR	-	1396		
CAS*-before-RAS* Refresh Current	I_{CC4}	RAS*, CAS* cycling @ t_{RC} = min.	2KR	-	1846	mA	
			4KR	-	1396		
Hyper Page Mode Current	I_{CC5}	RAS* ≤ V_{IL} CAS*, Address cycling @ t_{PC} = min	2KR	-	1306	mA	1, 3
			4KR	-	1306		
Input Leakage Current	I_{LI}	0V ≤ V_{in} ≤ V_{CC}+0.3V		-90	90	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{out} ≤ V_{CC} D_{out} = Disable		-20	20	µA	
Output High Voltage	V_{OH}	High I_{out} = -2mA		2.4	-	V	
Output Low Voltage	V_{OL}	Low I_{out} = 2 mA		-	0.4	V	

Notes: 1. Values depend on output load condition when the device is selected. Maximum Values are specified at the output open condition.
2. Address can be changed once or less while RAS* = V_{IL}.
3. Address can be changed once or less while CAS* = V_{IH}.

CAPACITANCE

(TA =+25°C, V_{CC} = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address, CAS*, WE*, OE*)	C_{I1}	13	pF	1
Input Capacitance (RAS*)	C_{I2}	70	pF	1
Input/Output Capacitance (DQ0~DQ71)	$C_{I/O}$	20	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS* = V_{IH} to disable D_{out}.

AC CHARACTERISTICS

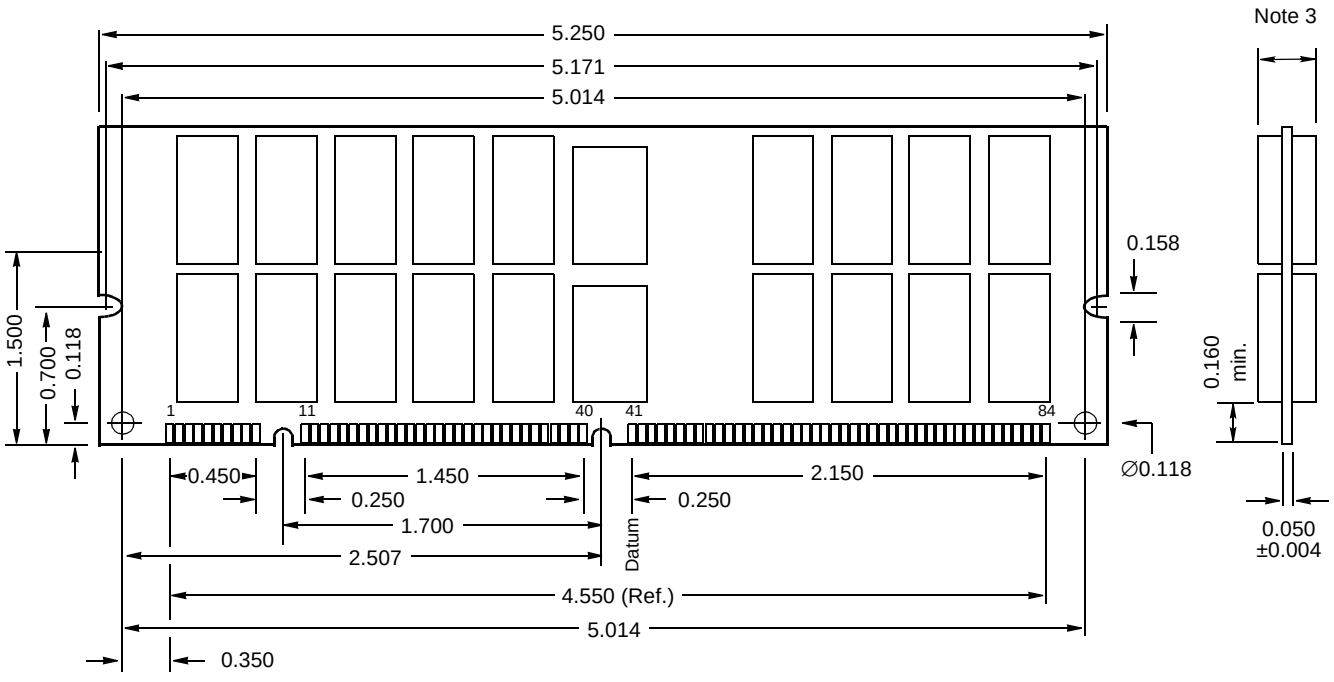
(TA = 0 to +70°C, V_{CC} = 3.3V±0.3V, V_{SS} = 0V)

Parameter		Symbol	60		Unit	Notes
			Min	Max		
Random read/write cycle time		t_{RC}	110	-	ns	
Access time from RAS*		t_{RAC}	-	60	ns	3,4
Access time from CAS*		t_{CAC}	-	20	ns	3,4,5
Access time from column address		t_{AA}	-	35	ns	3, 10
Transition time (rise and fall)		t_{T}	2	50	ns	2
RAS* precharge time		t_{RP}	40	-	ns	
RAS* pulse width		t_{RAS}	60	10000	ns	
RAS* hold time		t_{RSH}	20	-	ns	
CAS* hold time		t_{CSH}	44	-	ns	
CAS* pulse width		t_{CAS}	10	10000	ns	
RAS* to CAS* delay time		t_{RCD}	19	40	ns	4
RAS* to column address delay time		t_{RAD}	14	25	ns	10
CAS* to RAS* precharge time		t_{CRP}	10	-	ns	
Row address set-up time		t_{ASR}	5	-	ns	
Row address hold time		t_{RAH}	9	-	ns	
Column address set-up time		t_{ASC}	0	-	ns	
Column address hold time		t_{CAH}	10	-	ns	
Column address to RAS* lead time		t_{RAL}	35	-	ns	
Read command set-up time		t_{RCS}	0	-	ns	
Read command hold time to CAS*		t_{RCH}	0	-	ns	8
Read command hold time to RAS*		t_{RRH}	-1	-	ns	
Write command hold time		t_{WCH}	10	-	ns	
Write command pulse width		t_{WP}	10	-	ns	
Write command to RAS* lead time		t_{RWL}	20	-	ns	
Write command to CAS* lead time		t_{CWL}	10	-	ns	
Data-in set-up time		t_{DS}	-1	-	ns	9
Data-in hold time		t_{DH}	15	-	ns	9
Refresh period	2KR	t_{REF}	-	32	ms	
	4KR		-	64		
Write command set-up time		t_{WCS}	0	-	ns	7
CAS* set-up time (CBR refresh)		t_{CSR}	15	-	ns	1
CAS* hold time (CBR refresh)		t_{CHR}	9	-	ns	1
RAS* precharge to CAS* hold time		t_{RPC}	4	-	ns	
Access time from CAS* precharge		t_{CPA}	-	40	ns	3, 11
Hyper page mode cycle time		t_{HPC}	25	-	ns	
CAS* precharge time (Hyper page)		t_{CP}	10	-	ns	
RAS* pulse width (Hyper page)		t_{RASP}	60	100000	ns	12

Notes:
1. An initial pulse of at least 200µs is required after power-up followed by a minimum of eight RAS* cycles before device operation is achieved.
2. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.) and are assumed to be 5 ns for all inputs.
3. Measure with a load equivalent of 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) limit can be met; t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RACD}$ (max.).
6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is a non restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If t $_{WCS}$ Š t $_{WCS}$(min.) the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS* leading edge in early write cycles.
10. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) limit can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{ACP}.
12. t_{RASC} defines RAS* pulse width in fast page mode cycles.

Physical Dimensions

168-pin DIMM



Front View

Notes:
1. All dimensions are in inches.
2. Pin 85 is behind pin 1 on the back side.
3. Thickness = 0.350 for SOJ devices.
   = 0.280 for TSOP devices.

Ordering Information

E D C 8 B V 72 42 B _ - 60 J G - _ S

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15)

(1) **Memory Type**
F : Fast Page Mode (FPM)
E : Extended Data Out (EDO)

(2) **Module Shape**
S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**
A : 72-pin
B : 144-pin
C : 168-pin
D : 200-pin

(4) **Word Depth**
1 : 1M
2 : 2M
4 : 4M, etc.

(5) **Buffer Type**
B : Buffered
U : Unbuffered
R : Registered

(6) **Operating Voltage**
N : 5V
V : 3,3V

(7) **Data Width**
(ex. 8=x8, 32=x32, 72=x72 etc.)

(8) **Device Configuration / Refresh**
41 : 1Mx4, 1K Refresh Cycle
42 : 4Mx4, 2K Refresh Cycle
44 : 4Mx4, 4K Refresh Cycle
82 : 2Mx8, 2K Refresh Cycle
14 : 1Mx16, 4K Refresh Cycle
11 : 1Mx16, 1K Refresh Cycle

(9) **Module Revision *1**
Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(10) **Power consumption**
Blank : Standard
L : Low Power

(11) **Speed**
50 : 50ns
60 : 60ns
70 : 70ns

(12) **Package of Component**
J : SOJ
T : TSOP

(13) **Module Lead Finish**
S : Solder Plate
G : Gold Plate

(14) **Private Brand Name *2**
Blank : Common Products
G : FMG Brand

*2 This column is applicable to custom modules, NOT applicable to JEDEC standard commodity products

(15) **Assembly & Test Site**
S : Smart Modular Technologies

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Memory Marketing Dept.
4-1-1, Kamikodanaka Nakahara-ku,
Kawasaki 211-88, Japan
Tel: +81-44-754-3767
Fax: +81-44-754-3343

Internet: http://www.fujitsu.co.jp/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street
San Jose, CA 95134-1804, USA.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center (Mon-Fri: 7am-5pm (PST))
Tel: +1-800-866-8608
Fax: +1-408-922-9179

Internet: http://www.fujitsumicro.com/

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich–Buchschlag
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

Internet: http://www.fujitsu-ede.com/

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#05-08, 151 Lorong Chuan
NewTechPark
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

Internet: http://www.fsl.com.sg/

Printed in Germany