

EDC2UV6482B-60(J/T)G-S

16MByte (2M x 64) CMOS EDO DRAM Module - 3.3V

General Description

The EDC2UV6482B-60(J/T)G-S is a high performance, EDO (Extended Data Out) 16-megabyte dynamic RAM module organized as 2M words by 64 bits, in a 168-pin, dual-in-line (DIMM) memory module.

The module utilizes eight, Fujitsu MB81V17805B-60(PJ/PFTN) CMOS 2Mx8 EDO dynamic RAMs in a surface mount package on an epoxy laminate substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

Control lines provided are such that byte control is possible. Serial PD on the module is provided by using a 128 byte serial EEPROM.

Features

- High Density: 16MByte
- Fast Access Time of 60ns (max.)
- Low Power: 3.2 W (max.) - Active (60ns)
57.6mW (max.) - Standby (LVTTTL)
28.8mW (max.) - Standby (CMOS)
- LVTTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.000 inch

ABSOLUTE MAXIMUM RATINGS

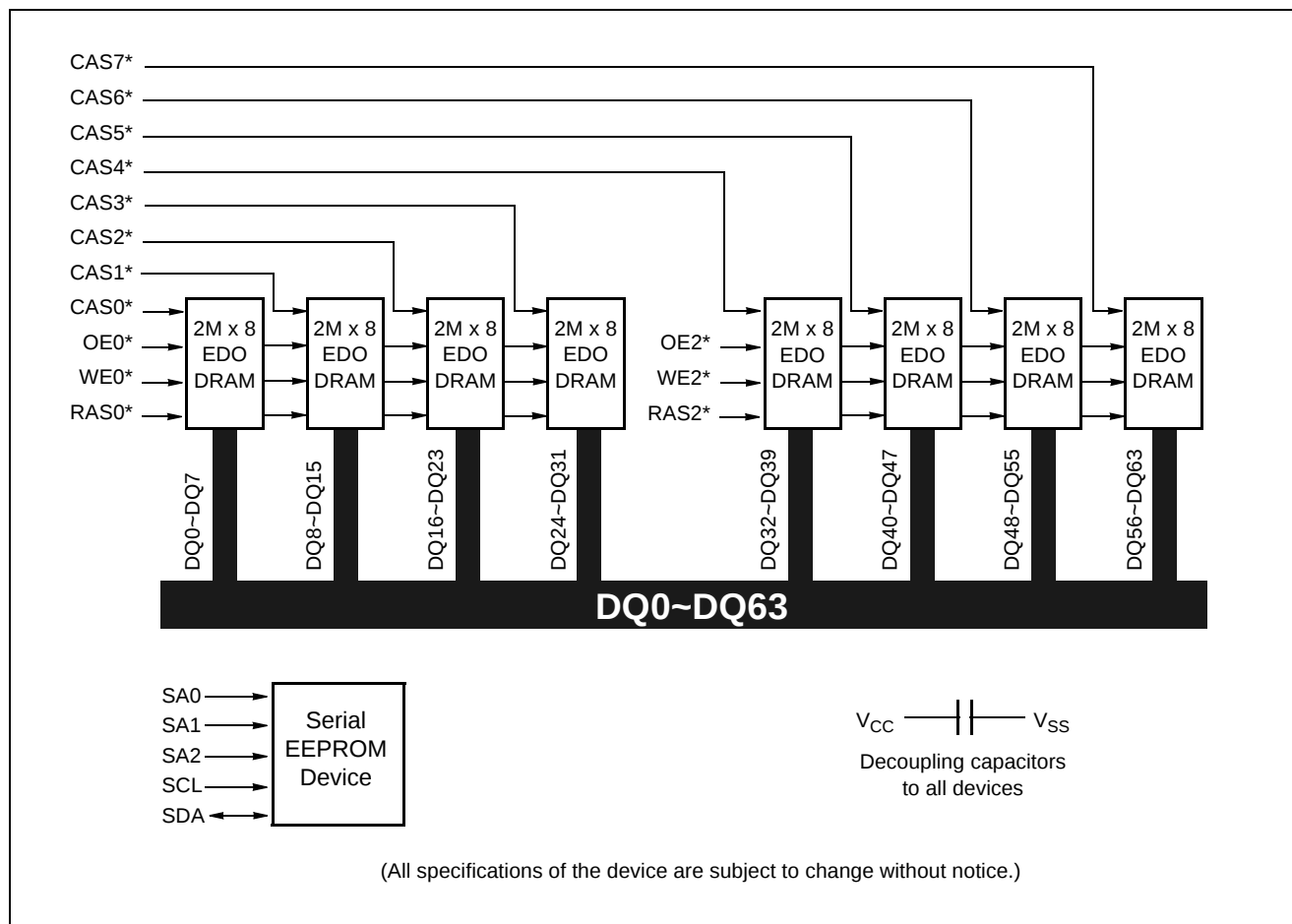
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V _{SS}	V _T	-0.5 to +4.6	V
Power Dissipation	P _T	8	W
Operating Temperature	T _{opr}	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +125	°C
Short Circuit Output Current	I _{OS}	50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	3.0	3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High voltage	2.0	-	V _{CC} +0.3	V
V _{IL}	Input Low voltage	-0.3	-	0.8	V

Functional Diagram



- Notes:
1. "*" signifies active low signal.
 2. Addresses A0 ~ A10 are connected to all DRAMs.

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Pin Name

A0~A11	Addresses	CAS0*~CAS7*	Column Address Strokes
DQ0~DQ63	Data Inputs/Outputs	SA0~SA2	Decode Inputs
WE0*, WE2*	Write Enable	SCL	Serial Clock
RAS0*, RAS2*	Row Address Strokes	V _{CC}	Power Supply
SDA	Serial Data Input/Output	V _{SS}	Ground
OE0*, OE2*	Output Enable	NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	OE2*	86	DQ32	128	NC
3	DQ1	45	RAS2*	87	DQ33	129	NC
4	DQ2	46	CAS2*	88	DQ34	130	CAS6*
5	DQ3	47	CAS3*	89	DQ35	131	CAS7*
6	V _{CC}	48	WE2*	90	V _{CC}	132	NC
7	DQ4	49	V _{CC}	91	DQ36	133	V _{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{CC}	101	DQ45	143	V _{CC}
18	V _{CC}	60	DQ20	102	V _{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC	105	NC	147	NC
22	NC	64	V _{SS}	106	NC	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	WE0*	69	DQ24	111	NC	153	DQ56
28	CAS0*	70	DQ25	112	CAS4*	154	DQ57
29	CAS1*	71	DQ26	113	CAS5*	155	DQ58
30	RAS0*	72	DQ27	114	NC	156	DQ59
31	OE0*	73	V _{CC}	115	NC	157	V _{CC}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V _{CC}	82	SDA	124	V _{CC}	166	SA1
41	V _{CC}	83	SCL	125	NC	167	SA2
42	NC	84	V _{CC}	126	NC	168	V _{CC}

DC CHARACTERISTICS

($V_{CC} = 3.3V \pm 0.3V$, $V_{SS} = 0V$, $T_A = 0$ to $+70^\circ C$)

Parameter	Symbol	Test Condition	60		Unit	Note
			Min.	Max.		
Operating Current	I_{CC1}	RAS*, CAS* cycling; $t_{RC} = \text{min.}$	-	880	mA	1, 2
Standby current	I_{CC2}	LVTTTL Interface RAS*, CAS* $\geq V_{IH}$ $D_{out} = \text{High-Z}$	-	16	mA	
		CMOS Interface RAS*, CAS* $\geq V_{CC} - 0.2V$ $D_{out} = \text{High-Z}$	-	8	mA	
RAS* -only Refresh Current	I_{CC3}	CAS* $\geq V_{IH}$; RAS*, Address cycling @ $t_{RC} = \text{min.}$	-	880	mA	2
CAS*-before-RAS* Refresh Current	I_{CC4}	RAS*, CAS* cycling @ $t_{RC} = \text{min.}$	-	880	mA	
Hyper Page Mode Current	I_{CC5}	RAS* $\leq V_{IL}$; CAS*, Address cycling @ $t_{PC} = \text{min.}$	-	720	mA	1, 3
Input Leakage Current	I_{LI}	$0V \leq V_{in} \leq V_{CC} + 0.3V$	-80	80	μA	
Output Leakage Current	I_{LO}	$0V \leq V_{out} \leq V_{CC}$ $D_{out} = \text{Disable}$	-10	10	μA	
Output High Voltage	V_{OH}	High $I_{out} = -2mA$	2.4	-	V	
Output Low Voltage	V_{OL}	Low $I_{out} = 2 mA$	0	0.4	V	

- Notes:
1. Values depend on output load condition when the device is selected. Maximum Values are specified at the output open condition.
 2. Address can be changed once or less while RAS* = V_{IL} .
 3. Address can be changed once or less while CAS* = V_{IH} .

CAPACITANCE

($T_A = +25^\circ C$, $V_{CC} = 3.3V \pm 0.3V$)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	45	pF	1
Input Capacitance (RAS0*, OE0, WE0)	C_{I2}	25	pF	1
Input Capacitance (CAS0*~CAS7*)	C_{I3}	10	pF	1
Input Capacitance (RAS2*, WE2*, OE2*)	C_{I4}	25	pF	1
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	12	pF	1, 2

- Notes:
1. Capacitance is measured with Boonton Meter or effective capacitance method.
 2. CAS* - V_{IH} to disable D_{out} .

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AC CHARACTERISTICS

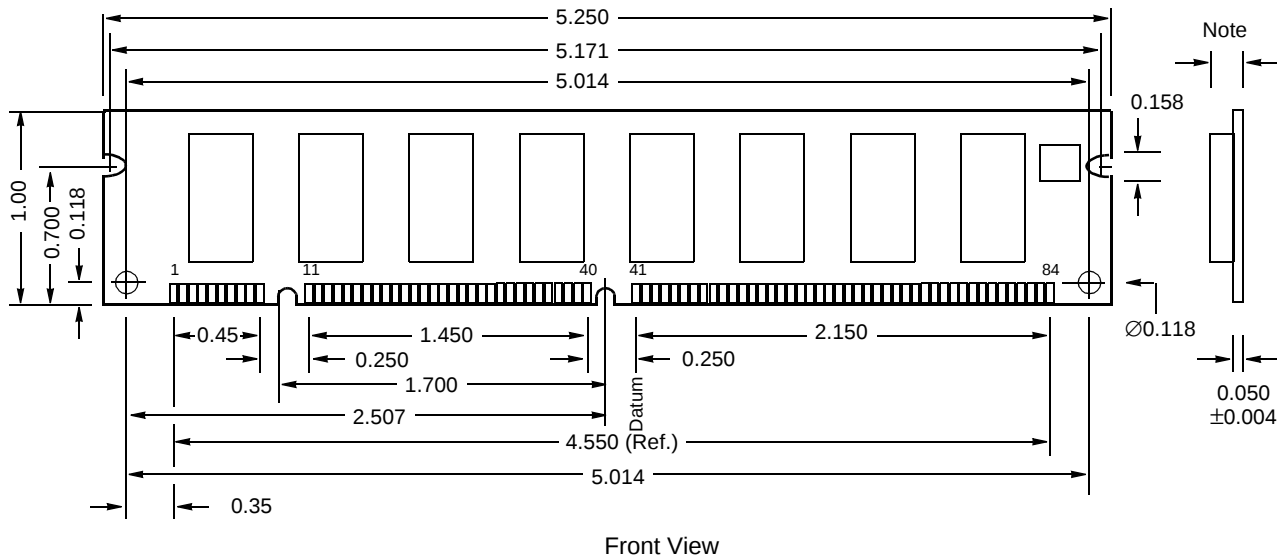
(TA = 0 to +70°C, V_{CC} = 3.3V±0.3V, V_{SS} = 0V)

Parameter	Symbol	60		Unit	Notes
		Min	Max		
Random read/write cycle time	t _{RC}	110	-	ns	
Access time from RAS*	t _{RAC}	-	60	ns	3, 4
Access time from CAS*	t _{CAC}	-	15	ns	3, 4, 5
Access time from column address	t _{AA}	-	30	ns	3, 10
Transition time (rise and fall)	t _T	2	50	ns	2
RAS* precharge time	t _{RP}	40	-	ns	
RAS* pulse width	t _{RAS}	60	10000	ns	
RAS* hold time	t _{RSH}	15	-	ns	
CAS* hold time	t _{CSH}	45	-	ns	
CAS* pulse width	t _{CAS}	10	10000	ns	
RAS* to CAS* delay time	t _{RCD}	20	45	ns	4
RAS* to column address delay time	t _{RAD}	15	30	ns	10
CAS* to RAS* precharge time	t _{CRP}	5	-	ns	
Row address set-up time	t _{ASR}	0	-	ns	
Row address hold time	t _{RAH}	10	-	ns	
Column address set-up time	t _{ASC}	0	-	ns	
Column address hold time	t _{CAH}	10	-	ns	
Column address to RAS* lead time	t _{RAL}	30	-	ns	
Read command set-up time	t _{RCS}	0	-	ns	
Read command hold time to CAS*	t _{RCH}	0	-	ns	8
Read command hold time to RAS*	t _{RRH}	0	-	ns	
Write command hold time	t _{WCH}	10	-	ns	
Write command pulse width	t _{WP}	10	-	ns	
Write command to RAS* lead time	t _{RWL}	15	-	ns	
Write command to CAS* lead time	t _{CWL}	10	-	ns	
Data-in set-up time	t _{DS}	0	-	ns	9
Data-in hold time	t _{DH}	10	-	ns	9
Refresh period (2048 cycles)	t _{REF}	-	32	ms	
Write command set-up time	t _{WCS}	0	-	ns	7
CAS* set-up time (CBR refresh)	t _{CSR}	10	-	ns	1
CAS* hold time (CBR refresh)	t _{CHR}	10	-	ns	1
RAS* precharge to CAS* hold time	t _{RPC}	5	-	ns	
Access time from CAS* precharge	t _{CPA}	-	35	ns	3, 11
Hyper page mode cycle time	t _{HPC}	25	-	ns	
CAS* precharge time (Hyper page)	t _{CP}	10	-	ns	
RAS* pulse width (Hyper page)	t _{RASP}	60	100000	ns	12

- Notes:
1. An initial pulse of at least 200 μ s is required after power-up followed by a minimum of eight RAS* cycles before device operation is achieved.
 2. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.) and are assumed to be 5 ns for all inputs.
 3. Measure with a load equivalent to 2 TTL loads and 100pF.
 4. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) limit can be met; t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 5. Assumes that $t_{RCD} \geq t_{RAD}$ (max.).
 6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL} .
 7. t_{WCS} is non restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}(\text{min.})$ the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
 8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. These parameters are referenced to the CAS* leading edge in early write cycles.
 10. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ limit can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
 11. Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{ACP} .
 12. t_{RASC} defines RAS* pulse width in fast page mode cycles.

Physical Dimensions

168-pin (84x2) DIMM



- Notes:
1. All dimensions are in inches.
 2. Pin 85 is behind pin 1 on the back side.
 3. Thickness = 0.202 for SOJ DRAMs
= 0.125 for TSOP DRAMs

EDC2UV6482B-60T G - S

Ordering Information

E D C 2 U V 64 82 B _ - 60 T G - _ S
(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15)

(1) **Memory Type**

F : Fast Page Mode (FPM)
E : Extended Data Out (EDO)

(2) **Module Shape**

S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**

A : 72-pin
B : 144-pin
C : 168-pin
D : 200-pin

(4) **Word Depth**

1 : 1M
2 : 2M
4 : 4M, etc.

(5) **Buffer Type**

B : Buffered
U : Unbuffered
R : Registered

(6) **Operating Voltage**

N : 5V
V : 3.3V

(7) **Data Width**

(ex. 8=x8, 32=x32, 72=x72 etc.)

(8) **Device Configuration / Refresh**

41 : 1Mx4, 1K Refresh Cycle
42 : 4Mx4, 2K Refresh Cycle
44 : 4Mx4, 4K Refresh Cycle
82 : 2Mx8, 2K Refresh Cycle
14 : 1Mx16, 4K Refresh Cycle
11 : 1Mx16, 1K Refresh Cycle

(9) **Module Revision *1**

Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(10) **Power consumption**

Blank : Standard
L : Low Power

(11) **Speed**

50 : 50ns
60 : 60ns
70 : 70ns

(12) **Package of Component**

J : SOJ
T : TSOP

(13) **Module Lead Finish**

S : Solder Plate
G : Gold Plate

(14) **Private Brand Name *2**

Blank : Common Products
G : FMG Brand

*2 This column is applicable to custom modules, NOT applicable to JEDEC standard commodity products

(15) **Assembly & Test Site**

S : Smart Modular Technologies

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