

Wide Band Power FET

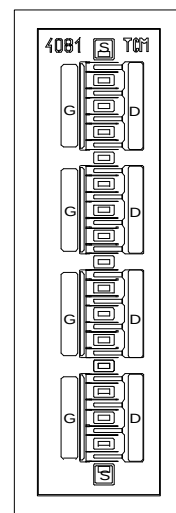
GaAs Field Effect Transistor

Description

The EC5724 device, available in chip form, is a power GaAs Field Effect Transistor, designed for wideband oscillator and amplifier applications, up to 18GHz. Individual via hole connection is made between each source pad and the gold plated back face metallization, through the 25 μ m thick GaAs substrate. The 0.5 μ m Aluminium gates are protected by a layer of silicon nitride. It is available in chip form.

Main Features

Output power at 1dB compression point :
 Single cell (600 μ m) : 24dBm
 Four cells (2400 μ m) : 30dBm
 Gain at 1dB compression point :
 Single cell (600 μ m) : 8dB at 18GHz
 Four cells (2400 μ m) : 7dB at 18GHz
 Chip size : 1.52 x 0.51 x 0.065 mm



G: Gate
 D: Drain
 S: Source

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Idss	Saturated drain current	640	960	1280	mA
P1dB	Output power at 1dB gain compression	29	30		dBm
Ga	Associated gain	6	7		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

Electrical Characteristics

Tamb = +25°C

Symbol	Parameter	Test Conditions	Single cell			Four cells			Unit
			Min	Typ	Max	Min	Typ	Max	
Idss	Saturated drain current	Vds= 1V Vgs=0V	160	240	320	640	960	1280	mA
Vp	Pinch off voltage	Vds= 1V Ids=Idss/100	-4	-3	-2	-4	-3	-2	V
Gm	Transconductance	Vds= 1V Ids=Idss/2	70	80		280	320		mS
Igsd	Gate to source/drain leakage current	Vgsd= -6V			600			2400	μA
Rth	Channel-case thermal resistance			60			15		°C/W

Dynamic characteristics

Tamb = +25°C

Symbol	Parameter	Test Conditions	Single cell		Four cells		Unit
			Min	Typ	Min	Typ	
P1dB	Output power at 1dB gain compression	Vds= 8V F= 18GHz	23	24	29	30	dBm
Ga	Associated gain at 1dB gain compression	single cell: Ids= 110mA	7	8	6	7	dB
ηadd	Power added efficiency	four cells: Ids= 440mA	20	25	20	25	%

Absolute Maximum Ratings (1)T_{amb} = +25°C

Symbol	Parameter		Values	Unit
Vds	Drain to source voltage		10	V
Ids	Drain current	single cell	320	mA
		four cells	1280	mA
Pt	Total power dissipation	single cell	1.5	W
		four cells	6	W
Vgs	Gate to source voltage		-6	V
Tch	Operating channel temperature		175	°C
Tstg	Storage temperature range		-65 to +175°C	°C

(1) Operation of this device above any one of these parameters may cause permanent damage

Typical Scattering Parameters

"S" Parameters, operating conditions single cell :

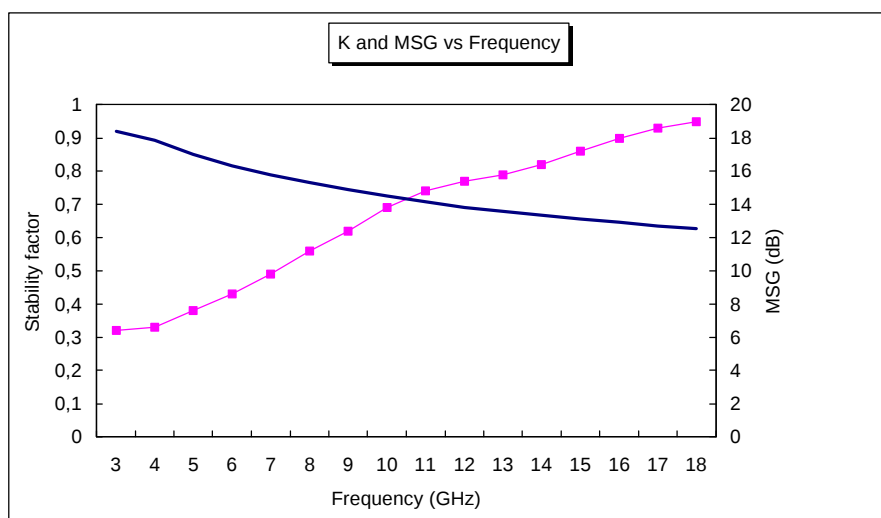
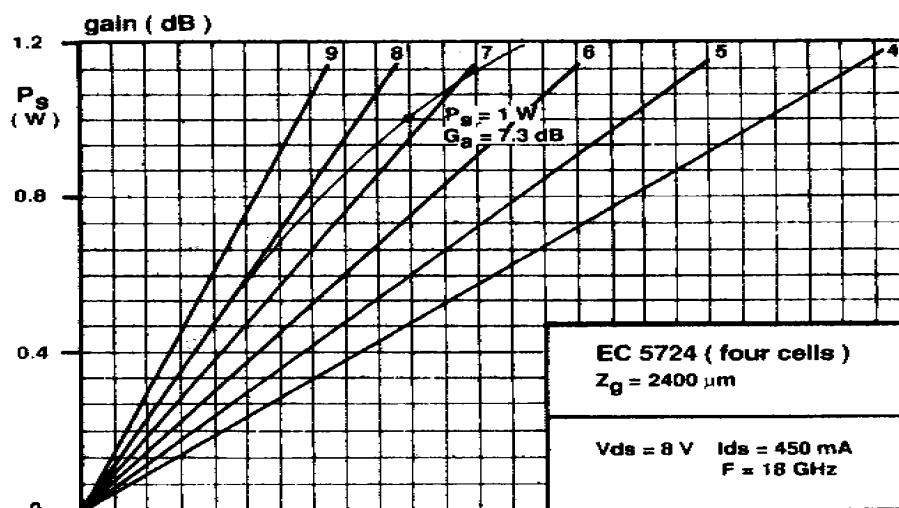
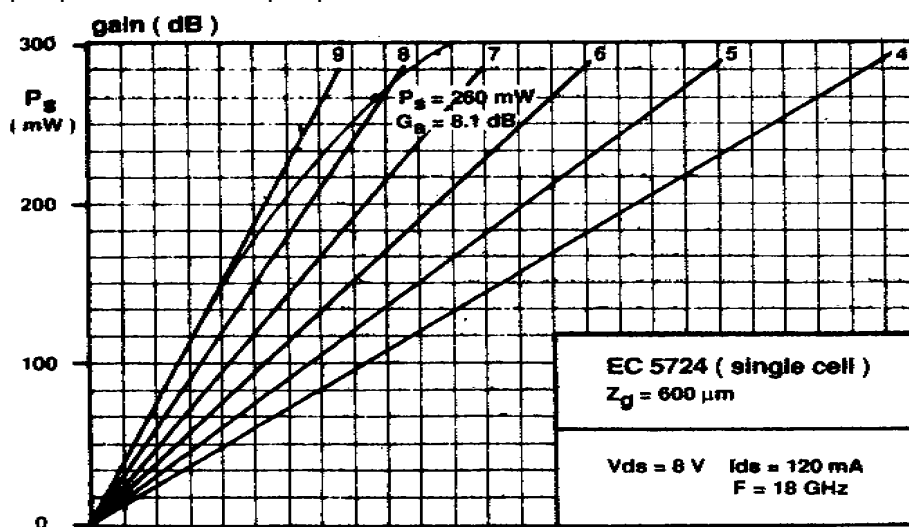
V_{ds} = 8V, I_{ds} = 110mA, including 0.10nH gate and 0.20nH drain serie inductances

Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°
3	-0.95	-82.7	-25.62	36.2	11.16	118.1	-5.57	-51.5
4	-1.04	-99.5	-25.26	25.6	10.47	104.3	-5.53	-63.2
5	-1.14	-112.2	-24.86	16.9	9.15	92.6	-5.35	-73.3
6	-1.18	-122.3	-24.75	9.3	7.89	82.5	-5.09	-82.0
7	-1.21	-130.5	-24.82	2.9	6.70	72.5	-4.77	-89.6
8	-1.23	-137.4	-25.01	-2.4	5.57	65.1	-4.39	-96.2
9	-1.23	-142.8	-25.25	-6.9	4.49	57.5	-4.02	-102.4
10	-1.23	-147.3	-25.51	-10.7	3.48	50.5	-3.69	-108.3
11	-1.22	-151.3	-25.76	-13.8	2.54	44.2	-3.37	-113.2
12	-1.19	-154.6	-25.99	-16.5	1.67	38.1	-3.07	-118.1
13	-1.13	-157.8	-26.28	-19.2	0.86	32.2	-2.82	-122.9
14	-1.09	-161.3	-26.61	-21.4	0.09	26.6	-2.60	-126.7
15	-1.09	-164.5	-26.91	-22.1	-0.65	20.9	-2.35	-130.1
16	-1.11	-167.2	-27.17	-22.3	-1.35	15.7	-2.14	-133.9
17	-1.11	-169.5	-27.35	-23.0	-2.00	10.9	-1.98	-137.7
18	-1.12	-171.8	-27.41	-23.1	-2.32	6.2	-1.91	-140.6

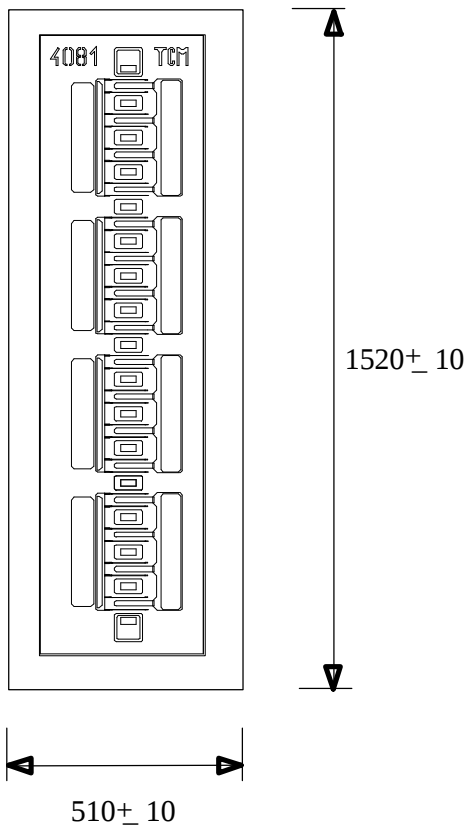
Typical results

Tamb = +25°C

Typical output power versus input power



Chip Mechanical Data



dimensions in μm

Drain area = $255 \times 55 \mu\text{m}$

Gate area = $255 \times 55 \mu\text{m}$

Thickness = $65 \pm 15 \mu\text{m}$

Recommended die attach :

Stage temperature = 300°C
(minimize temp. and time whenever possible)

Preforms = Au/Sn (80/20)

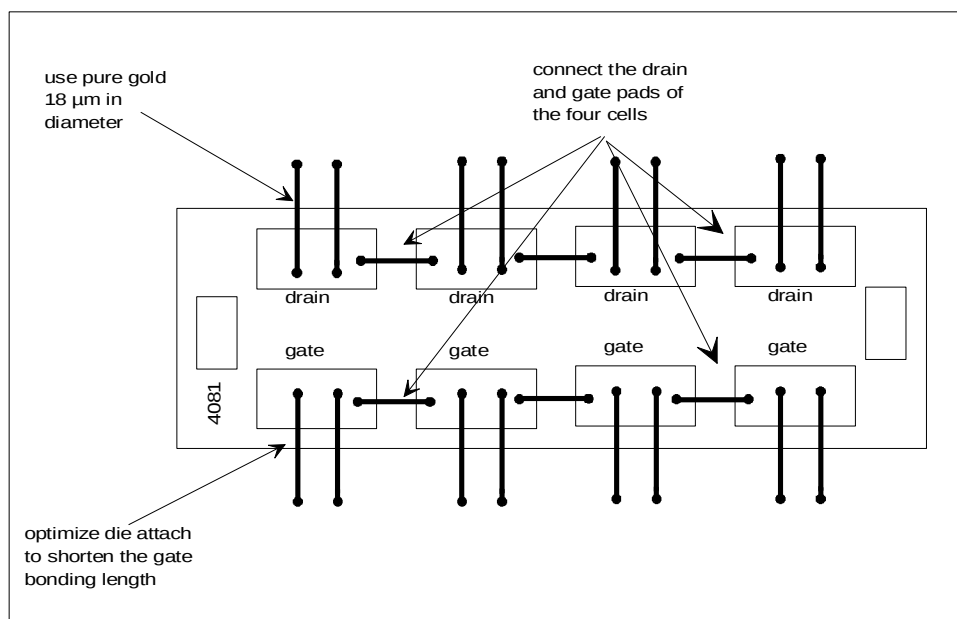
Atmosphere : dry nitrogen or forming gas flow

Recommended bonding :

$\varnothing 18 \mu\text{m}$ very pure gold wire

(Thermal compression)

The bonder should be properly grounded.



Optimum bonding

Ordering Information

Chip form : EC5724-99X/0

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